ENGINEERING DESIGN GUIDELINES FOR ELECTROMAGNETIC PULSE HARDENING OF NAVAL EQUIPMENT(U) ELECTRO MAGNETIC APPLICATIONS INC DENVER CO S R ROGERS ET AL. 15 JUL 81

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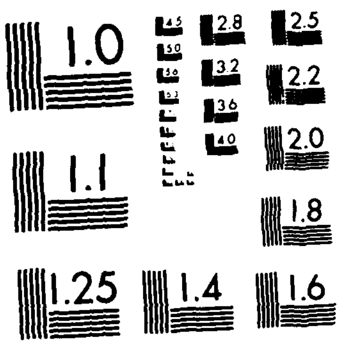

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EMA ELECTRO MAGNETIC APPLICATIONS, INC.
1978 SOUTH GARRISON
DENVER, COLORADO 80227

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FINAL REPORT

15 July 1981

Prepared for

Naval Surface Weapons Center
White Oak
Silver Spring, Maryland 20910

Under Contract N60921-80-C-0190

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This document is intended to be used by engineers who design and manufacture shipboard equipment. It is complete in the sense that both the EMP hazard and the means of mitigating the hazard (hardening) are presented. The hazard is described, which not only discusses EMP generation in a general sense, but it also presents specific threat levels for EMP fields and transient currents and voltages induced on cables and antennas which are connected to electronic equipment. This specific threat constitutes an EMP survivability criteria which must be met by the mission critical equipment.

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ABSTRACT (Cont.)

The necessary hardening technology areas include volume shielding, cable shielding and connectors, interface susceptibility analysis, terminal protective devices, upset and upset hardening, common mode rejection techniques, optical isolation, and grounding/bonding techniques. Test techniques which can verify equipment hardness are presented along with methods to observe the equipment's hardness and maintain the hardness.

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CHAPTER 1

INTRODUCTION

When a nuclear weapon is detonated in the exoatmosphere, a large area of the surface of the earth can be illumined by a large electromagnetic pulse (EMP) field. This field consists typically of a plane wave of 50 kV/m peak electric field amplitude, a 10 ns risetime, and an energy density of nearly 1 Joule/m^2. If a ship of a few thousand square meters surface area is in the region illumined by the EMP, it is easy to see that the EMP energy incident on a ship can be a few thousand Joules. Test data has demonstrated that as little as 10 μJoules is sufficient to cause an integrated circuit to be damaged. Thus, it is clear that several orders of magnitude of shielding or isolation is necessary in order to prevent semi-conductor devices from being damaged by an incident EMP.

Fortunately, nearly all of the energy incident on a ship is reflected away because of the natural process of electromagnetic scattering from the ship's metallic surface, and only a very small fraction of the total incident energy propagates into a ship's interior by means of antennas, masts, exposed cables, and apertures. Simulated EMP tests have shown that current and voltage levels on a ship's internal cabling present a potentially serious hazard to shipboard electronics. This hazard takes the form of either permanently damaging electronic components or temporarily upsetting electronic circuits.

Because of this potential hazard, it is necessary to harden the mission critical shipboard electronics. The objective of this document is to clearly describe the available techniques, methods, and information that can be used by design engineers to assess the EMP survivability status of electronic equipment, and to design, develop, and validate hardened electronic equipment.

This document is intended to be used by engineers who design and manufacture shipboard equipment. It is complete in the sense that both the EMP hazard and the means of mitigating the hazard (hardening) are presented. The hazard is described in Chapter 2, which not only discusses EMP generation in a general sense, but it also presents specific threat levels for EMP fields and transient currents and voltages induced on cables and antennas which are connected to electronic equipment. This specific threat constitutes an EMP survivability criteria which must be met by the mission critical equipment.

The remainder of this document describes how the criteria can be met. The necessary hardening technology areas include volume shielding (Chapter 3), cable shielding and connectors (Chapter 4), interface susceptibility analysis (Chapter 5), terminal protective devices (Chapter 6) upset and upset hardening (Chapter 7) common mode rejection techniques and optical isolation (Chapter 8), and grounding and bonding techniques (Chapter 9). Test techniques which can verify equipment hardness are given in Chapter 10. Finally, the problem of observing equipment's hardness and keeping it hard are discussed in Chapter 11.

CHAPTER 2

SUMMARY OF ELECTROMAGNETIC PULSE SOURCES AND EFFECTS

2.0 Executive Summary

Chapter 2 discusses briefly the generation of EMP and how EMP energy couples to electronic circuitry. The most important material is contained in Section 2.4 which defines the environments to which newly manufactured equipment must be hardened.

2.1 High Altitude EMP Generation

A nuclear detonation generates large amounts of energy which can be grouped in such categories as blast, thermal radiation, nuclear radiation, and electromagnetic pulse (EMP). This section provides an introduction to EMP generation. For further technical descriptions of EMP, the reader should consult the References [2.1-2.8].

The energy contained in EMP is similar to that in EM waves generated by a lightning strike, but the high frequency energy content in EMP is a much larger fraction of the total pulse energy.

While every detonation (whether below ground, on the surface, at medium altitude, or at high altitude) produces EMP, the extent, duration, and intensity vary greatly with altitude. The high altitude case (height of burst (HOB) greater than 20 miles) is the subject of particular interest *in this document.*

The electromagnetic fields in EMP are created by the coherent motion of large numbers of electrons. The basic process for the creation of the electrons is shown in Figure 2.1. The nuclear detonation generates gamma rays; these gamma rays collide with air molecules and by Compton scattering eject high-energy electrons. The motion of these Compton electrons (e_c) outward is the Compton current.

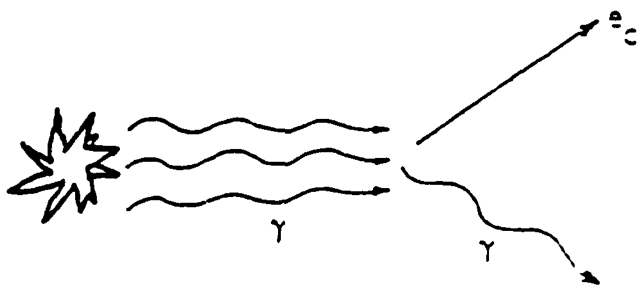


Figure 2.1 Simple Illustration of Compton Current

A spherically symmetric current distribution does not radiate an electromagnetic field; thus, a nuclear detonation in a perfectly homogeneous atmosphere would not radiate EMP (an intense field is created in a volume around the burst, however).

The earth's atmosphere varies with altitude making it inhomogeneous. Thus, a nuclear detonation above the earth's atmosphere produces Compton currents which are asymmetrical and, therefore, capable of generating electromagnetic fields which propagate to great distances. The gamma rays traveling toward the earth interact with air molecules and create Compton currents in a large region of the upper atmosphere. These currents interact with the earth's magnetic field to generate the EMP which then propagates downward with little attenuation along the path of the initial gamma rays. The resulting area of coverage encompasses all points within line-of-sight of the burst (but with amplitude variations from point to point). Figure 2.2 shows the coverage from bursts at 60 miles (radius of coverage of about 685 miles) and 250 miles (radius of coverage of about 1375 miles). In this high altitude case, the energy density in the EMP is large. Because some of this energy will be coupled to sensitive electronic circuits through currents induced on the conductors of the ship, circuit upset or permanent damage can result.

Figure 2.3 shows a simple illustration of the generation of EMP from a high-altitude detonation. In References 2.5 and 2.6 are presented technical discussions of the high altitude EMP generation process and comparisons of theoretical predictions with the limited experimental data from high altitude Pacific tests.

In a general nuclear exchange, high-altitude bursts will occur because of the deployment of U.S. and enemy ABM systems. For these reasons, high-altitude burst EMP is a significant threat to shipboard equipments.

An extensive bibliography of EMP literature is presented in Volume IV of Reference 2.3, and a much more complete discussion of EMP sources is presented in Reference 2.7.

2.2 EMP Coupling to Ships

The process by which EMP energy appears on and within a ship is termed coupling.

The coupling of EMP into electronics systems has received considerable attention over the last 15 years. Historically, most of the coupling effort in the overall EMP community has been applied to aerospace and ground based systems with only a relatively small amount of direct application to shipboard systems. However, the general content of the overall EMP coupling technology does apply to ships as well.

EMP coupling can be divided into three categories as follows:

External Coupling
External coupling is the process by which currents and charges (or, alternatively, magnetic and electric fields) are induced on the ship's exterior surface. These fields are really of no consequence in themselves except that they act as sources which can propagate energy into the ship's interior.

Internal Coupling
Internal coupling can be defined as the penetration of local fields through the hull or deck surface. There are several types of penetrations including

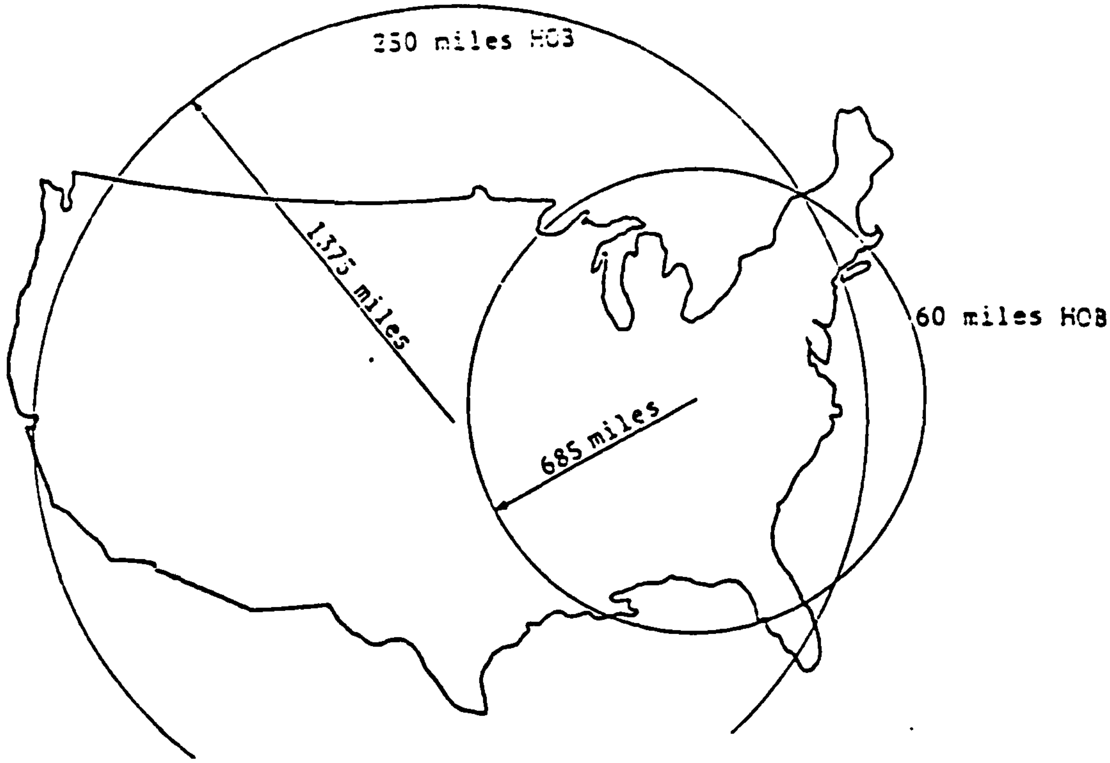


Figure 2.2 Area of Coverage of EMP from High-Altitude Detonations

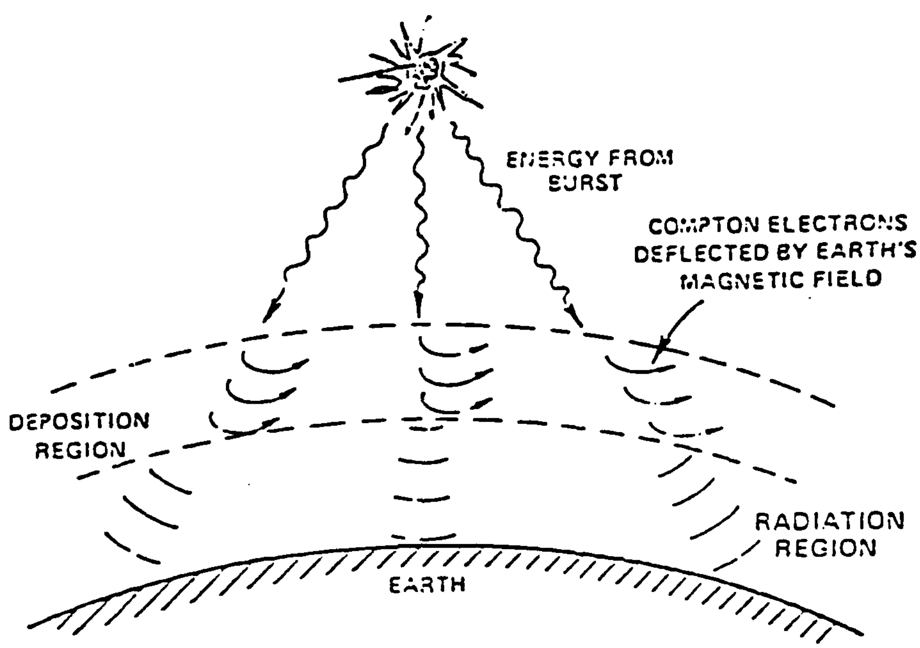


Figure 2.3 Illustration of the Basic Geometry of the High-Altitude Burst [2.3]

antennas, apertures (individual windows), exposed cables, and diffusion. It should be noted that for ships, diffusion through the skin can always be neglected for metal surfaces because penetration by other processes dominates the internal fields by several orders of magnitude. Also it should be noted that the concept of separating external and internal coupling processes is valid only if the penetration causes only a small perturbation on the surface fields. For the case of large apertures or penetrations such as masts, the external and internal coupling problems are really inseparable.

Interior Propagation

Interior propagation can be defined as the propagation of EMP induced transients within the interior of the ship and the determination of voltages and currents on connector pins of electronic boxes. This propagation occurs principally by means of the ship's electrical cables which are used for normal power and signal transmission. These cables also form efficient transmission lines by which the EMP induced signals readily propagate from one part of the ship to another. These transient signals can be described in terms of voltages and currents that ultimately appear at the cable terminations where sensitive electron circuits such as computers or communication equipment can be permanently damaged or temporarily upset.

There is a considerable body of literature on the subject of EMP coupling. The interested reader is referred to References 2.8 through 2.12 for further information.

2.3 The Approach to EMP Hardening

In the context of this document, hardening refers to the process of incorporating design practices with the objective of providing equipment survivability to the EMP environment. Therefore, the hardening process requires two data points: 1) the EMP environment, and 2) the damage or upset threshold of the electronics. Once these two facts are known, one can determine the total mitigation of the EMP transient required for survivability. The main problems confronting the designer are to determine where to apply the hardening practices, what practices should be applied, and how much hardening is required where they are applied.

The usual approach, often referred to as the zonal approach, and which is found to be effective, is to first identify the topology of the systems which require hardening. Identification of this topology establishes zone boundaries or surfaces through which EMP energy must pass to reach sensitive electronics. The energy can pass through these zone boundaries by field diffusion, apertures and by conducted transients. The total shielding effectiveness of the successive boundaries must be large enough to reduce the energy passed to tolerable levels. At each boundary, the hardening practices applied for each penetration must be balanced. This means, for example, that it would not be sensible to try to get 100 dB of shielding from the enclosure shield if the cables penetrating the enclosure were not hardened to a comparable level.

This concept of a zonal philosophy is illustrated in Figure 2.4, which shows one possible topological identification for shipboard applications. Various shielding layers are identified which separate regions of space into distinct environments. In this case, the shield layers are identified as the hull

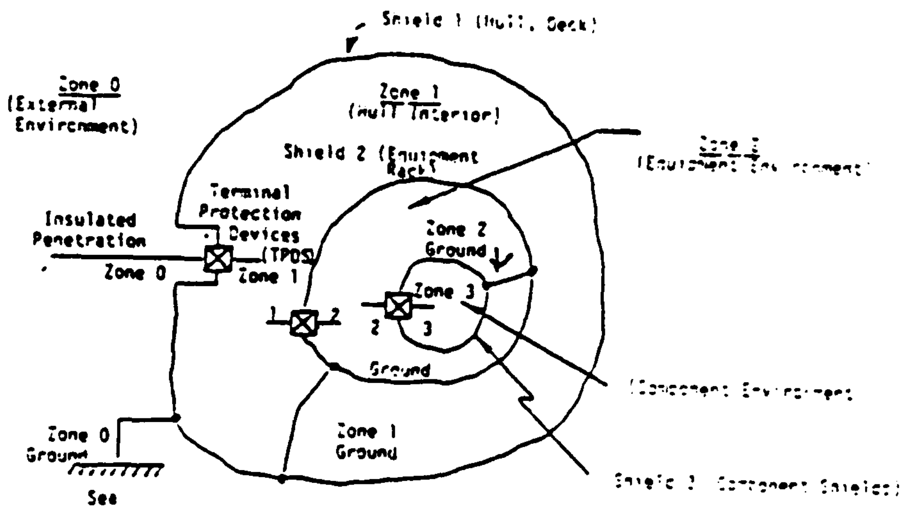


Figure 2.4 A Possible Zonal Development for Shipboard Equipment Hardening

(including the deck), equipment rack shields, and the individual shields of equipments within the equipment rack. It is noted that another layer could be identified if there existed a shielded room or bay, for example. Also shown is the topology of the grounding scheme which connects the shielding layers to each other. Between these shield layers are the zones for which environments can be established.

Once the zones and the shielding layers have been identified, the next step is to determine how much hardening should be achieved at each layer. This process is called allocation. The allocation must be reasonable in terms of cost and realizability, that is, the allocation for a given layer must be able to be readily obtained at a reasonable cost. In addition, it must be realized that one must be careful about adding up attenuations. For example, if a sheet of material shields the peak electric field by 40 dB, 2 sheets do not necessarily cause 80 dB attenuation.

In order to accomplish the allocation, some measure of mitigation must be defined. Several measures might be used, such as voltage, current, electromagnetic fields, power, or energy. Allocation can then be defined in terms of how much one of these quantities is reduced at each zone boundary.

A useful allocation measure is energy, because the damaging effects of the HEMP induced transients on conductors can be described as an energy transfer phenomenon. The energy picked up on a conductor is focused on a component part of relatively small volume. The component part will heat up until some permanent change results.

In order to develop an allocation strategy, it is necessary to establish the minimum threshold for the equipment interface pins. Given the minimum threshold and the worst case threat levels, the allocation can logically evolve. The threshold can be determined by testing or the analytical procedures described in Chapter 5.

Also in order to accomplish a meaningful hardening allocation, a numerical means is required that could permit the specification and measurement of design practice effectiveness. A simple technique is desirable. If energy is chosen as a measure of threat levels and thresholds, the effectiveness of a treatment expressed as the ratio of input energy to the energy penetration through the shield is a logical choice. Further, since the problem deals with very large and very small quantities, a logarithmic approach appears necessary. The quantity DBE can be defined as

$$DBE = 10 \log(\xi_{in}/\xi_{out}) \tag{2.1}$$

to be the measure of effectiveness. If, for example, an unshielded cable picked up 1000 Joules on the signal wires in a certain environment while the specified cable shield reduced the signal wire pickup to 1 Joule, the effectiveness of the design practice of cable shielding would provide 30 DBE. By defining DBE in terms of "dB of energy", a simple tally can be made to determine if sufficient hardening is allocated. The difference of the threat level expressed in DBJ and the minimum threshold (DBJ) should equal the sum of the allocated DBE.

Again, it must be said that this simple use of energy must take into account the factors of signal amplitude (voltage, current, and charge and current density), rate-of-rise, and bandwidth to assure true design practice effectiveness. The energy measure allows a simple view of a more complex situation.

Finally, an allocation matrix can be defined. This matrix defines the levels of mitigation that can be achieved by applying certain hardening practices to the zones and their boundaries. The hardening problem then becomes one of actually implementing these hardening practices and assuring that they really function as planned.

For more information on topological concepts, the reader is referred to References 2.8, 2.13 and 2.14.

2.4 EMP Survivability Criteria for Ships

2.4.1 Background

In the past EMP survivability requirements were often imposed on the contractor's task to convert these environments to electrical parameters (i.e., transient voltages, currents, and surface fields) in order to design, develop and test electronic systems, subsystems and black boxes. This has resulted in many problems, uncertainties and ambiguities. The purpose of this section is to present the equipment level EMP survivability requirements in a common and realizable set of criteria and procedures for the numerous equipments and subsystems that must be able to operate in an EMP environment.

This section defines the EMP environments as a set of requirements and test limits for the determination of the (EMP) survivability characteristics of electronic, electrical, and electromechanical equipment. The requirements shall be applied for electronic/electrical equipment procurements, as specified in the individual equipment specifications, or the contract or order.

The EMP survivability criteria levels presently incorporated in this document are based on the results of EMP tests of the HMCS HURON, HMS SHEFFIELD, USS GLOVER, ex-USS VALCOUR and ex-USS LAFFEY. Therefore, the present criteria are based on tests of Destroyer Class ships. The best available projection of the effectiveness of platform level hardening of ships conforming to MIL-STD-1310D [2.15] is that the maximum interior bulk cable (i.e. the portion of the cable run within the protection envelope) current will not exceed ten (10) amperes. The interface cable transients that are specified for the interior cables of hardened Destroyer CLASS ships (i.e., Section 2.4.4.3) are based on this projection.

The present criteria are only directly applicable to unhardened Destroyer CLASS ships and cannot be extended to other ship CLASSES with high confidence. Nevertheless, until additional quantitative data is available, the criteria presented should be applied for all hardened and unhardened ship CLASSES.

The requirements of this section shall be applied to electronic, electrical, and electromechanical equipment as indicated herein after:

Critical Equipment - The requirements of this section shall be applied to all critical equipments which would affect overall system performance and mission success or safety if degraded or malfunctioned. All applicable tests required by this document shall be performed and a test report shall be submitted as part of the equipment procurement contract. Application of suppression measures and/or circumvention techniques to meet the requirements shall be detailed in the test report.

Non-Critical Equipment - Equipment not intended for use in tactical or critical military areas and equipment that would not affect overall system performance and mission success or safety if degraded or malfunctioned are excempt from meeting the requirements of this standard unless specifically required by the procuring activity.

2.4.2 Survivability Requirements

The EMP environment criteria consist of an interface pin current and/or voltage environment, a bulk cable current/voltage environment, and an electromagnetic field environment. The equipment shall operate within the essential performance limits of the equipment specification after being subjected to the EMP environment criteria. If the equipment is to be installed on an unhardened ship and the equipment hardening cost to meet the associated non-antenna interface pin or cable transients is prohibitive, the EMP survivability criteria shall not be completely waived unless the cost to meet the ten (10) amp interior cable current for hardened platforms is also prohibitive. Instead, the equipment should be hardened to the ten (10) amp interior cable current criteria that applies for hardened platforms; then if platform hardening is incorporated during the future SHIPALT, the equipment will have

the necessary level of EMP survivability. Any partial or complete waiver of the EMP survivability criteria must be approved by the procuring activity, ELEX-51024, and MAT-08DE.

Critical equipment shall have a survivability probability greater than 0.9 with a least a 0.5 confidence factor for the EMP environment criteria levels specified in this standard. Equipment survivability is discussed in Section 10.4. Failure is defined as the loss, degradation, or malfunction of any essential function of the equipment that would affect overall system performance and mission success or safety. Transient deviations are allowable during occurrence of the EMP effects provided the applicable detection and circumvention techniques, reset capability, and recovery times satisfy the functional requirements of the detailed specification.

2.4.3 Interface Pin Transients

2.4.3.1 Applicability

The EMP induced current and voltage transients that would appear at the non-antenna interface pins are a function of the equipment location, cable and connector types, cable length, cable routing, and the type of platform. If these items are not specified and included as part of the equipment procurement, then the non-antenna interface pin transients presented in Section 2.4.3.2 shall be applied as the EMP suvivability criteria for the non-antenna interface pins.

The EMP induced current and voltage transients that would appear at the antenna interface pin depends on the type of antenna, the protective measures incorporated into the antenna, and the isolation provided by any additional equipment in the rf transmission path. Therefore, the antenna interface pin transients presented in Section 2.4.3.3 shall be applied as the EMP survivability criteria for the antenna interface pins.

2.4.3.2 Non-Antenna Interface Pin Transients

Critical equipment shall be designed to withstand the following maximum common mode current or voltage damped sinusoidal transients at each non-antenna interface pin for the interconnecting wiring between equipment or subsystems:

$$\left.\begin{aligned} &I_p(t) = \pm I_{max} e^{-\pi f t/Q} \sin(2\pi f t), \\ \text{or}\qquad & \\ &V_p(t) = Z\, I_p(t), \end{aligned}\right\} \tag{2.2}$$

where

$I_p(t)$ = pin current, amp,
$V_p(t)$ = pin to case voltage, volts,

f = test frequency, hertz,

t = time, seconds,

Q = decay factor $\equiv 16 \pm 4$,

Z = source impedance $\equiv$ 100 ohms.

I_{max} shall be shown as in Figure 2.5.

The verification of conformance to the above criteria shall be performed by tests specified in Section 10.3.2.2. The tests shall be performed for at least the injection frequencies of 0.5, 1, 2, 5, 10, 20, and 50 MHz. If the equipment has possible critical frequencies (e.g., cable resonant frequencies, clock frequencies, bandpass frequencies, etc.) additional testing at these frequencies shall be performed.

2.4.3.3 Unhardened Antenna Interface Pin Transients

Critical equipment shall be designed to withstand the following maximum common mode damped sinusoidal transient at each antenna interface pin:

$$\left.\begin{aligned} V_p(t) &= \pm V_{max} e^{-\pi ft/Q} \sin(2\pi ft) \\ I_p(t) &= V_p(t)/Z \end{aligned}\right\} \qquad (2.3)$$

where

$I_p(t)$ = common mode pin current in amps

$V_p(t)$ = pin to case voltage in volts

f = test frequency in hertz

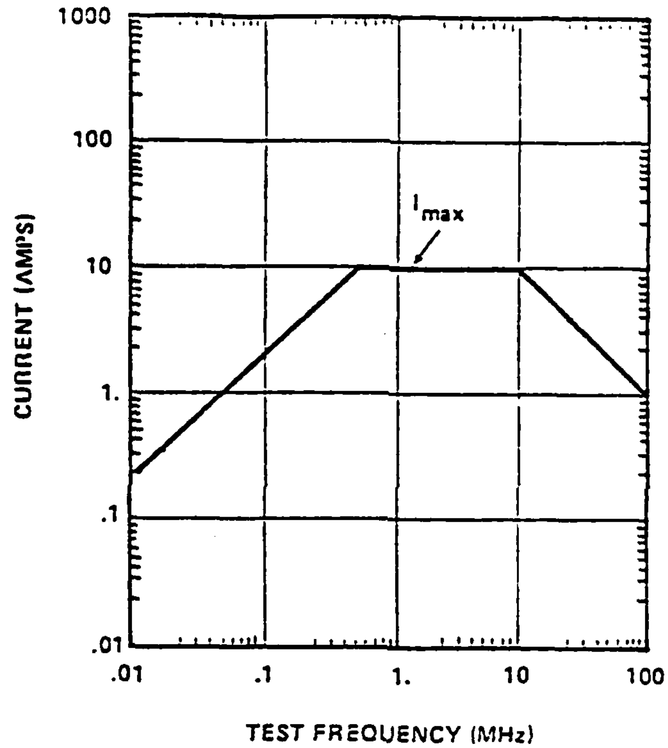
Q = decay factor $\equiv 16 \pm 4$

Z = 50 ohms

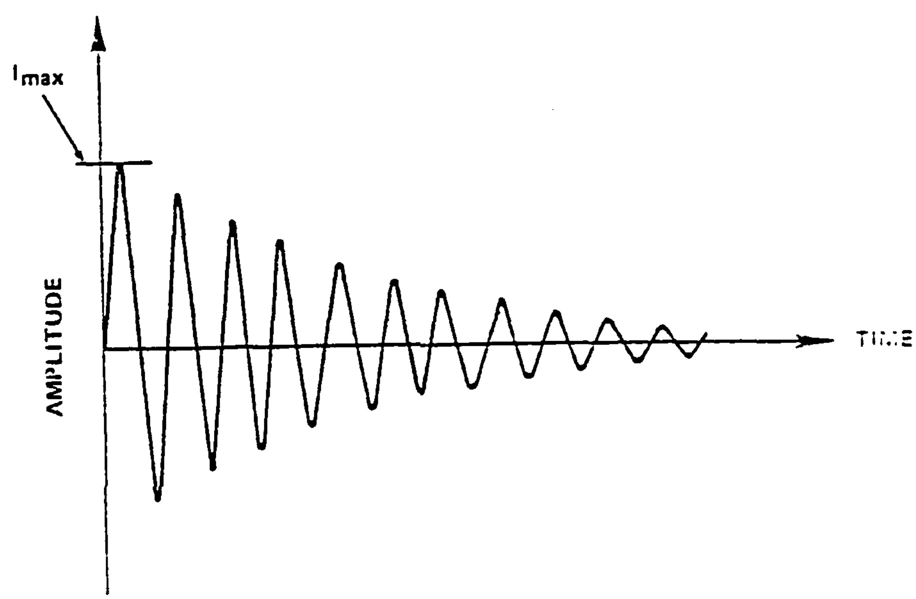
and V_{max} is the maximum pin voltage for each test frequency as shown in Figure 2.6.

HF antenna interface circuits shall use the maximum voltages labeled "HF Criteria" in Figure 2.6 while VHF and UHF antenna interface circuits shall use the "VHF/UHF Criteria" for the EMP hardening criteria.

The verification of conformance to the above criteria shall be performed by the tests specified in Section 10.3.3.1.



a. I_{max} as a Function of Frequency



b. Criteria Waveform

Figure 2.5 EMP Criteria Waveforms

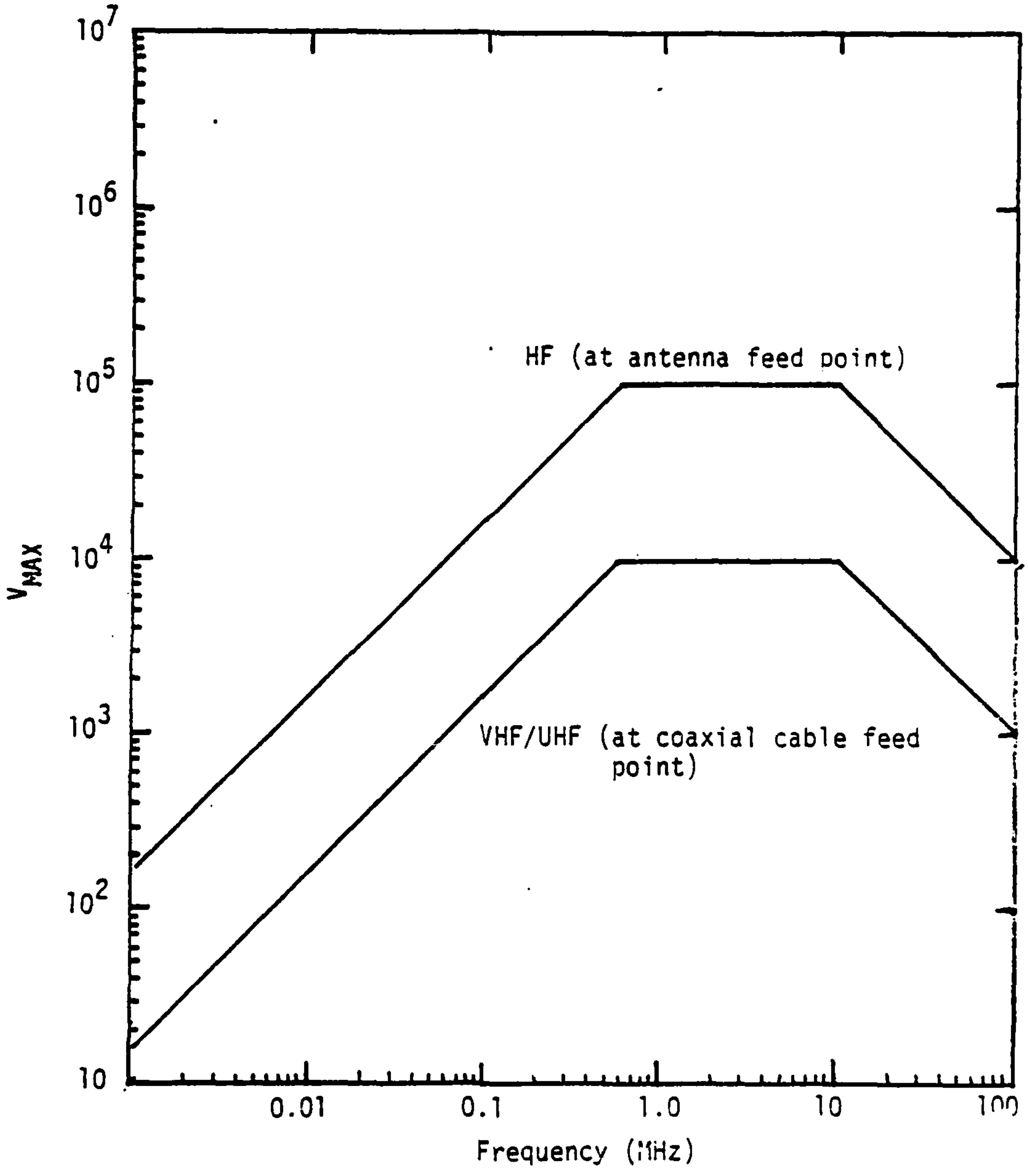


Figure 2.6 Criteria for Antennas

2.4.3.4 Hardened Antenna Interface Pin Transients

2.4.3.4.1 Hardened HF Antenna Pin Transients

Critical equipment shall be designed to survive the residual EMP transient developed by the hardened HF antenna system. This transient depends upon the effectiveness of the antenna protective device, therefore, the residual transient is the transient developed across the antenna protective device when it is subjected to antenna criteria presented in Section 2.4.3.3. The verification of conformance to the above criteria shall be performed by the tests specified in Section 10.3.3.2.1. The expected general characteristics of the residual transient has three stages which can deliver energy to the antenna interface pins. The first stage occurs before the antenna protective device fires and can be roughly characterized by a 10 to 20 nanosecond spike with an amplitude 3 times larger than the DC stand-off voltage of the protective device. The second stage occurs when the protective device is conducting and it acts as a source generator with a very low internal impedance. The third stage occurs after the damped sinusoid transient induced on the antenna decays in amplitude to the DC stand-off voltage of the protective device. At this point, the transient can be characterized as a damped sinusoid transient with the maximum amplitude equal to the DC stand-off voltage of the spark gap.

2.4.3.4.2 Hardened UHF/VHF Antenna Pin Transients

(To be determined)

2.4.4 Interface Cable Transients

2.4.4.1 Applicability

The EMP induced current and voltage transients that would appear on the interface cables are a function of the equipment location, cable and connector types, cable length, cable routing, and the type of platform (i.e. unhardened and hardened ship). If these items are specified and included as part of the equipment procurement, then the following appropriate cable transients can be applied as the EMP survivability criteria for the non-antenna interfaces and the equipment can be exempted from the above non-antenna interface pin transient criteria.

2.4.4.2 Unhardened Destroyer CLASS Ships

Exterior Cables - Critical equipment that is connected to exterior cables (i.e., a portion of its run above deck) shall be designed to withstand a maximum common mode cable current or voltage on each of these interface cables that is sixty (60) times greater than the above interface pin transients (see Table 2.1). Conformance to these criteria shall be verified by the tests specified in Chapter 10.

Interior Cables - Critical equipment that is connected to interior cables (i.e. its entire run below deck) shall be designed to withstand a maximum common mode cable current or voltage on each of these interface cables that is fifteen (15) times greater than the above interface pin transients (see Table 2.1). Conformance to these criteria shall be demonstrated by the tests specified in Chapter 10.

Table 2.1 Interface Cable Transients

Unhardened Destroyer CLASS Ships		Hardened Destroyer CLASS Ships	
Exterior Cables	Interior Cables	Exterior Cables	Interior Cables
$I_C(t)=60xI_p(t)$	$I_C(t)=15xI_p(t)$	$I_{CE}(t)=60xI_p(t)$	$I_C(t)=I_p(t)$
		$I_{CI}(t)=I_p(t)$	
$V_C(t)=60xV_p(t)$	$V_C(t)=15xV_p(t)$	$V_{CE}(t)=60xV_p(t)$	$V_C(t)=V_p(t)$
		$V_{CI}(t)=V_p(t)$	

$I_C(t)$=Common mode cable current (i.e., cable to case)

$I_{CE}(t)$=Common mode cable current on exterior (i.e., unprotected) portion of the cable run

$I_{CI}(t)$=Common mode cable current on interior (i.e., protected) portion of the cable run

$V_C(t)$=Common mode cable voltage (i.e., cable to case)

$V_{CE}(t)$-Common mode cable voltage on exterior (i.e., unprotected) portion of the cable run

$V_{CI}(t)$=Common mode cable voltage on interior (i.e., protected) portion of the cable run

2.4.4.3 Hardened Destroyer CLASS Ships

Exterior Cables - Critical equipment that is connected to exterior cables (i.e., a portion of its run outside the protection envelope) shall be designed to withstand a maximum common mode cable current or voltage on the exposed portion of each of these interface cables that is sixty (60) times greater than the interface pin transients (see Table 2.1). In addition, the equipment shall be designed to withstand the interior cable transients specified in the next paragraph, on the protected portion of each of these interface cables (i.e., that portion of the cable run that is within the protection envelope). Conformance to this criteria shall be verified by the tests specified in Chapter 10.

Interior Cables - Critical equipment that is connected to interior cables (i.e., its entire run within the protection envelope) shall be designed to withstand a maximum common mode cable current or voltage on each of these interface cables that is equal to the above interface pin transients (see Table 2.1). Conformance to these criteria shall be demonstrated by the tests specified in Chapter 10.

2.4.5 Electromagnetic Field Transients

Critical equipment shall be designed to survive the transient electromagnetic field produced by the EMP (i.e. the electromagnetic field criteria). The electromagnetic field criteria which apply to the equipment are specified according to equipment location.

2.4.5.1 Exterior Spaces

Critical equipment to be located in an exterior space shall be designed to withstand direct exposure to the high altitude burst EMP environment defined as,

$$\left.\begin{aligned} E(t) &= E_0(e^{-\alpha t} - e^{-\beta t}), \\ &\text{and} \\ H(t) &= \frac{E(t)}{z_0}, \end{aligned}\right\} \qquad (2.4)$$

where:

$E(t)$ = electric field, volts/meter,

$H(t)$ = magnetic field, amps/meter

E_0 = 5.25 x 10^4 volts/meter,

α = 4.0 x 10^6 second,

β = 4.76 x 10^8 second, and

z_0 = 377 ohms.

2.4.5.2 Interior Spaces

Critical equipment located in interior spaces shall be designed to survive the electromagnetic fields produced by a source cable located one (1) meter away carrying the cable transients specified in Table 2.1. Conformance to these criteria shall be demonstrated by the tests specified in Section 10.3.4.

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CHAPTER 3

VOLUME SHIELDING

3.0 Executive Summary

Chapter 3 discusses techniques for shielding circuitry using metal enclosures. Metal enclosures protect the sensitive circuit components by reflecting and attenuating most of the EMP fields. Within the contents of this chapter, it is demonstrated that equipment enclosures of moderate thickness ($\sim$1/8") in which care has been taken in the treatment of openings (apertures, seams, etc.) can protect the most sensitive circuit components from the environments specified in Section 2.4.

3.1 Introduction

The objective of this chapter is to present hardening techniques for shielding volumes such as rooms, cabinets, equipment racks, and other enclosures. Consequently, the various ways that electromagnetic (EM) energy can penetrate into these enclosures will be introduced and discussed. Data on and methods for calculating the resulting internal field, current, voltage, power, and energy levels will be presented and illustrated with example problems.

Section 3.2 will discuss direct penetration through shielding barriers (diffusion) where the EM energy penetrates lossy structures even in the absence of imperfections such as seams, holes, and cable entries. The penetration of plane sheets and canonically shaped objects (spheres, cylinders, etc.) as well as ordinary non-canonically shaped objects will be considered and illustrated. Since the enclosures considered here cannot realistically be manufactured out of a single monolithic piece of metal but rather must be constructed from a number of flat sheets which are bonded together in some fashion (welded, bolted, gasketed, riveted, etc.), the possibility of EM leakage at such weak spots must be considered along with other modifications to the surface such as fasteners. Consequently, EM penetration of seams and gaskets is discussed and illustrated in Section 3.3. In addition to seams and gasketed joints, for example, actual enclosures also often require openings to facilitate access, viewing, natural lighting, and ventilation. Section 3.4 provides the guidelines necessary for specifying and/or treating such openings (apertures), while Section 3.5 discusses the use of materials such as metal honeycomb panels or wire mesh (screen) to provide additional hardening. Finally, in Section 3.6, techniques involving the use of "waveguides below cutoff" will be described, discussed, and illustrated. Such short waveguides, attached to entry holes in an enclosure and extending out or into the interior of the enclosure, can sometimes be used to attenuate the fields which would otherwise enter the enclosure through the holes. Metal honeycomb panels are a variation of the "waveguide below cutoff" technique where a large number of such waveguides are arrayed side-by-side in a two-dimensional configuration, and where, therefore, slightly different techniques must be employed (see Section 3.5).

To be able to adequately evaluate the ability of mission critical equipment to function without failure (that is, without the loss, degradation, or malfunction that would affect the overall system performance and mission success or safety) in the EMP environment, not only do the effects of exterior

(HEMP or high altitude burst EMP) field but also those of interior (cable propagated) fields need to be considered. Consequently, three EMP environments will be considered here. The first is the standard exterior HEMP plane wave defined by the electric field in paragraph 2.4.5.1. The second is the interior electromagnetic field produced by the configuration shown in Figure 3.1 where the wire is driven by a current source providing the damped sinusoidal waveform given in paragraph 2.4.3.2 with $I_{max} = 10$ A. The third environment consists of the same damped sinusoidal current waveform described above directly injected onto the enclosure. The test frequencies are 0.5 MHz, 2.0 MHz, and 10 MHz. The current will be injected onto the enclosure 0.5 ft from the edge of the seam, aperture, air vent, or cutoff waveguide in an attempt to model worst case responses. In the case of diffusion, the current will be injected, in turn, in the center of each face of the enclosure, and the worst-case results reported.

Each of the sections discussed above will begin with a subsection outlining the background of the topic of the section. This will then be followed by one subsection for each of the EMP environments previously specified. Each of these latter sections will present data on and methods for calculating the resulting internal field, current, voltage, power, and energy levels, as well as illustrate the application of these methods with examples.

3.2 Direct Penetration Through Shielding Barriers (Diffusion)

3.2.1 Background

Shielding Effectiveness. In order to protect electronic circuits and components from the harmful effects of EMP, they are usually placed within a metal enclosure such as an equipment rack and/or a rack mounted equipment cabinet. In order to be able to determine the effectiveness of such a procedure or the relative effectiveness of several such procedures, some measure of shielding effectiveness must be available. The common definition of shielding effectiveness (SE) is that given by Reference 3.1.

$$SE = \text{Attenuation (dB)} = 20 \log_{10} (E_i/E_t). \qquad (3.1)$$

where E_i is the incident electrical field on the outside of the enclosure, while E_t is the electric field transmitted to the inside of the enclosure. A similar definition, of course, can be formulated for the magnetic field also. Further elaboration upon shielding effectiveness and its relation to MIL-STD-285 measurements can be found in References 3.1 and 3.2.

Schelkunoff Theory. The problem of determining the shielding efficiency of various enclosures has a long history, as the first such paper on the subject appears to be that by J. Larmor in the January 1884 issue of the Philosophical Magazine. Three basic approaches have been developed over the years. The first approach is to solve the field theory problem by solving Maxwell's equations with appropriate boundary conditions. The second is the circuit theory approach [3.3, 3.4] where the enclosure is viewed as an antenna - a fat dipole in the electric field case and a short-circuited loop in the magnetic field case. The third is the transmission line approach of Schelkunoff [3.5], and it is this method that is described here.

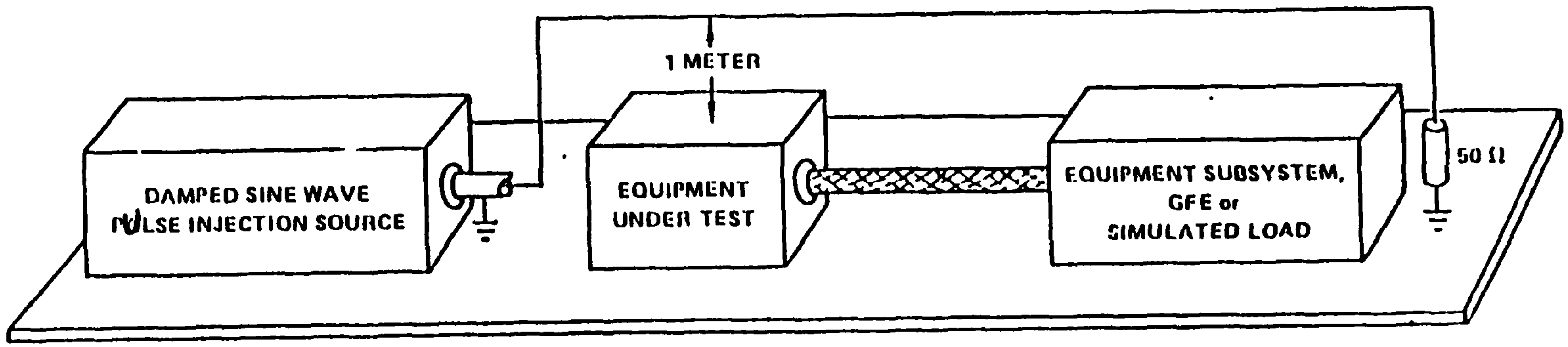


Figure 3.1 Test Configuration for "Interior Fields"

The shielding effectiveness (SE) of a continuous imperfectly conducting plane sheet was given by Schelkunoff [3.5]

$$
\left.
\begin{aligned}
SE &= R + A + B, \\
&\text{where} \\
R &= 20 \log_{10} \left(|k+1|^2 / 4|k| \right), \\
A &= 20 \log_{10} (e)\, \alpha t, \\
B &= 20 \log_{10} \left| 1 - \frac{(k-1)^2}{(k+1)^2} e^{-2(1+i)\alpha t} \right| \\
k &= \frac{Z_{wave}}{Z_{shield}}, \\
\alpha &= (\pi \mu \sigma f)^{1/2} = 1/\delta, \\
Z_{shield} &= \left(\frac{2\pi\mu f}{\sigma} \right)^{1/2}, \\
Z_{wave} &= \text{the wave impedance,}
\end{aligned}
\right\} \quad (3.2)
$$

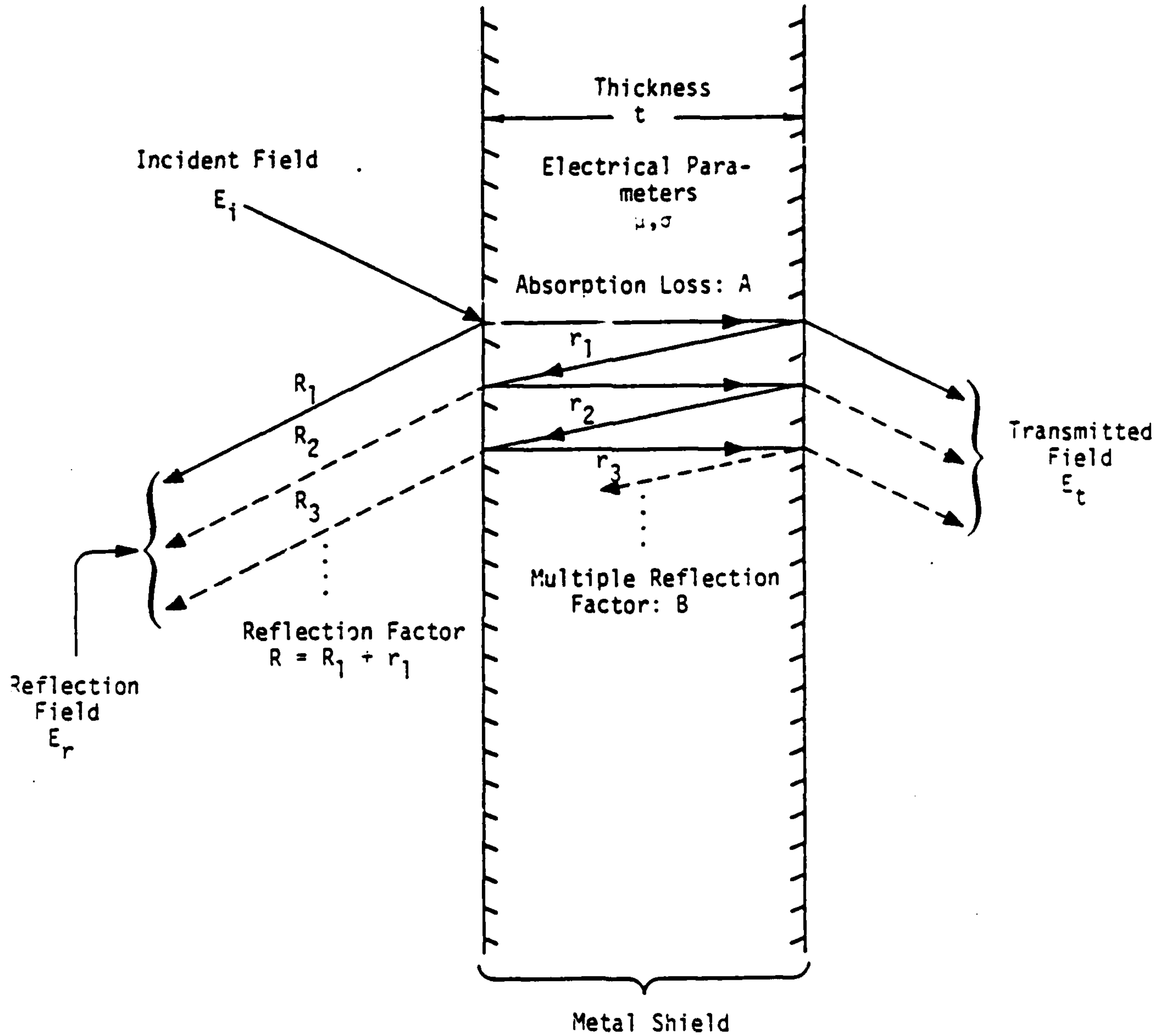
and where f is the frequency, t, μ, and σ are the thickness, permeability, and conductivity of the shield, respectively, δ is the skin depth, and e is the base of the natural (Naperian) logarithms. In (3.2) R represents the losses due to the first reflection at each surface of the metal shield, while A represents the absorption loss in the shield. B, on the other hand, represents the effects of multiple reflections in the metal shield. This is all illustrated in Figure 3.2. In order to evaluate (3.2), one needs to also know the wave impedance Z_{wave}. For a plane wave in free space, the wave impedance is given by

$$Z_{wave} = Z_p = \frac{\mu_0}{\epsilon_0} = 120\,\pi\,\Omega \doteq 377\,\Omega. \qquad (3.3)$$

Close to a short electric dipole, however, the wave impedance is approximately given by

$$Z_{wave} = Z_E = -j\, 7.1 \times 10^{-7}/fr\ \Omega, \qquad (3.4)$$

where f is the frequency in Hz and r is the distance from the dipole in inches. This is called the electric of high-impedance field, and the impedance is inversely proportional to the relative permittivity. The field close to and parallel to a small loop is called the magnetic or low-impedance field, and its wave impedance is given by [3.6]:



$$SE = 20 \log_{10} (E_i/E_t) \doteq (R_1 + r_1) + A + B = R + A + B$$

Figure 3.2 Schelkunoff Shielding Effectiveness

$$Z_{wave} = Z_M = j\ 2 \times 10^{-7}/fr\ \Omega. \tag{3.5}$$

Substituting (3.3) through (3.5) into (3.2), then yields the following expressions for the "reflection term" R [3.6, 3.7]:

$$R_P = 168 - 10 \log_{10} \left[\frac{\mu_r f}{g}\right] \text{dB},$$

$$R_E = 354 - 10 \log_{10} \left[\frac{\mu_r f^3}{g} \ r^2\right] \text{dB}, \tag{3.6}$$

$$R_M = 20 \log_{10} \left[\frac{0.462}{r}\sqrt{\frac{\mu_r}{f\ g}} + 0.136r\sqrt{\frac{f\ g}{\mu_r}} + 0.354\right] \text{dB}$$

where

μ/μ_0 = the permeability of the shield relative to free space ($\mu_0 = 4\pi \times 10^{-7}$; see Table 3.1),

$g = \sigma/\sigma_c$ = the conductivity of the shield relative to copper ($\sigma_c = 5.8 \times 10^7$ mhos/m; (see Table 3.1),

f = the frequency in Hz,

r = *the distance from the source to shield in inches.*

Similarly, expressing the "absorption term" A yields [3.7]:

$$A = 20 \log_{10} (e) \sqrt{23.2}\ \ 0.0254\ \pi\ (\mu_r\ \sigma_r\ \ldots)^{1/2}$$
$$\cong 3.338\ (\mu_r\ \sigma_r\ f)^{1/2} \quad \text{dB}, \tag{3.7}$$

while the "multiple reflection term" B can be expressed as [3.7]:

$$B = 20 \log_{10} \left[1 - x \cdot 10^{-A/10} \left\{\cos \left(A.10 \cdot \log_{10}(e)\right) - j \ \text{Sin} \left(A/10 \cdot \log_{10}(e)\right)\right\}\right]$$
$$\cong 20 \log_{10} \left[1 - x \cdot 10^{-A/10} \left\{\cos\ (0.230A) - j\ \text{Sin}(0.230\ A)\right\}\right] \text{dB},$$

where (3.8)

$$x = \frac{4(1-m^2)^2 - 2m^2 - j\ 2\sqrt{2}\ m\ (1 + m^2)}{\left[1 + (\ 1 + \sqrt{2}\ m)^2\right]^2}$$

and where

$$k = m = 0.766 \sqrt{\frac{f\ g}{\mu_r}}\ \ r = \frac{1}{K}$$

is the ratio of the incident magnetic field impedance (Z_{wave}) to the shield impedance (Z_{shield}).

It should be noted again that μ_r is the permeability of the shield relative to that of free space while g is the conductivity relative to that of copper. Typical values of g and μ_r (at 150 kHz) can be found in Table 3.1, while plots of R can be found in Figures 3.3, 3.4, and 3.5. Similarly, (3.7) and (3.8) for A and A + B (with x = 1) are plotted in Figure 3.6. It should also be noted that x is real and nearly equal to 1 except in the case of low-frequency shielding of magnetic fields, as is illustrated in Figure 3.7. From Table 3.1 and either (3.2), (3.6), (3.7), and (3.8), or from Figures 3.2 through 3.6, one can determine the amount of shielding (dB) obtained from a metal sheet of given thickness, conductivity and permeability, or alternately one can determine the required thickness for a specified level of shielding. An alternate method of solution is provided in Figures 3.8 through 3.13 where (3.6), (3.7), and (3.8) have been put in nomographic form. Sample calculations have been illustrated in Figures 3.10 through 3.12. To use the nomograms, one proceeds as follows:

1. Enter points (1), (2), and (3) on the r (or t), g/μ_r, and f scales, respectively, on each nomogram;
2. Connect points (1), (2) with a straight line to determine point (4);
3. Connect points (3) and (4) with a straight line to determine point (5);
4. Read the desired value (R, A, or K_ω) at point (5).

Now the value of K_ω and A are used in Figure 3.13 to determine the value of B, and finally the values of R, A, and B so determined are added per (3.4) to obtain the desired value of SE. One should also note that the values of μ_r used in Table 3.1 and in Figures 3.8 through 3.12 are for low frequencies (150 kHz), and that as the frequency increases, the effective value of μ_r will decrease. Consequently, appropriate adjustments must be made in the values of μ_r which are used. For example, the value of μ_r for iron given (at 150 kHz) in Table 3.1 is 1000. This value is good for frequencies lower than 150 kHz, but at higher frequencies it varies as shown in Table 3.2.

Table 3.2 The Frequency Dependence of μ_r for Iron

f:	<150 kHz	1 MHz	3 MHz	10 MHz	15 MHz	100 MHz	1000 MHz	1500 MHz	10,000 MHz
μ_r	1000	700	600	508	400	100	50	10	1

Copper and aluminum, on the other hand, have a value of μ_r of 1 which is good over the entire frequency range from DC to 10,000 MHz.

The preceding method for calculating shielding effectiveness, strictly speaking, only applies to an infinite flat plate of thickness t, and, in addition, only then in the frequency domain. However, it does allow such calculations for arbitrary wave impedances. Because of this, it may also be used in some cases for estimating the shielding effectiveness of enclosures. Lee and Bedrosian [3.8] point out, however, that this can greatly overestimate the shielding

Table 3.1 Electrical Parameters and Absorption Loss of Metals at 150 kHz [3.7]

Metal	g Relative Conductivity	μ Relative Permeability (at 150 kHz)	A/t Absorption Loss (at 150 kHz, dB/mil)
Silver	1.05	1	1.32
Copper, annealed	1.00	1	1.29
Copper, hard drawn	0.97	1	1.26
Gold	0.70	1	1.08
Aluminum	0.61	1	1.01
Magnesium	0.38	1	0.79
Zinc	0.29	1	0.70
Brass	0.26	1	0.66
Cadmium	0.23	1	0.62
Nickel	0.20	1	0.58
Phosphor-bronze	0.18	1	0.55
Iron	0.17	1000	16.9
Tin	0.15	1	0.50
Steel, SAE 1045	0.10	1000	12.9
Beryllium	0.10	1	0.41
Lead	0.08	1	0.36
Hypernick	0.06	80,000	88.5*
Monel	0.04	1	0.26
Mu-Metal	0.03	80,000	63.2*
Permalloy	0.03	80,000	63.2*
Stainless steel	0.02	1000	5.7

*Obtainable only if the incident field does not saturate the metal

[Note: $\sigma_{copper} = 5.8 \times 10^7$ mhos/meter
$\mu_{copper} = \mu_o = 4\pi \times 10^{-7}$]

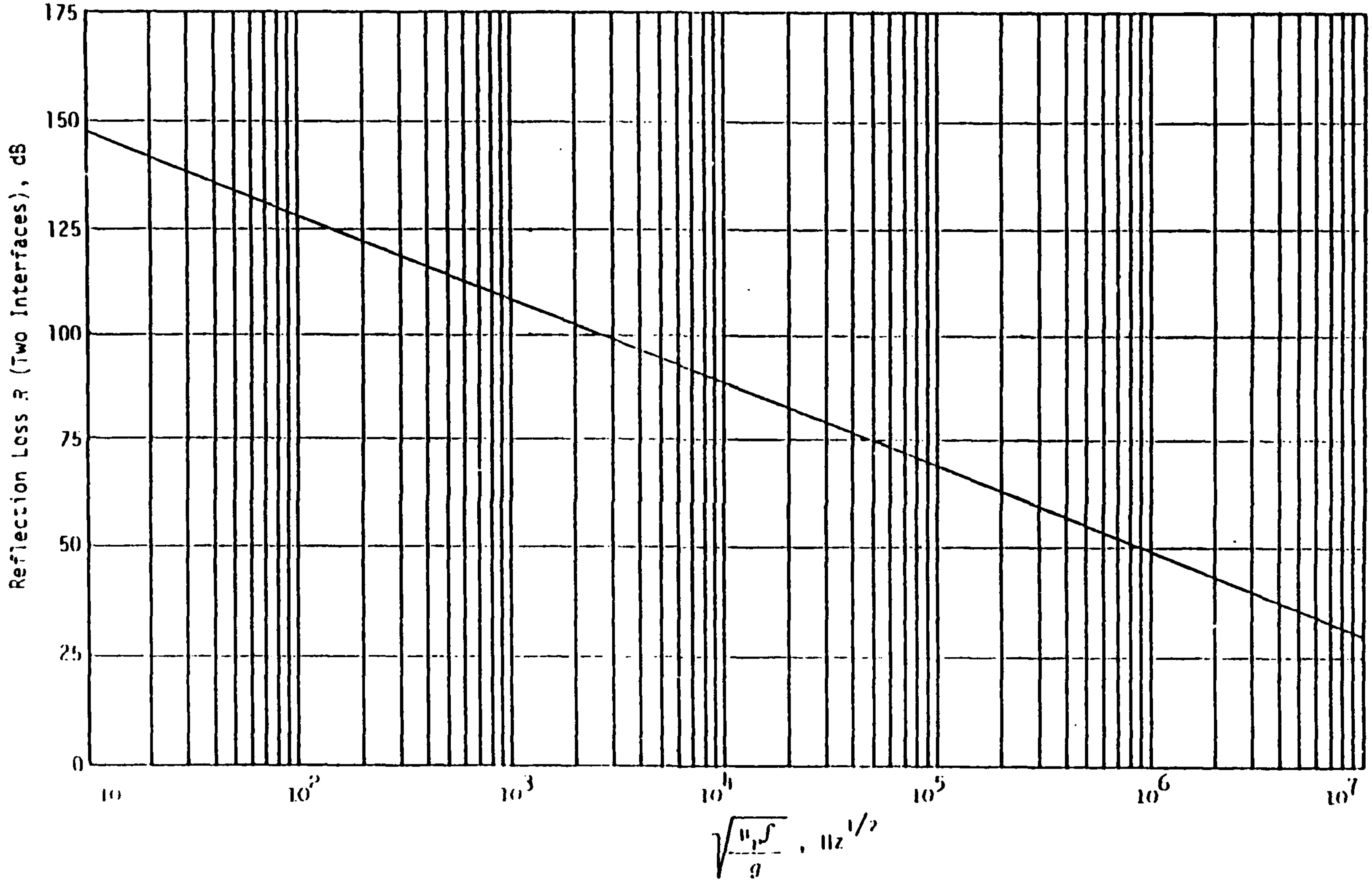


Figure 3.3 Reflection Loss for a Plane-Wave (R_p) [3.7]

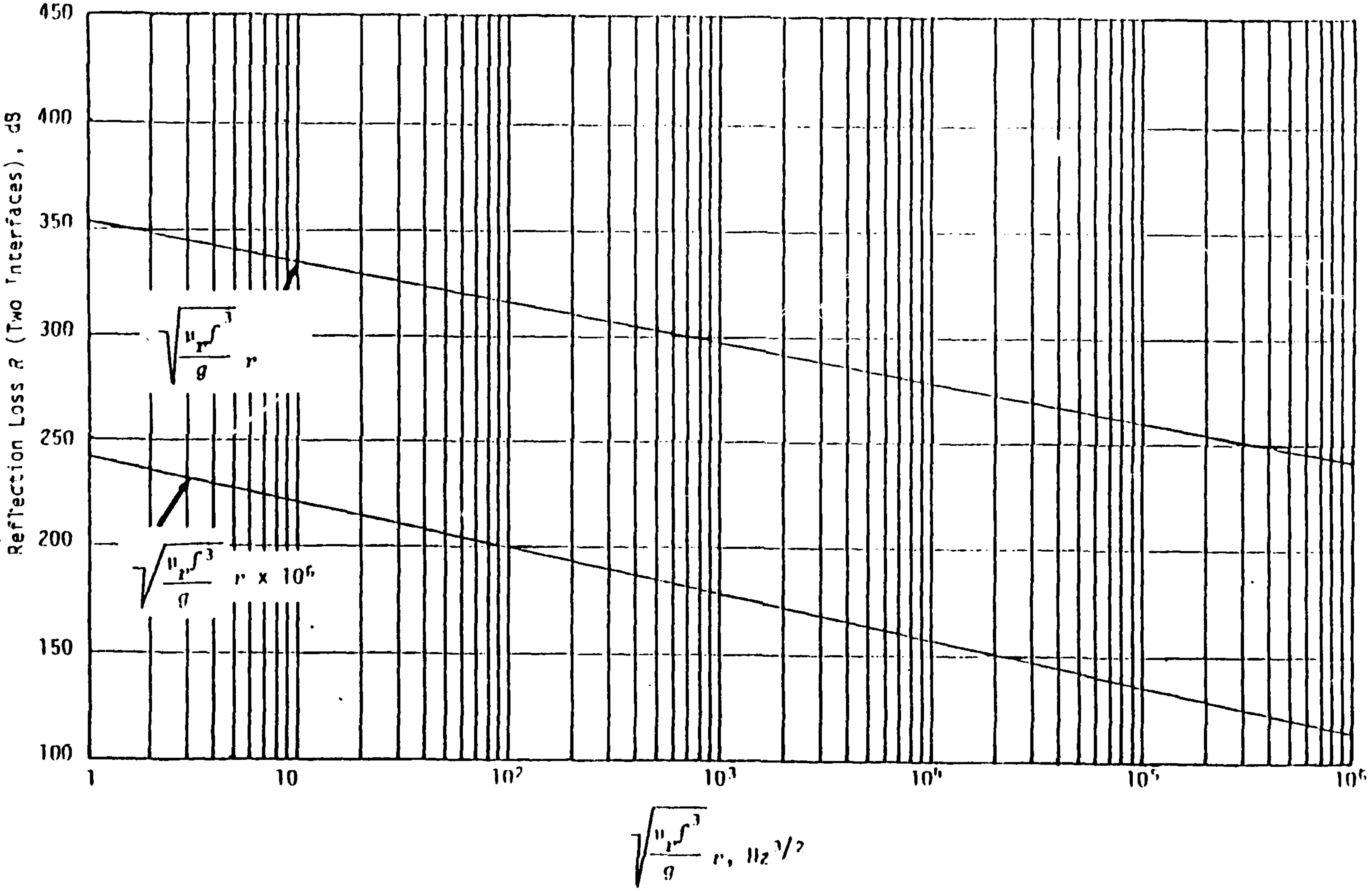


Figure 3.4 Reflection Loss for a High-Impedance Source (R_E) [3.7]

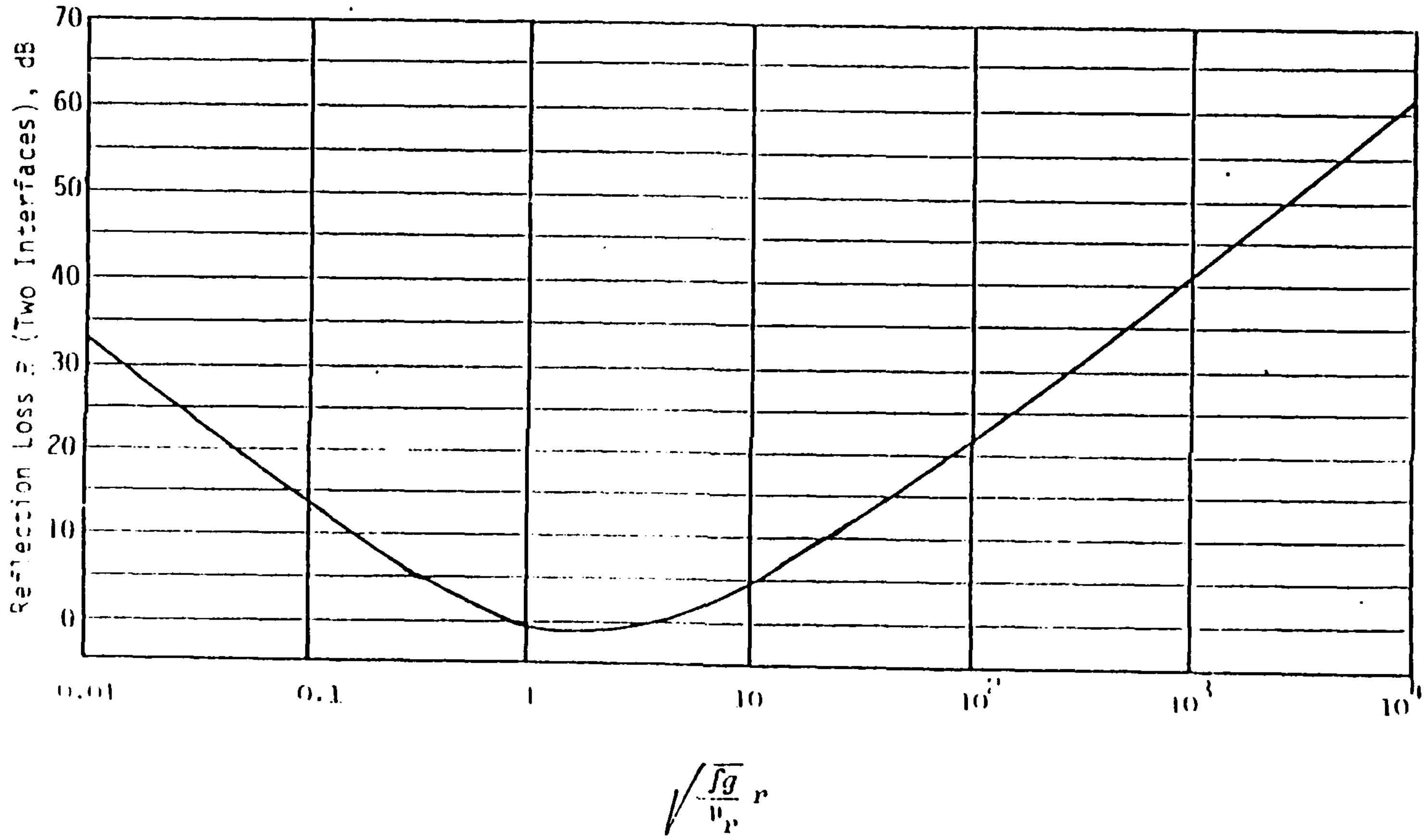


Figure 3.5 Reflection Loss for a Low Impedance Source (R_M) [3.7]

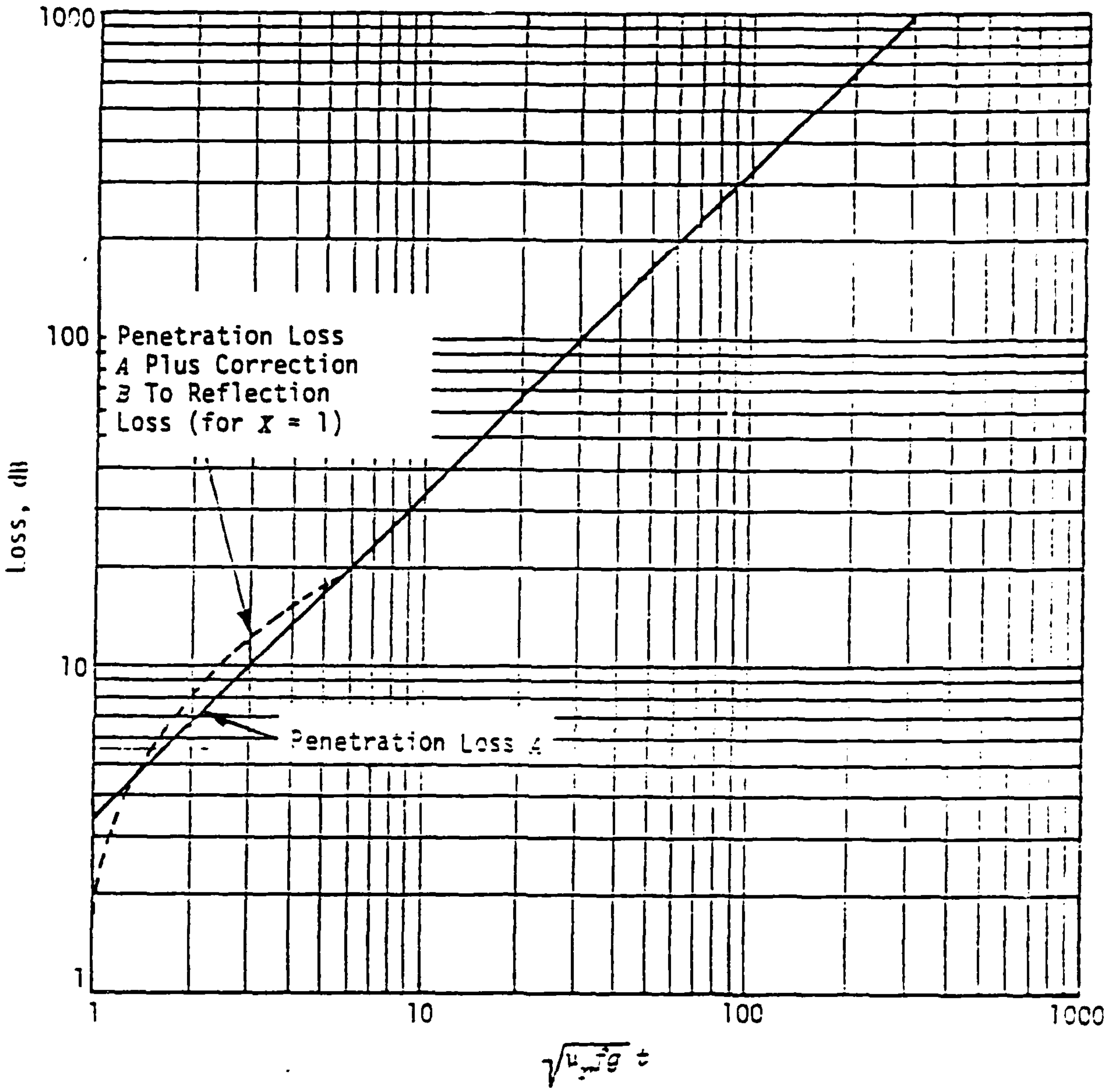


Figure 3.6 Absorption-Loss Curves (A, A+B), [3.7]

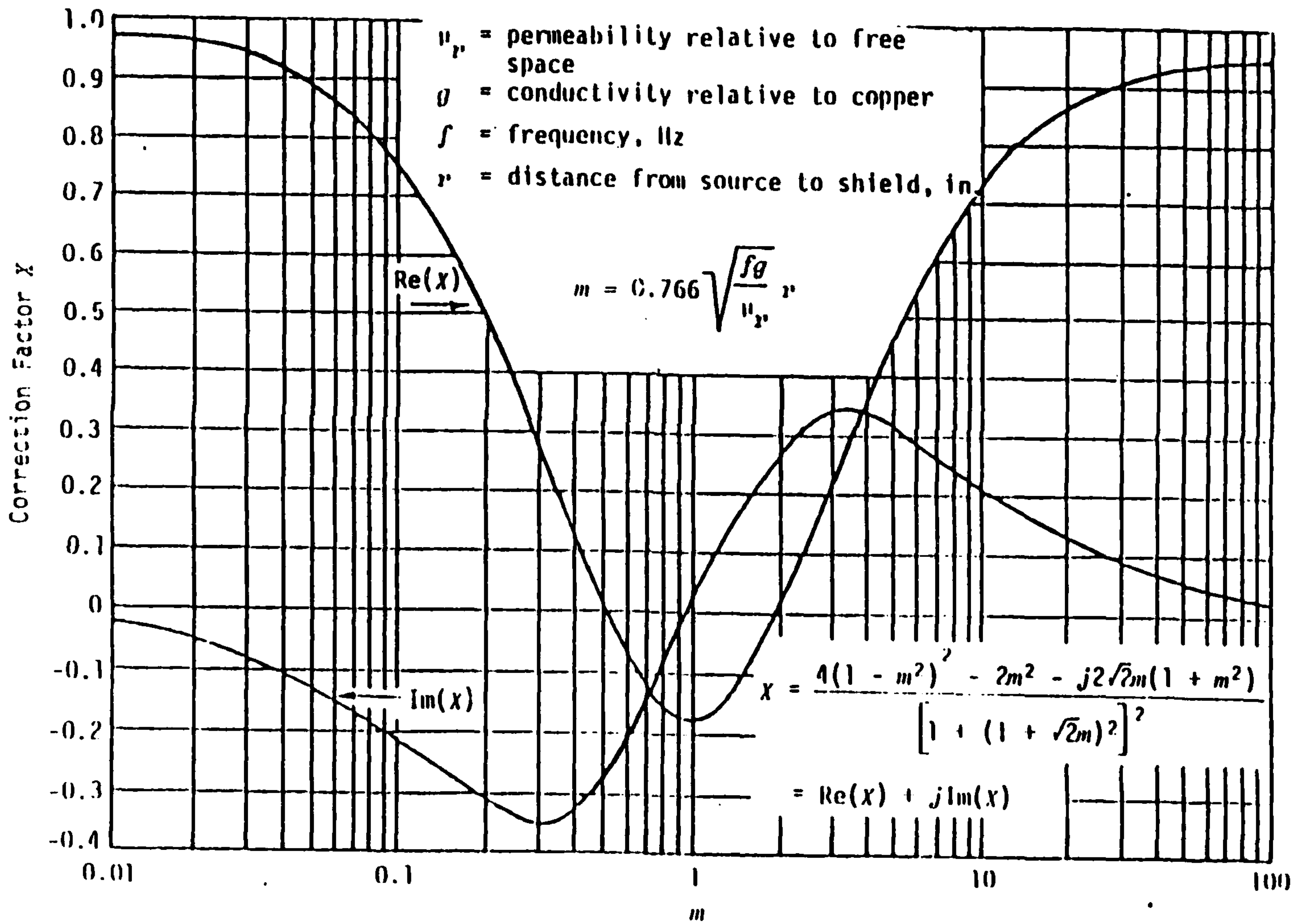


Figure 3.7 Correction Factor in Correction Term Having Internal Reflections (x) [3.7]

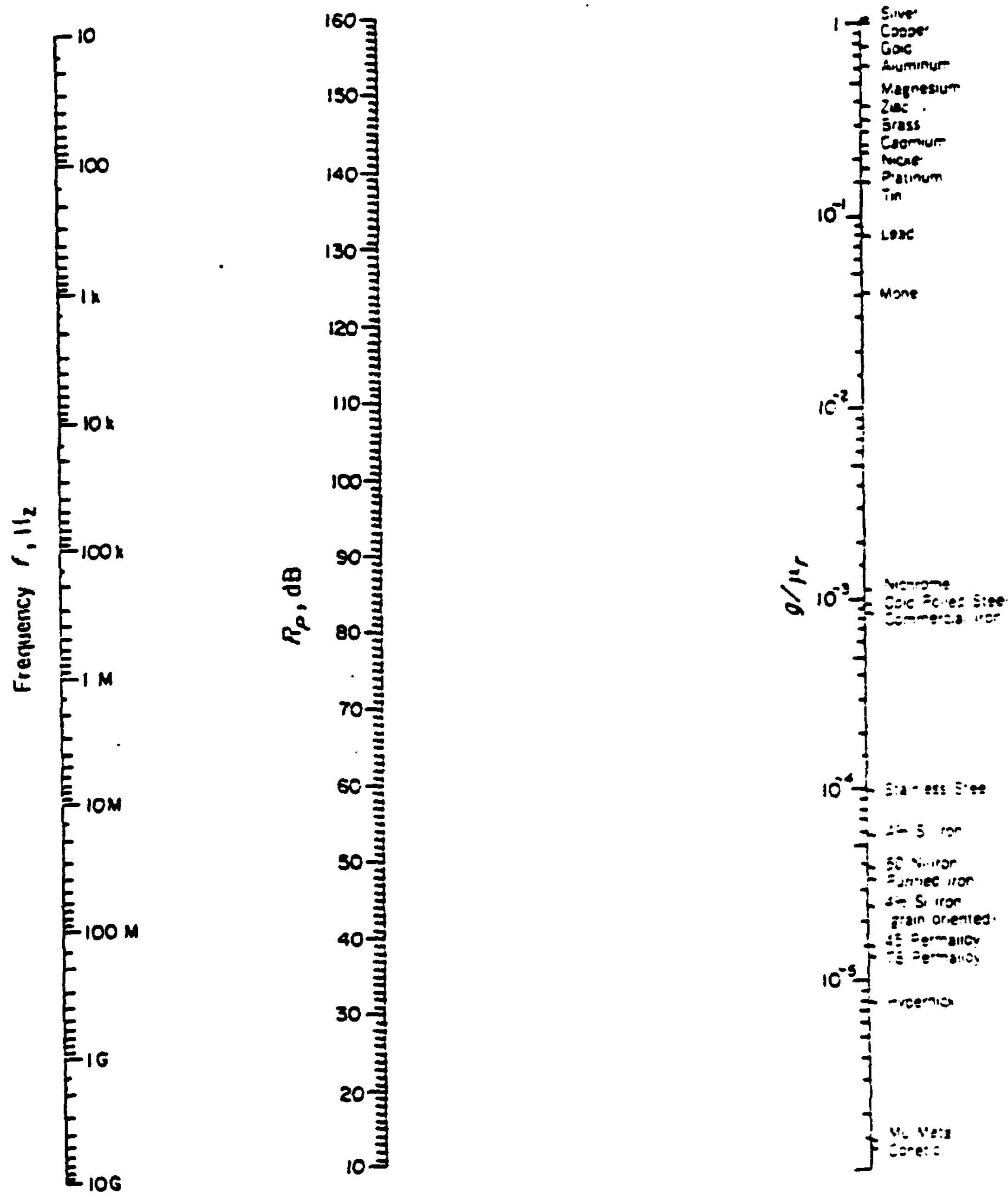


Figure 3.8 Plane Wave Reflection Loss R_p [3.7]

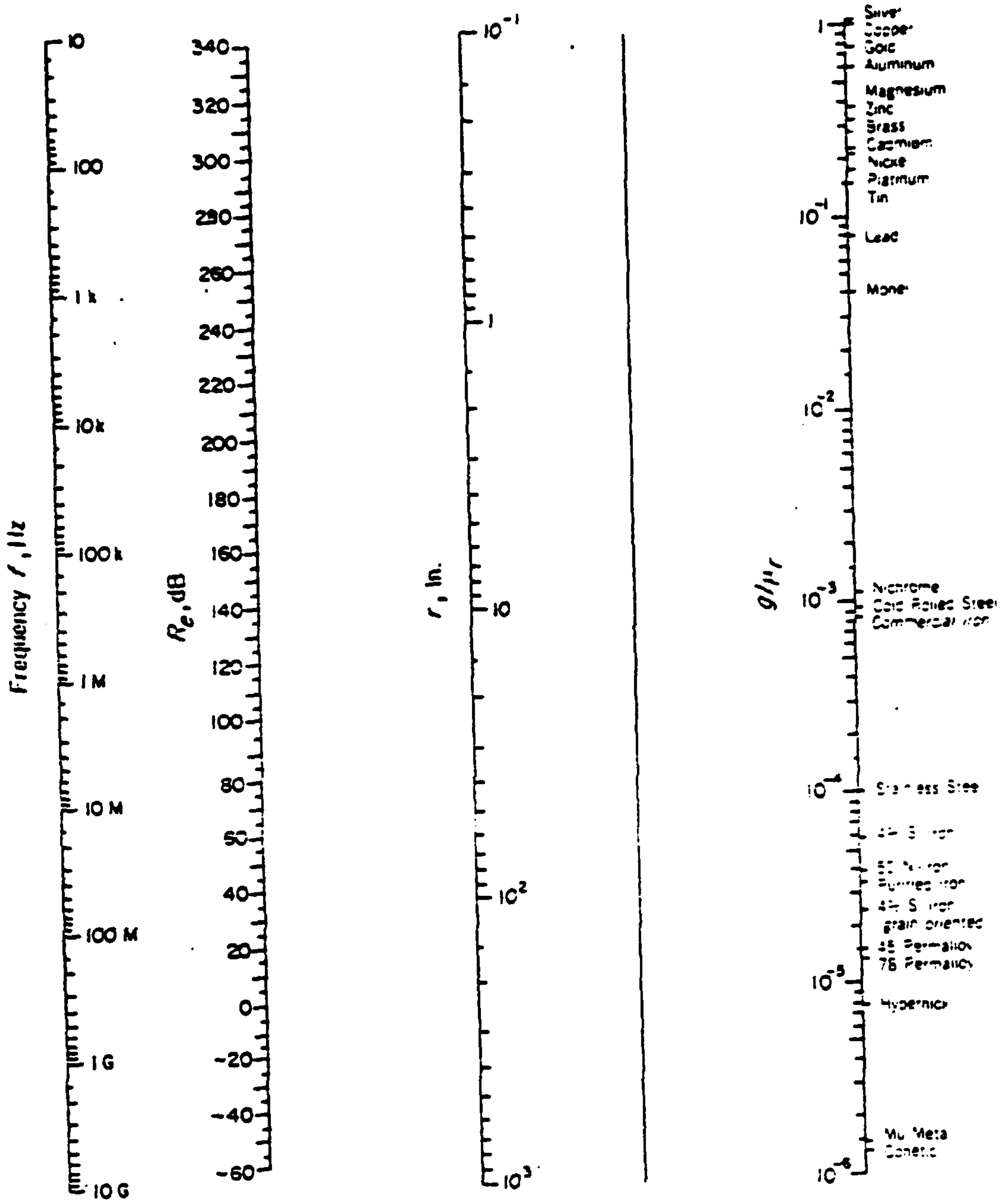


Figure 3.9 Electric Field Reflection Loss R_E [3.7]

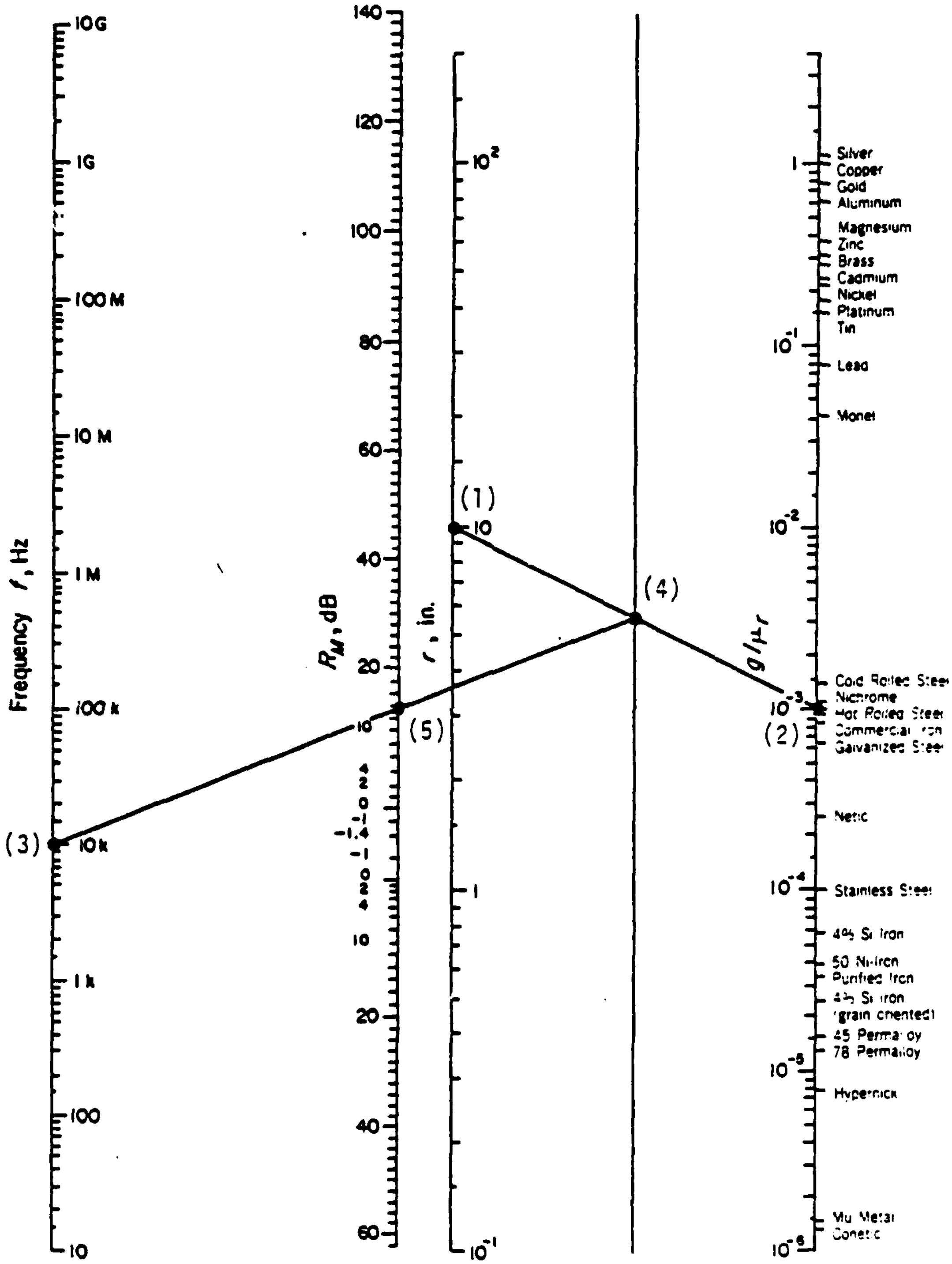


Figure 3.10 Magnetic Field Reflection Loss R_M [3.7]

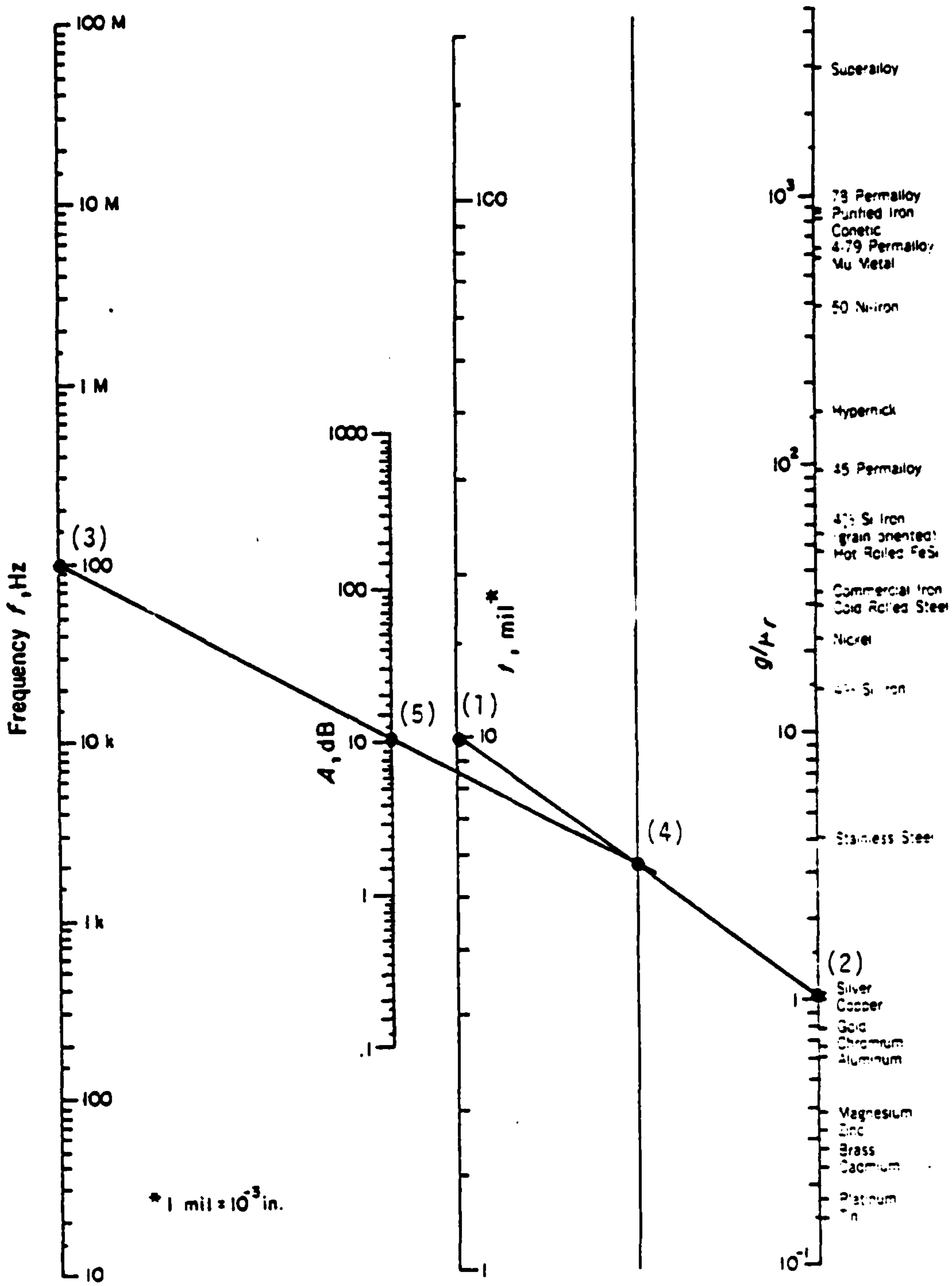


Figure 3.11 Absorption Loss A [3.7]

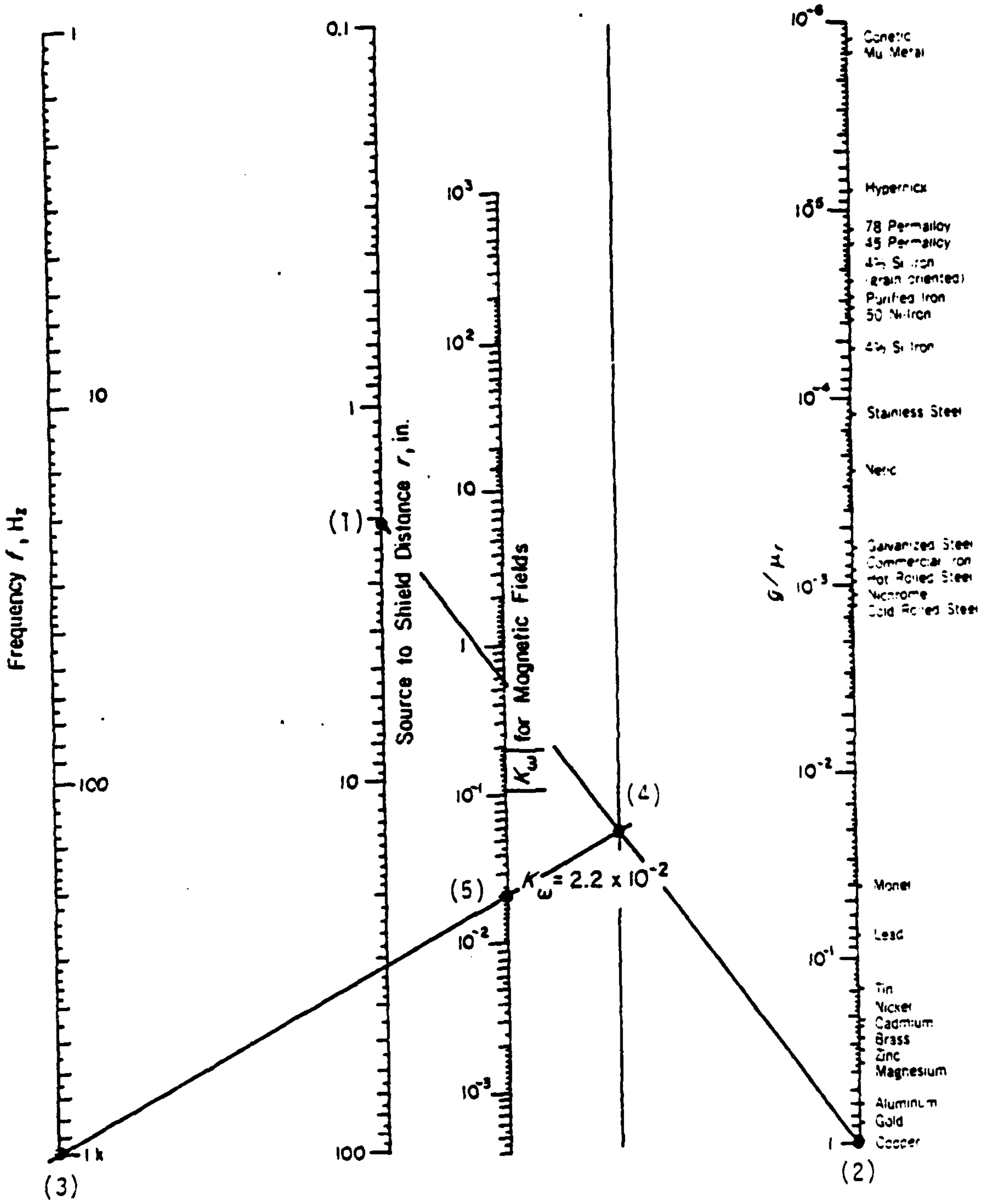


Figure 3.12 Chart for Computing K for Magnetic Field Secondary Reflection Loss [3.7]

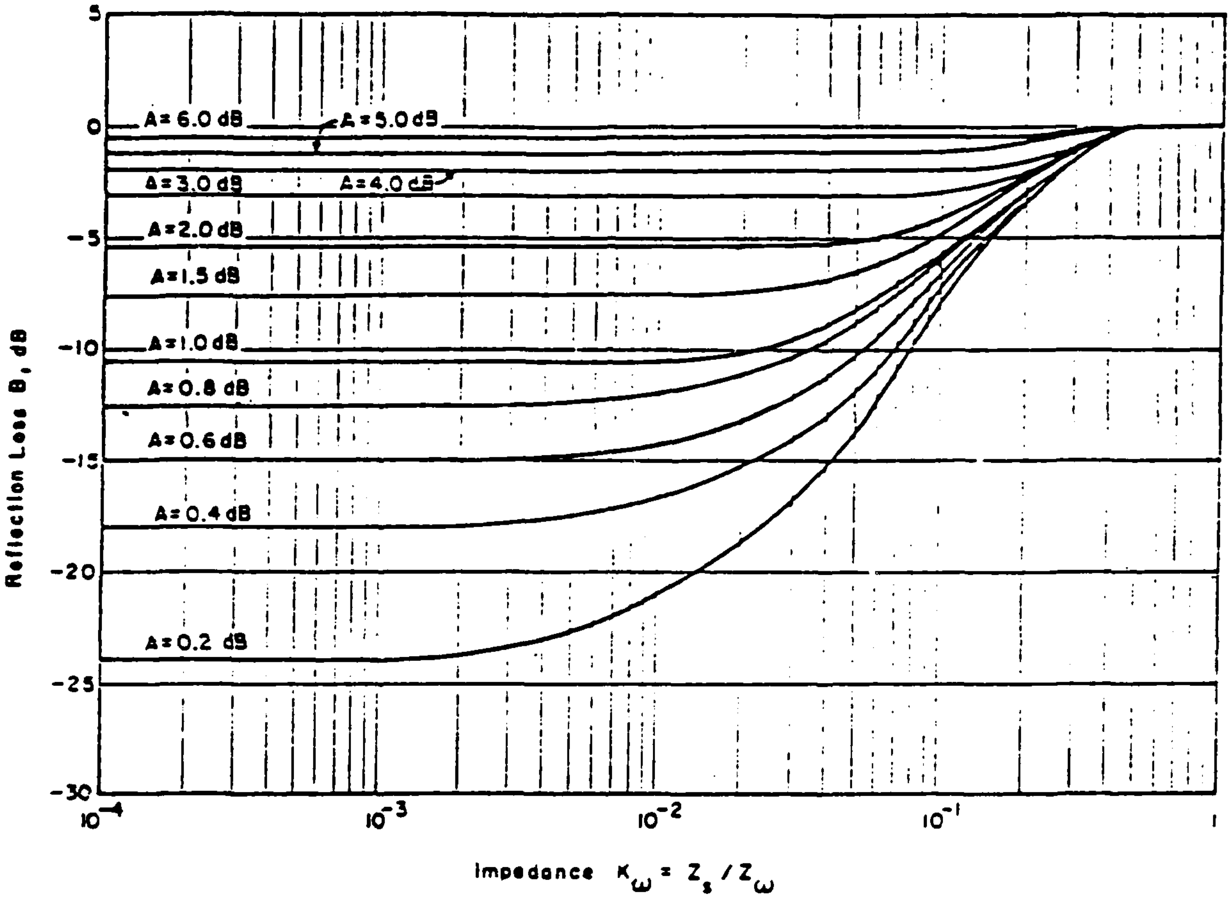


Figure 3.13 Chart for Computing Secondary Losses for Magnetic Fields (B) [3.7]

effectiveness of the enclosure at low frequencies. For example, test data obtained for shielding effectiveness of enclosures obtained by MIL-STD-285 may be related to other cases (plane wave, for example) by the methods described in Reference 3.1.

Canonically Shaped Enclosures. In this section simple formulae are given, both in the frequency domain and in the time domain, for the shielding effectiveness of various simply-shaped enclosures. Because the electric field is strongly attenuated at both high and low frequencies by the mechanism of reflection and absorption, and because at high frequencies, where the wall thickness of the enclosure is larger than the skin depth, the magnetic field is similarly attenuated, consideration is directed here to the low-frequency magnetic field.

The difference between four simple canonical shapes are discussed in both the frequency and the time domains. These are: a single infinite flat plate, two infinite flat parallel plates, an infinite circular cylindrical shell, and a spherical shell. By considering Maxwell's equations, the usual boundary conditions, and the standard (scalar) constitutive relations, the shielding effectiveness can be written in the frequency domain as [3.8 - 3.10]:

$$SE = 20 \log_{10} (|T_m|) \quad dB, \tag{3.9a}$$

where

$$T_m(s) = \frac{H_t(s)}{H_i(s)} = \frac{1}{\cosh(p)+(\xi_1 p+\xi_2/p) \sinh(p)}, \tag{3.9b}$$

and where

$$\left.\begin{aligned}
H_i(s) &= \text{the incident magnetic field,} \\
H_t(s) &= \text{the internal (transmitted) magnetic field,} \\
p &= \sqrt{s\tau_d}, \\
\tau_d &= t_\Delta = \mu\sigma\Delta^2, \\
s &= i\,2\pi f, \\
\Delta &= \text{the thickness of the enclosure walls (m.)} \\
& \quad \text{[Note: in what follows } \Delta \text{ is the thickness} \\
& \quad \text{and t is time],} \\
\mu &= \mu_r\mu_o = \\
& \quad (\mu_o = 4\pi\times10^{-7}), \\
\sigma &= \text{the conductivity of the walls (mhos/m),} \\
f &= \text{the frequency (Hz.),}
\end{aligned}\right\} \tag{3.9c}$$

and wnere

$$\xi_1 = \begin{cases} 0, \text{ (one plate)} \\ K, \text{ (two plates)} \\ K/2 \text{ (cylinder, longitudinal H)} \\ K/2 \text{ (cylinder, transverse H)} \\ K/3 \text{ (sphere)} \end{cases}, \qquad (3.9d)$$

$$\xi_2 = \begin{cases} \frac{Z_0}{R}, \text{ (one plate)} \\ 0, \text{ (two plates)} \\ 0, \text{ (cylinder, longitudinal H)} \\ \frac{1}{2K}, \text{ (cylinder, transverse H)} \\ \frac{2}{3K}, \text{ (sphere)} \end{cases}, \qquad (3.9e)$$

with

$$\left.\begin{aligned} K &= \frac{a}{\mu_r \Delta}, \\ a &= \text{half-separation (two plates), inside radius (cylinder, sphere)}, \\ Z_0 &= \text{the (plane) wave impedance} = 120\pi\Omega \cong 377\Omega, \\ R &= (\sigma\Delta)^{-1} = \text{the DC resistance of the enclosure wall.} \end{aligned}\right\} \qquad (3.9f)$$

In most cases of interest (except iron and steel), $\mu_r \approx 1$ and $\Delta << a$, and hence $K >> 1$. In these cases, one therefore has that $0 \le \xi << 1$ and as a result (3.9) simplifies somewhat because the ξ_2 term can then be neglected in all cases except that for the single plate (and for iron and steel). This simplification is reflected in the results present in Figure 3.15. In that figure and in Figure 3.14 are given values of shielding effectiveness versus frequency for the various canonical enclosure geometries and for various conductivities. One can immediately see from these two figures that, as noted above, at low frequencies the shielding effectiveness of a single metal plate is almost 100 dB larger than that for other enclosures of the same material. It is also interesting to note that the single plate results of the previous section (Schelkunoff Theory) agree well with the single plate results presented in Figure 3.14. For example at 1 kHz Figure 3.14 gives a shielding effectiveness value of about 142 dB for $\sigma = 3.8 \times 10^7$, $\mu = \mu_0$, and $t = \Delta = 1.5$ mm (t = thickness here) while from Figure 3.3 one obtains roughly 136 dB and from Figure 3.6 roughly 5.6 dB, for a total of 141.6 dB. Similarly, at 1 MHz Figure 3.14 yields

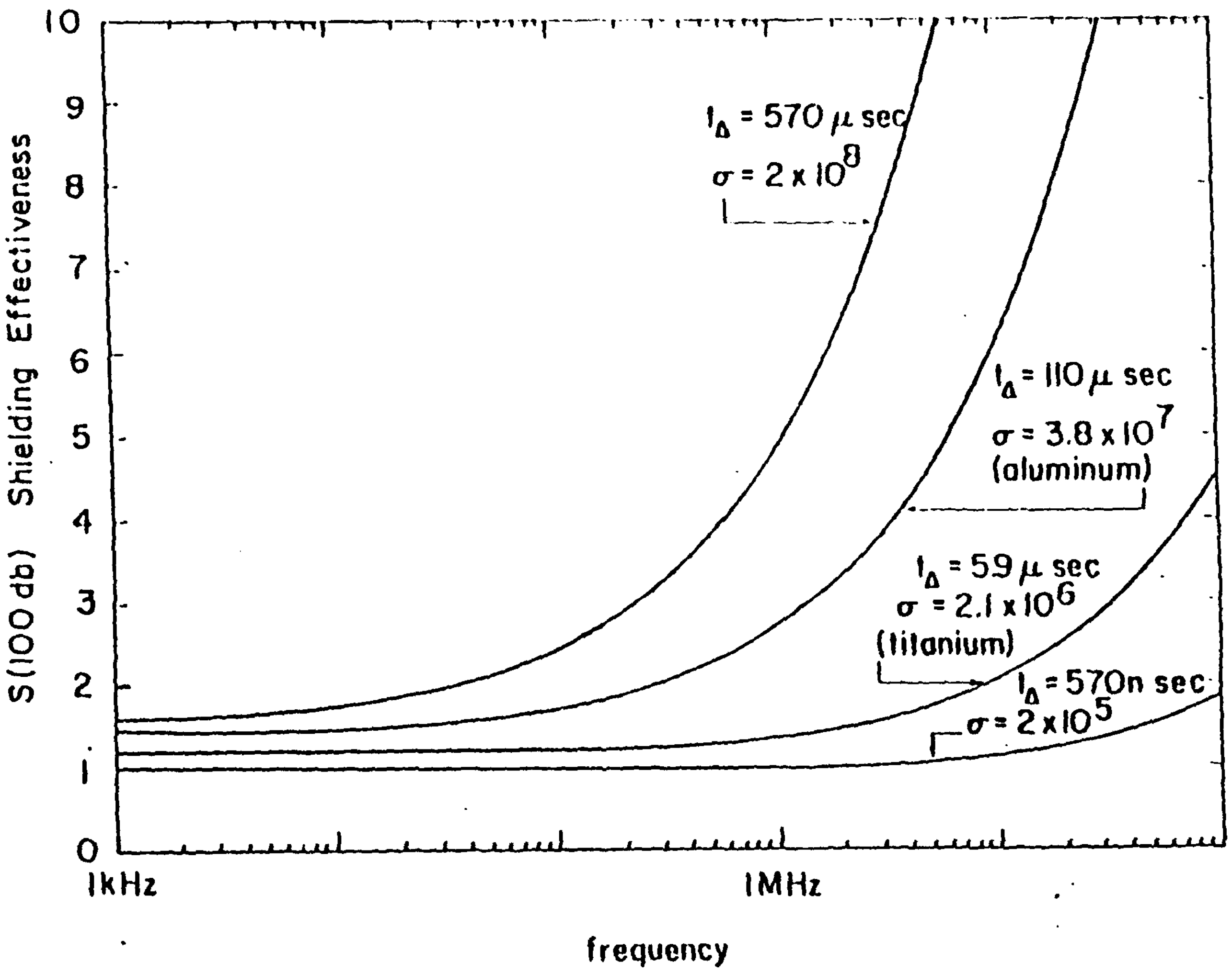


Figure 3.14 The Single-Plate Shielding Effectiveness with $\mu = \mu_0$, $\tau_d = t_\Delta$, and Δ = 1.5 mm [3.9]

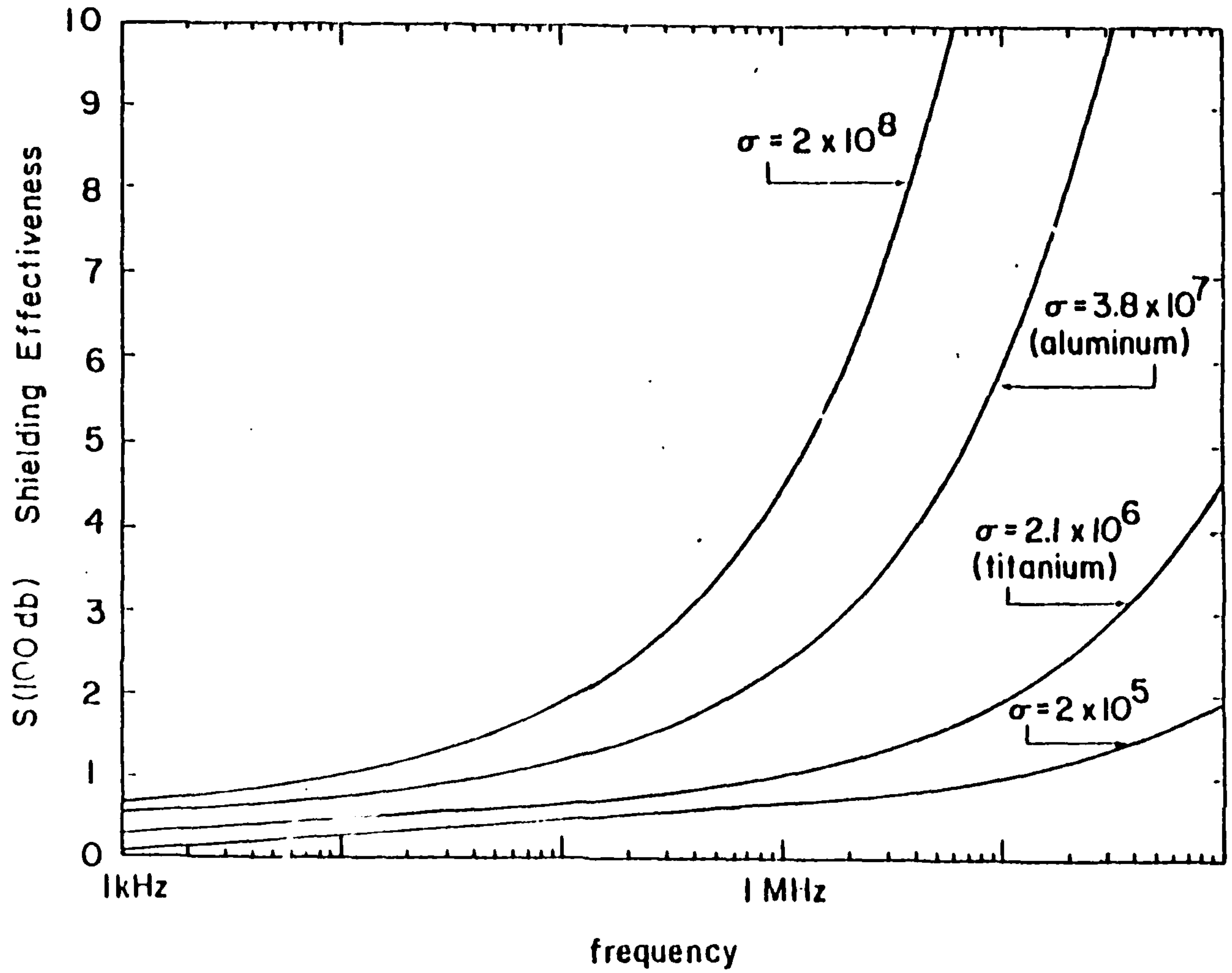


Figure 3.15 The Enclosure Shielding Effectiveness of Two Parallel Plates (a = 1 m), a Cylindrical Shell for Transverse Polarization (a = 2 m), and a Spherical Shell (a = 3 m). The Wall Thickness is Λ = 1.5 mm, while $\mu = \mu_0$ [3.9]

roughly 280 dB, while Figure 3.3 and 3.6 give roughly 105 dB and 185 dB respectively, for a total of 290 dB. However, when Schelkunoff Theory is compared to Figure 3.15 for the other canonical enclosures, one predicts a shielding effectiveness for these two cases of roughly 55 dB and 240 dB respectively. Thus enclosure shape plays an important role in determining the shielding effectiveness of enclosures.

The frequency domain results presented above can be transformed to the time domain as follows (where $H_i(s) = H_o$):

$$H_t(t) = \frac{H_o}{2\pi j} \int_{-j\infty+\alpha}^{+j\infty+\alpha} T_m(s)\, e^{st}\, ds. \tag{3.10}$$

Then according to [3.9], this can be evaluated to yield

$$H_t(t) = \frac{2H_o}{t_\Delta} \sum_{n=0}^{\infty}{}' \frac{q_n\, e^{-q_n^2 t/t_\Delta}}{\left\{1+\xi_1+\xi_1^2\, q_n^2+[\xi_2+\xi_2^2]\, q_n^{-2}\right\} \sin(q_n)} \tag{3.11a}$$

where the prime on the summation indicates that the sum is to run over all $q_n > 0$ which satisfy

$$\cot(q_n) = \xi_1 q_n - \xi_2/q_n \tag{3.11}$$

Although the above series solution is especially useful for late times due to the rapid convergence which accrues when $t > t_\Delta$, it is, in fact the exact solution and converges formally for all $t > 0$. The results for the simplified case discussed above where ξ_2 can be neglected and ξ_1 dominates are shown in Figure 3.16. These curves are "universal" in the sense that they can be used for any of the simple canonical shapes discussed above (except for the single plate and, of course, iron and steel) by using the appropriate values of $\xi=\xi_1$ in (3.9d) and (3.9f) and of τ_d (or t_Δ from (3.9c)). Using these values one obtains "Y" from Figure 3.16, and then computes

$$SE = -20 \log_{10} (Y/Y_c) \text{ dB}. \tag{3.12}$$

By making the appropriate approximations ($\xi_1 = 0$ and $\xi_2 = (Z_o/R) >> 1$ in the single plate, and $\xi_1 >> 1 >> \xi_2$ in the case of the other canonical enclosures), one can simplify (3.11) for early and late times. The results are as follows [3.9]:

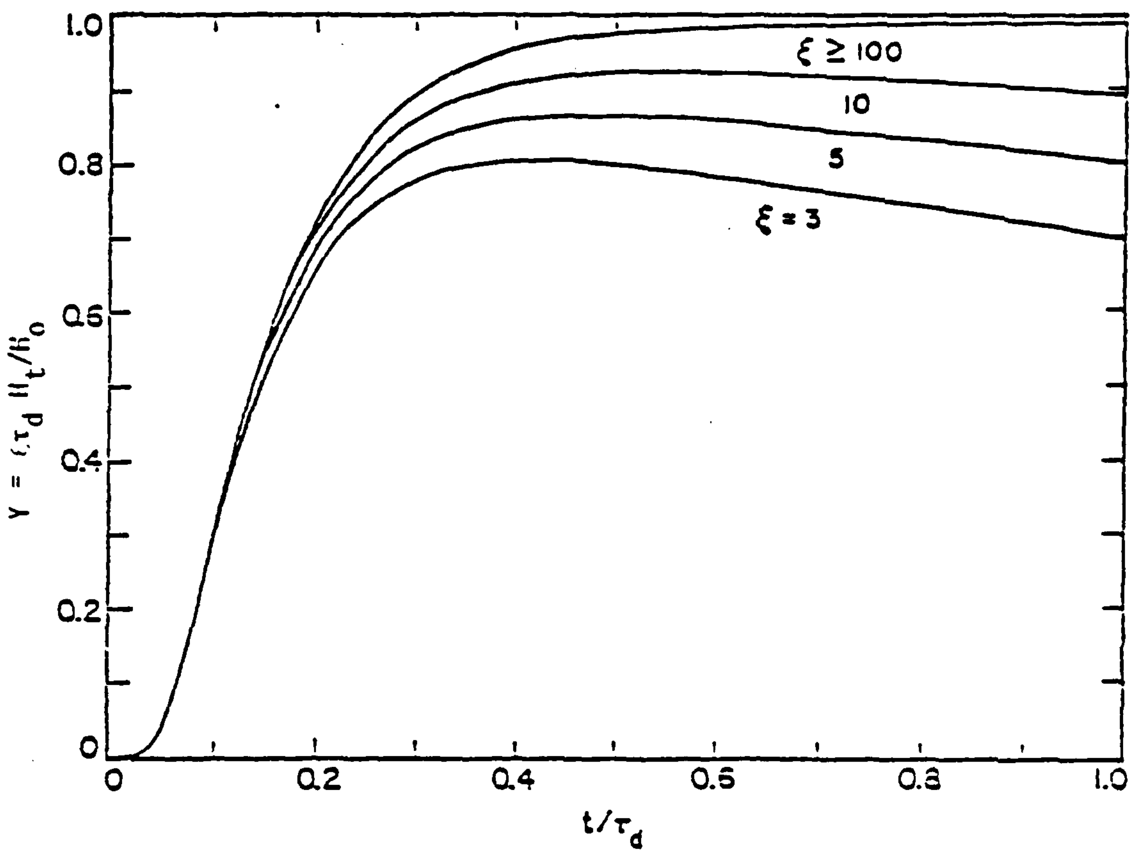


Figure 3.16 Time Variations of the Penetrant EMP for Various Values of ξ ($\xi = \xi_1$) [3.10]

Single Plate:

Early time ($t/t_\Delta \leq 0.05$):

$$H_t(t) = \frac{H_o e^{-t_\Delta/(4t)}}{\sqrt{\pi}\, t_\Delta} \left(\frac{R}{Z_o}\right)\left(\frac{t_\Delta}{t}\right)^{5/2} , \qquad (3.13a)$$

Late time ($t/t_\Delta \geq 0.05$):

$$H_t(t) = \frac{2\pi^2 H_o}{t_\Delta}\left(\frac{R}{Z_o}\right)\left[e^{-\pi^2 t/t_\Delta} - 4e^{-4\pi^2 t/t_\Delta} + 9e^{-9\pi^2 t/t_\Delta}\right], \qquad (3.13b)$$

Other Enclosures:

Early time ($t/t_\Delta \leq 0.1$):

$$H_t(t) = \frac{2H_o e^{-t_\Delta/(4t)}}{\sqrt{\pi}\; \xi t_\Delta}\left(\frac{t_\Delta}{t}\right)^{1/2} , \qquad (3.13c)$$

Late time ($t/t_\Delta \geq 0.1$):

$$H_t(t) = \frac{H_o}{\xi t_\Delta}\left[e^{-t/(\xi t_\Delta)} - 2e^{-\pi^2 t/t_\Delta} + 2e^{-4\pi^2 t/t_\Delta}\right]. \qquad (3.13d)$$

These four approximations can be found compared against the exact results from (3.11) in Figures 3.17 and 3.18. As can be seen there, the approximations or "engineering formulae" in (3.13) provide a simple and accurate method for obtaining the shielding effectiveness of these four canonical enclosures. It should again be recalled, however, that to obtain the "universal" curves, in the case of the single plate, it was assumed that $\xi_1 >> 1 >> \xi_2$. The effect of these assumptions is examined in Figures 3.19 and 3.20 where one can get an idea of their range of validity. It has also been pointed out a number of times that the results above (for enclosures other than the single plate) do not strictly apply to iron and steel material because they do not satisfy the relation $\xi_1 >> 1 >> \xi_2$, and, in addition, their μ_r is a function of frequency (as was shown in Table 3.2). For the frequency range of interest here (roughly 0.5 to 10 MHz), however, μ_r can be taken to be constant and equal to approximately 700 or 800, while lower frequency ranges require larger values. This then allows one to use (3.11) to compute estimates of shielding effectiveness, as is shown in Figures 3.20 and 3.21. It can be seen from these two figures that one could also use the "universal" curves (those with ξ_2 neglected) if

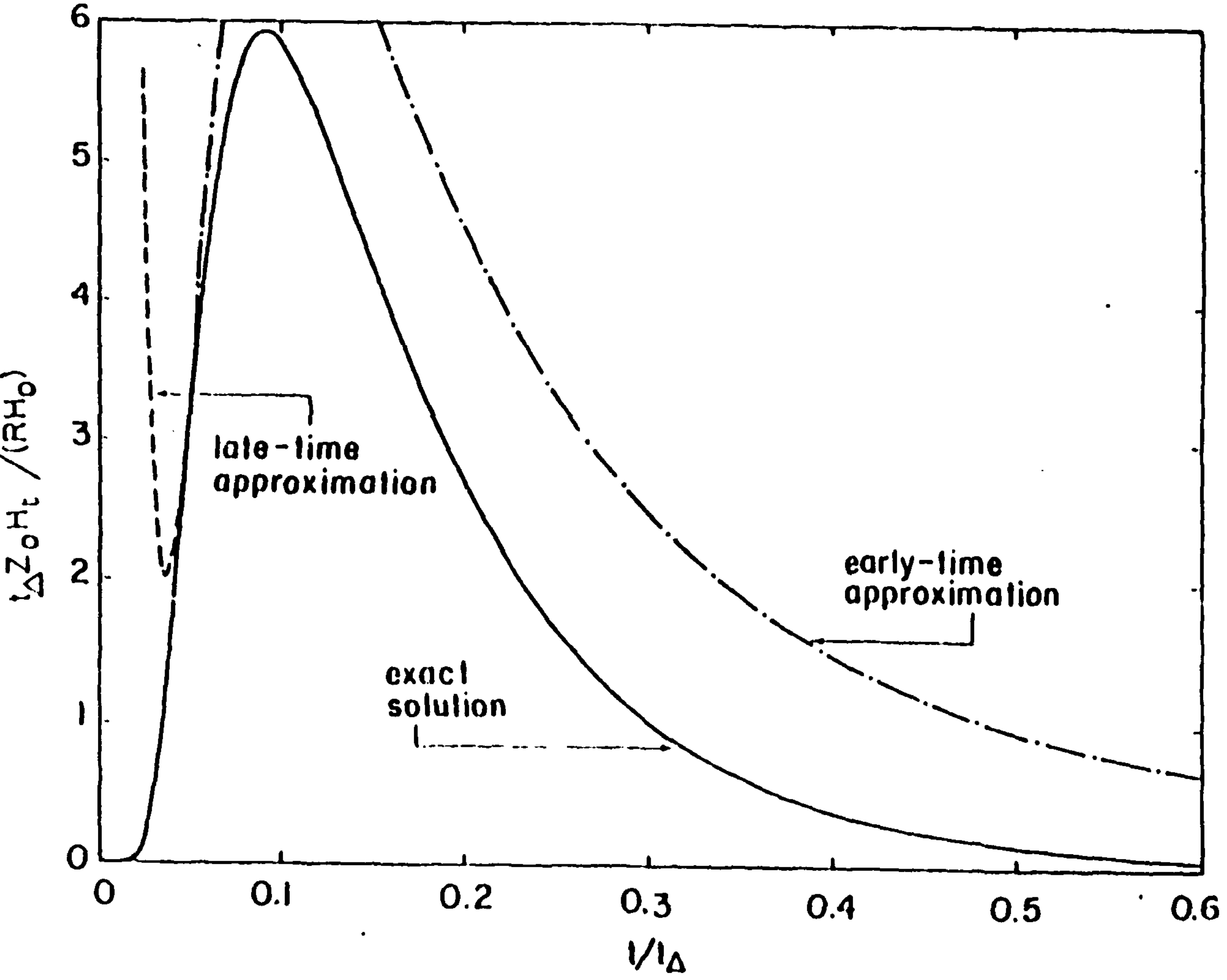


Figure 3.17 Single-Plate Impulse Response [3.9]

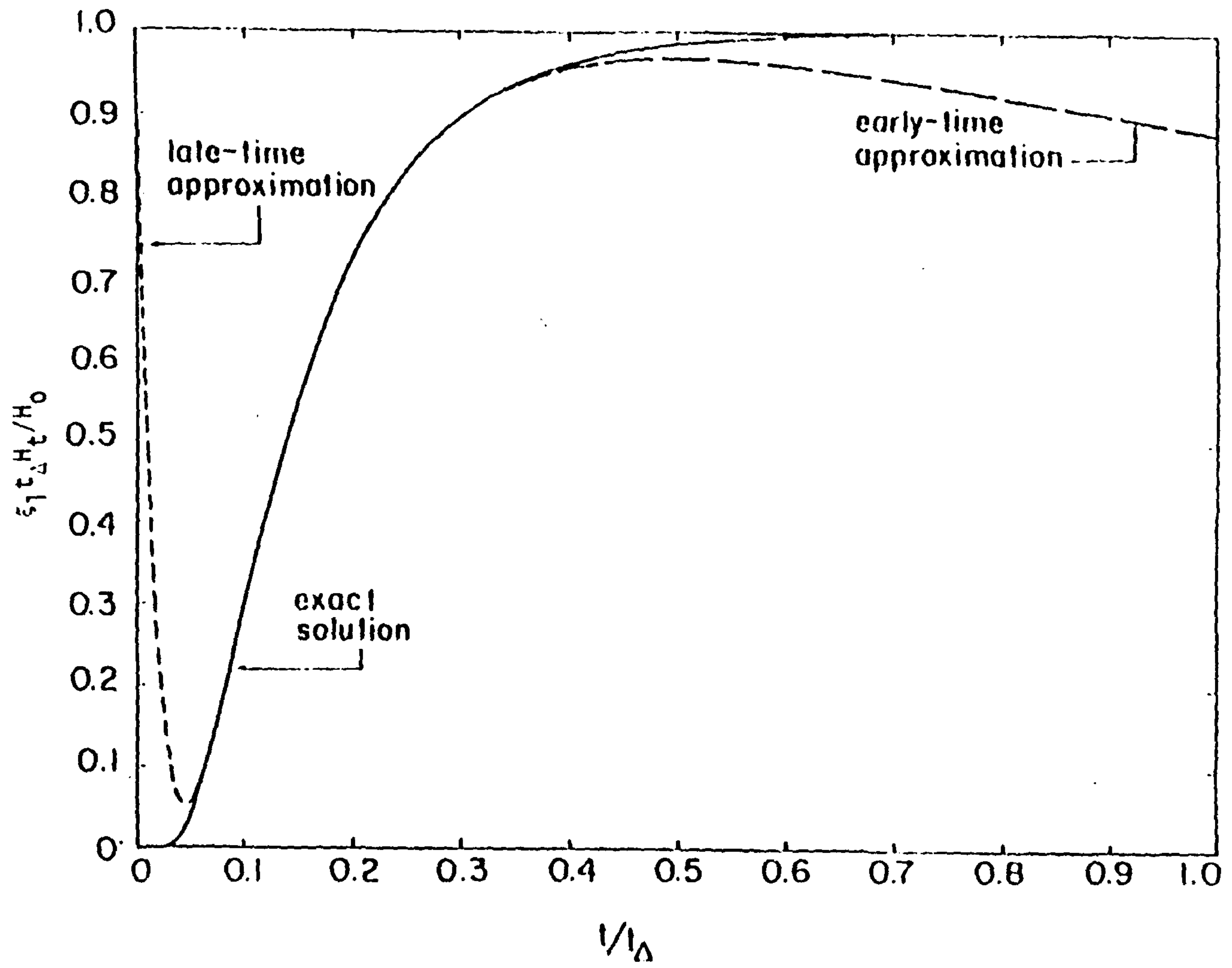


Figure 3.18 Enclosure Impulse Response ($\xi_1 \geq 100$) for Two Parallel Plates ($\xi_1 = a/\Lambda$), a Cylindrical Shell ($\xi_1 = a/2\Lambda$), and a Spherical Shell ($\xi_1 = a/3\Lambda$) [3.9]

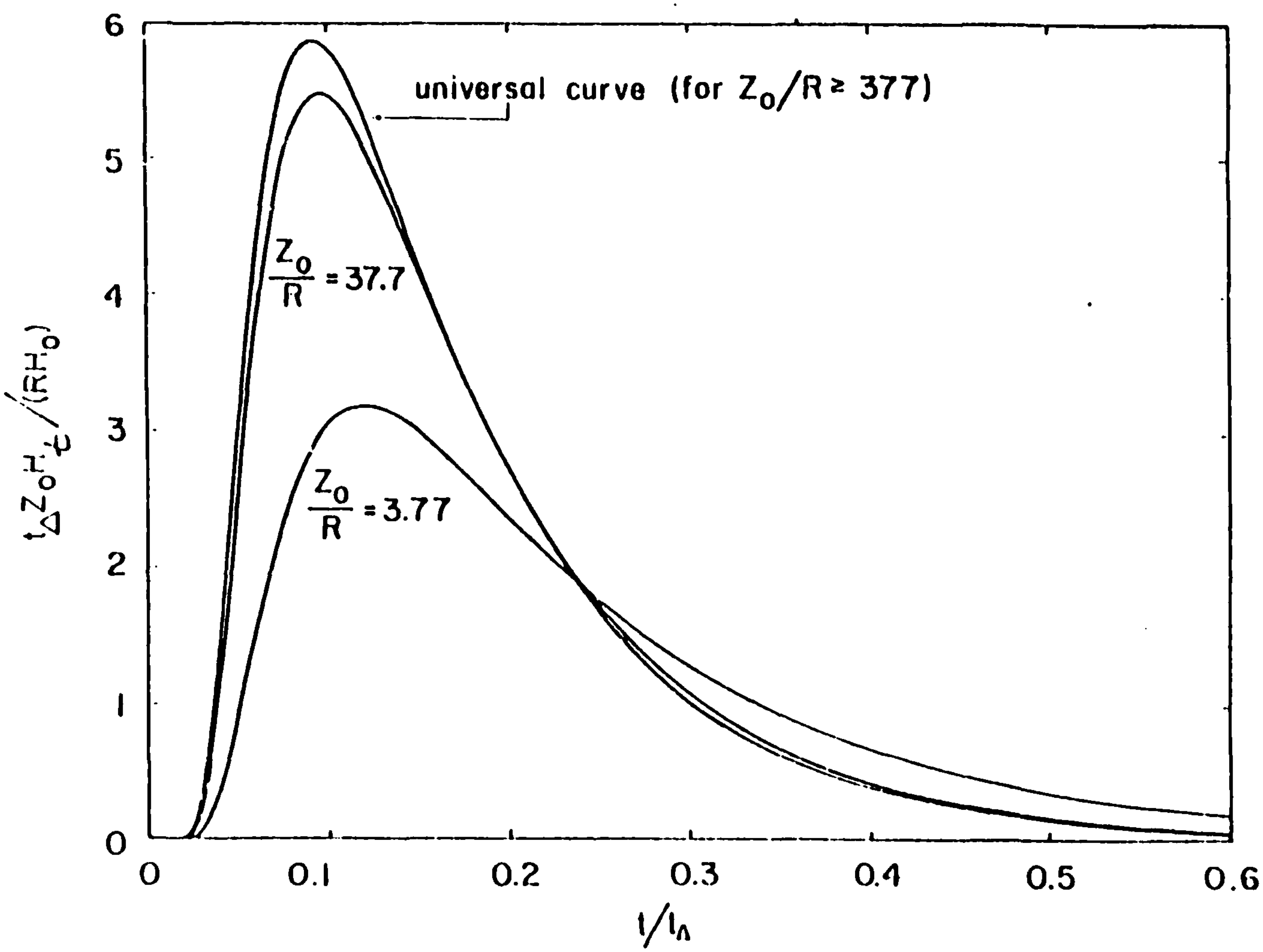


Figure 3.19 Effect of DC Skin Resistance on Single-Plate Response [3.9]

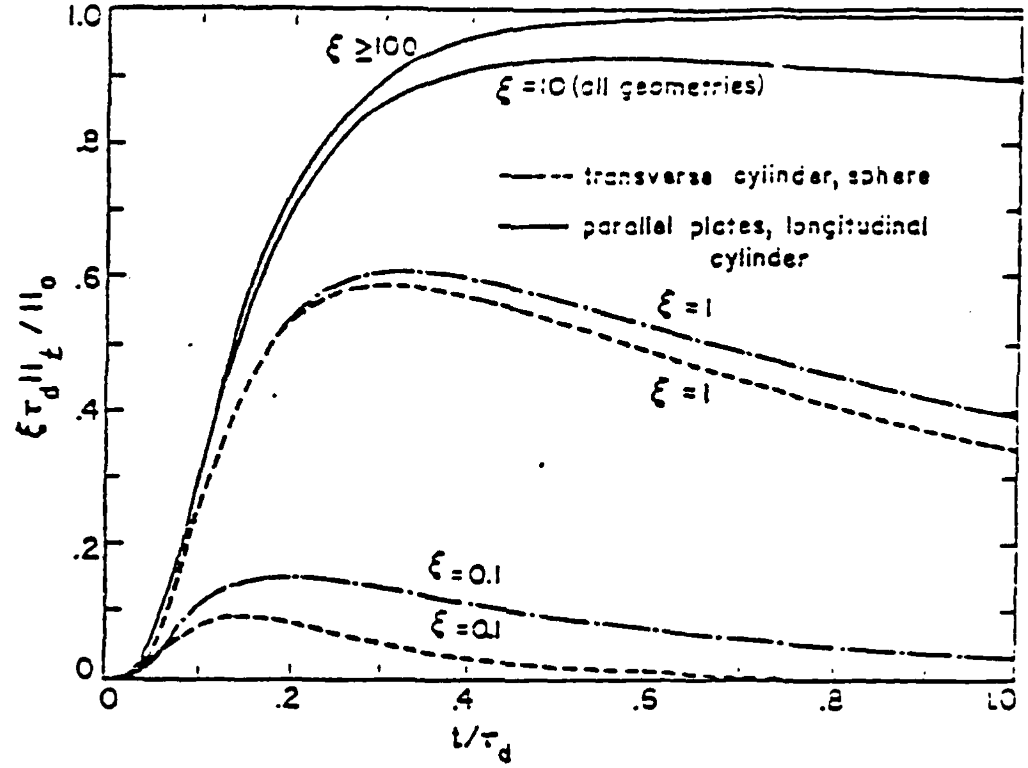


Figure 3.20 Effect of Geometry on Enclosure Response. ξ=K for Two Parallel Plates, ξ=K/2 for Cylindrical Shell, ξ=K/3 for Spherical Shell [3.10]

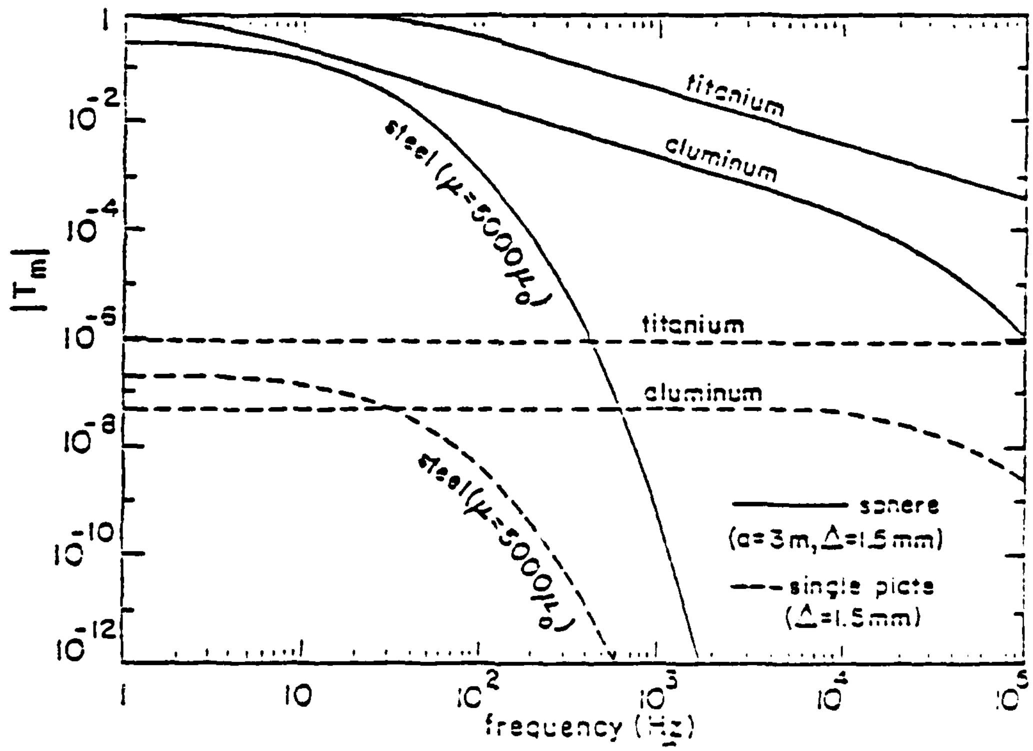


Figure 3.21 Single-Plate and Enclosure Transfer Function Versus Frequency Where T_m is Defined by (3.9b), [3.10]

desired, because they underestimate the shielding effectiveness of the enclosure in question. Other parameters of interest can be deduced as shown in Table 3.3.

Table 3.3 Engineering Parameters of the Penetrant Pulse [3.10]

Geometry	ξ	H^{int}(peak)	$\dot{H}^{int}$(peak)	Rise Time (10 - 90%)	Decay Time (1/e)
Single plate	$\frac{Z_o}{R}$	$\frac{6\ H_o}{\xi t_\Delta}$	$\frac{120\ H_o}{\xi t_\Delta^2}$	$\frac{t_\Delta}{20}$	$\frac{t_\Delta}{\pi^2}$
Parallel plates	$\frac{\mu_o r}{\mu\Delta}$	$\frac{H_o}{\xi t_\Delta}$	$\frac{6\ H_o}{\xi t_\Delta^2}$	$\frac{t_\Delta}{4}$	ξt_Δ
Cylinder	$\frac{\mu_o r}{2\mu\Delta}$	$\frac{H_o}{\xi t_\Delta}$	$\frac{6\ H_o}{\xi t_\Delta^2}$	$\frac{t_\Delta}{4}$	ξt_Δ
Sphere	$\frac{\mu_o r}{3\mu\Delta}$	$\frac{H_o}{\xi t_\Delta}$	$\frac{6\ H_o}{\xi t_\Delta^2}$	$\frac{t_\Delta}{4}$	ξt_Δ

Noncanonically Shaped Enclosures. Since Figure 3.20 shows that as $\xi(=\xi_1)$ becomes large the detailed geometrical differences in the enclosures become less important, then the existence of a general formula valid for arbitrary geometry is suggested. As Lee and Bedrosian [3.8 - 3.10] show, this general relation is given by

$$\xi = \frac{1}{\mu_r} \frac{V}{S\Delta} = \frac{\tau_f}{\tau_d}, \tag{3.14}$$

where

$\tau_d = t_\Delta = \mu\sigma\Delta^2$ = the diffusion time,

$\tau_f = L/R$ = the fall (decay) time,

$R = (\sigma\Delta)^{-1}$ = the DC wall resistance,

$L = \mu_o V/S$ = the cavity inductance.

It is easy to show that this reproduces the ξ_1 values shown in (3.9d) - except for the first. With this value of ξ and the values of τ_d (or equivalently t_Δ) one can now obtain the shielding effectiveness for arbitrarily shaped enclosures from (3.12) and either Figure 3.16, equation (3.13), or (3.11) in the previous section.

3.2.2 Shielding from Exterior Fields

As (2.4) indicates, the incident fields here are plane waves. Consequently, the theory presented in Section 3.2.1 is applicable. The enclosure to be considered everywhere in this chapter is the standard rack cabinet with dimensions 6'H x 2'W x 3'D, and about 2-3 mm thick. Then $V = 36\ ft^3 = 1.02\ m^3$ and $S = 72\ ft^2 = 6.69\ m^2$ in (3.14). If the metal is aluminum, then from Table 3.1 $\sigma = (0.61) \times (5.8 \times 10^7)$ mhos/meter, and $\mu_r = 1$. This yields a value for ξ of 60.96 and a value for τ_d (or t_Δ of 0.111. Hence $\xi\tau_d$ is 6.78 and Y from Figure 3.16 is roughly 0.98 at is peak value. The result from (3.12) is a (time domain) magnetic field shielding effectiveness of roughly 17 dB. The electric field shielding effectiveness of course, will be much larger, as explained earlier, and, hence, of no consequence here. From (2.4), the peak H field will be roughly 139.3 Amperes/meter, hence the peak magnetic field internal to the cabinet will be roughly 17 dB lower, or approximately 20 Amperes/meter.

3.2.3 Shielding from Interior Fields

In this case the incident field is not a plane wave. Rather, it is the field at the surface of the enclosure due to the current of equation (2.2) being used to drive a wire, as shown in Figure 3.1. Because, to first order, the diffusion fields inside the enclosure are driven only by the surface current density on the enclosure, then a reasonable estimate of the magnetic field inside the enclosure can be obtained from the equivalent plane wave field which would cause the same surface current density. In order to determine the surface current density on the enclosure, a three-dimensional numerical finite-difference calculation was performed for the situation depicted in Figure 3.1 and equation (2.2). In this calculation, Maxwell's equations are solved by standard numerical techniques [3.1] to obtain the electric and magnetic field components everywhere in the problem space as a function of time. As a result, the total magnetic field $\bar{H}$ everywhere on the surface of the enclosure is determined as a function of time. This value is simply related to the surface current density $\bar{J}$ by $\bar{J} = \bar{n} \times \bar{H}$, while it is related to an equivalent plane wave incident field (H_o) by $\bar{J} = 2\bar{n} \times \bar{H}$. Hence the equivalent plane wave field (H_o) is equal to H/2. By determining the peak value of H on the enclosure, one can then determine the equivalent peak plane-wave field H/2 and use the methods of the previous section to determine H in the enclosure.

The finite difference calculations yielded a peak H of 3.0 Amperes/meter. Consequently the internal field should be 17 dB smaller than H/2, or roughly 0.2 Amperes/meter.

3.2.4 Shielding from Cable Currents (Current Injection)

As was indicated in Section 3.1, the current waveform given by (2.2), in the present instance, is injected directly onto the enclosure (see Figure 3.22). The current is assumed to enter the surface of the enclosure and to distribute uniformly (in angle) and flow in a radial direction. Then, the electric field immediately inside of the enclosure wall is given by

$$E(\omega) = \frac{I(\omega)}{2\pi r} Z_T(\omega), \tag{3.15}$$

where I is the current, r is the radial distance from the center point of the injected current, and Z_T is the surface transfer impedance of the metal walls. The total voltage along a radial line between point r_o and r_{max} is then given by

$$V(\omega) = \int_{r_o}^{r_{max}} E(\omega)\, dr. \tag{3.16}$$

In order to estimate a worst case response, r_o is taken to be the radius of a #22 AG wire (r_o = 0.000648 m) and r_{max} is taken to be the largest shelter dimension (r_{max} = 6 ft = 1.8288 m). A metal wall thickness (Δ) of 2 to 3 mm is also assumed.

Evaluating (3.15) and (3.16), then yields

$$\left.\begin{aligned} V(\omega) &= \frac{\ln\left(r_{max}/r_o\right)}{2\pi} I(\omega)\, Z_T(\omega), \\ &\text{where} \\ I(\omega) &= 10 \text{ A for } 0.5,\ 2,\ \text{and } 10 \text{ MHz} \\ Z_T(\omega) &= \eta/\mathrm{Sinh}\,(k\Delta), \end{aligned}\right\} \tag{3.17}$$

with (see Figure 3.23 for a plot of η):

$$\begin{aligned} \eta &= [i\, 2\pi\mu f/\sigma]^{1/2} = (1+i)\,\alpha/\sigma, \\ K &= (1+i)\alpha, \\ \alpha &= [\pi\mu f\sigma]^{1/2}, \\ r_o &= \text{minimum radius in meters}, \\ r_{max} &= \text{maximum radius in meters}, \\ \Delta &= \text{metal wall thickness in meters}. \end{aligned}$$

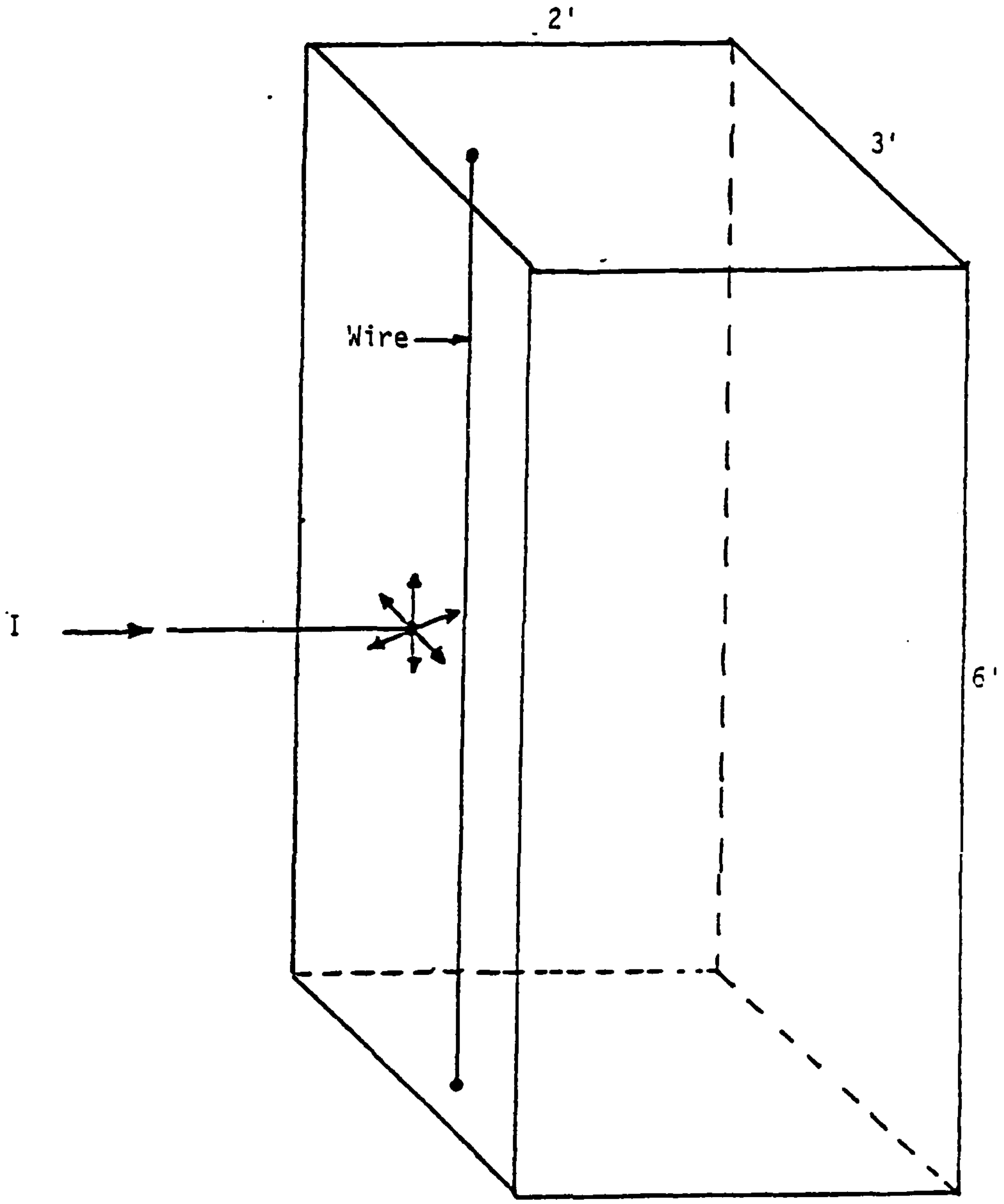


Figure 3.22 Diffusion of the Current Injected Fields

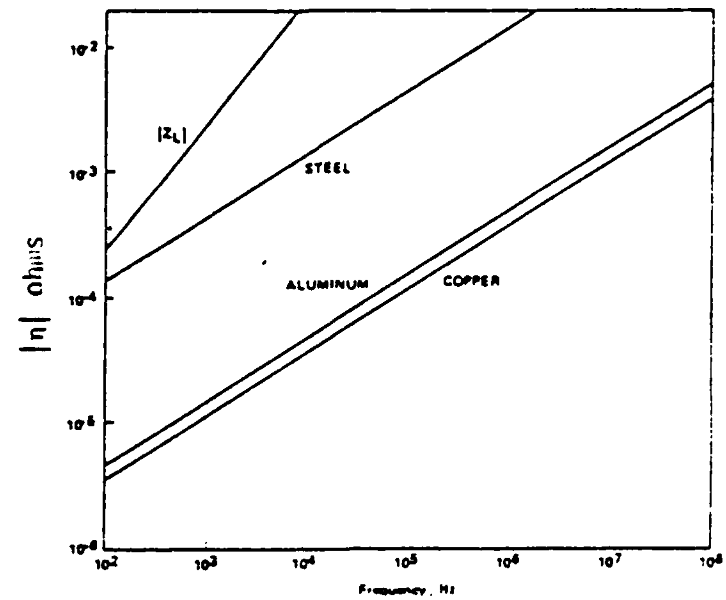


Figure 3.23 Shield Impedance $|\eta|$ (Equation 3.17) for Copper, Aluminum, and Steel and the Loop Wave Impedance $|Z_L|$ (r = 12 in.) Plotted as Functions of Frequency [3.1]

$\omega = 2\pi f$,

f = the frequency in Hz.,

σ = the wall conductivity in mhos/meter,

μ = the wall permeability.

As (3.17) easily shows, this results in an induced voltage of no more than a few microvolts. This can also be seen from scaling the results in Reference 3.11 (page 93) by the appropriate relative assumed current values.

3.2.5 Summary

As can be demonstrated from the previous sections, in all cases the field leakage due to diffusion can be kept to a quite small level by using metal walls of even small thickness.

3.3 Seams

3.3.1 Background

It can be seen from the results in the previous section that the direct penetration of EMP energy through the metal walls of an enclosure by diffusion can be successfully reduced to a small level. However, an enclosure cannot realistically be manufactured out of a single monolithic piece of metal. Rather, flat metal sheets must be bonded together at the edges to form an enclosure and this gives rise to seams.

Seams are traditionally the weak spots in any electromagnetically shielded enclosure. The main objective in seam design is to provide a low ($\leq 10^{-3}$ ohm-meter) seam transfer impedance Z_s (ohm-meters) in order to minimize its leakage. Also the impedance must not significantly degrade with age, environment and usage. In terms of the exterior surface current density J_s (Ampere/meter), the internal voltage V_s (Volts) induced across the seam is given by

$$V_s(\omega) = J_s(\omega)\, Z_s(\omega). \tag{3.18}$$

If a wire were routed immediately behind the seam, V_s is the maximum voltage that would be induced upon it. There is, in addition, the seam transfer admittance Y_s which relates the current induced on a near-by internal wire to the external voltage It has been found however, for good quality seams that the sources arising from the transfer admittance are dominated by sources arising from the transfer impedance in all cases of practical interest [3.11, 3.13]. Therefore the discussion here centers on Z_s. Also, Z_s depends upon the direction of current flow with respect to the seam, with the largest induced voltages occurring when J_s is perpendicular to the seam direction. When J_s is parallel to the seam direction, the induced voltage is much smaller. Therefore the discussion here deals with currents normal to the seam direction.

Two types of seams are discussed here. They are continuous-welded and bolted seams. Because continuous welding has been observed to provide as much shielding as continuous metal [3.11], attention is focused here on bolted seams. Such bolted seams can be either gasketed or metal-to-metal lapped joints (plated or unplated), and data on the surface transfer impedance Z_s will be presented for each. There is not a great deal of seam data available in transfer impedance format, but there is enough to show that properly designed and installed bolted or gasketed seams can provide the required amount of shielding. Various types of gasketing, caulking, and lapped-joint schemes have been evaluated in a special test fixture (see Figures 3.24 and 3.25) which is used to measure the seam transfer impedance [3.13 - 3.16]. In the case of bolted lapped joints some of the available data [3.17] is in the form of polarizability M. In this case, Z_s occurs due to imperfect contact between the irregular metal surfaces and is primarily inductive:

$$Z_s = j\omega L_s = j\omega \mu_0 M, \tag{3.19}$$

where M is the polarizability per unit length of the seam in m^2. The polarizability of such bolted joints depends upon the bolt torque, the spacing

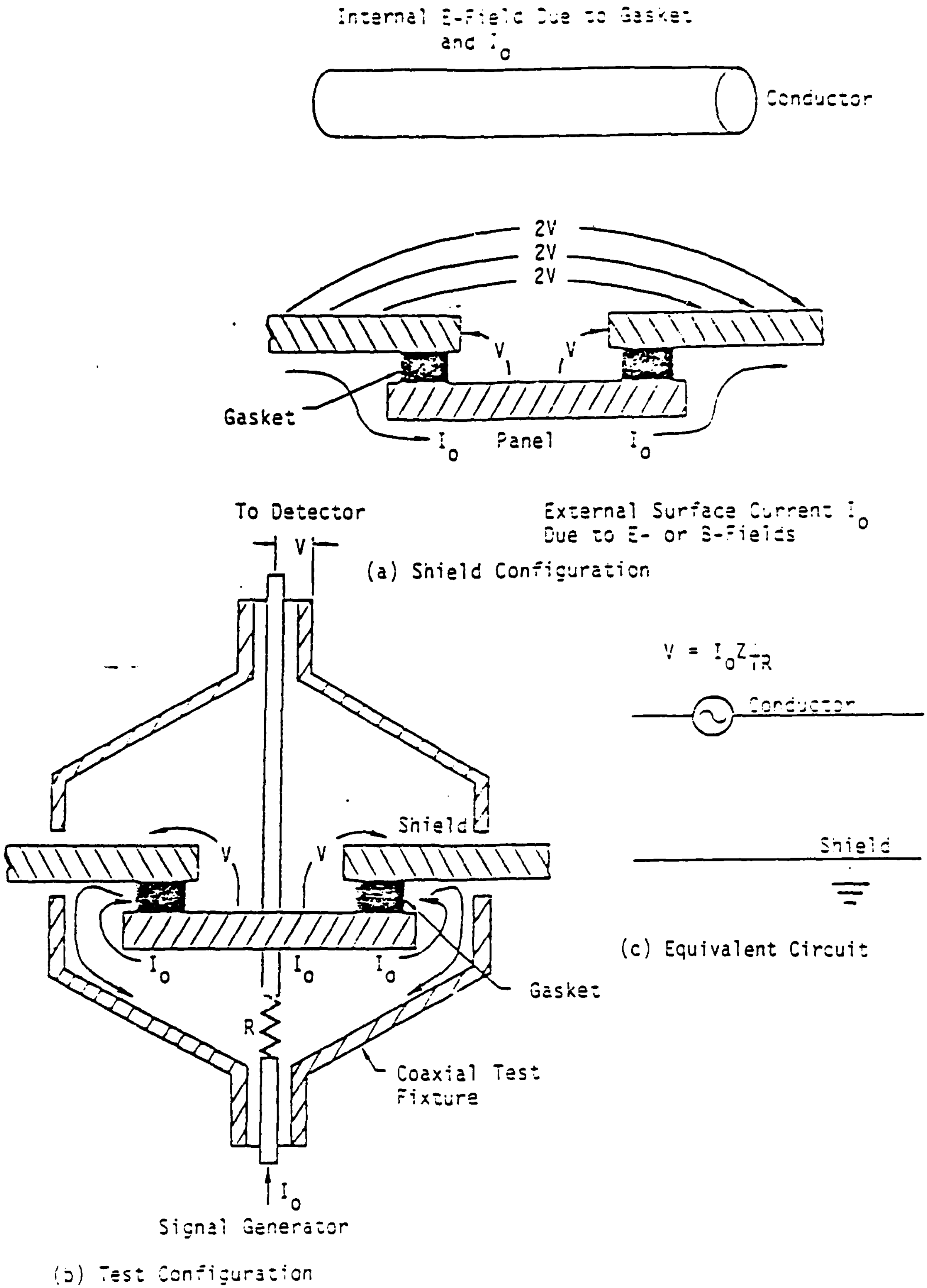


Figure 3.24 A Schematic Representation of the Transfer Impedance Test Fixture [3.13]

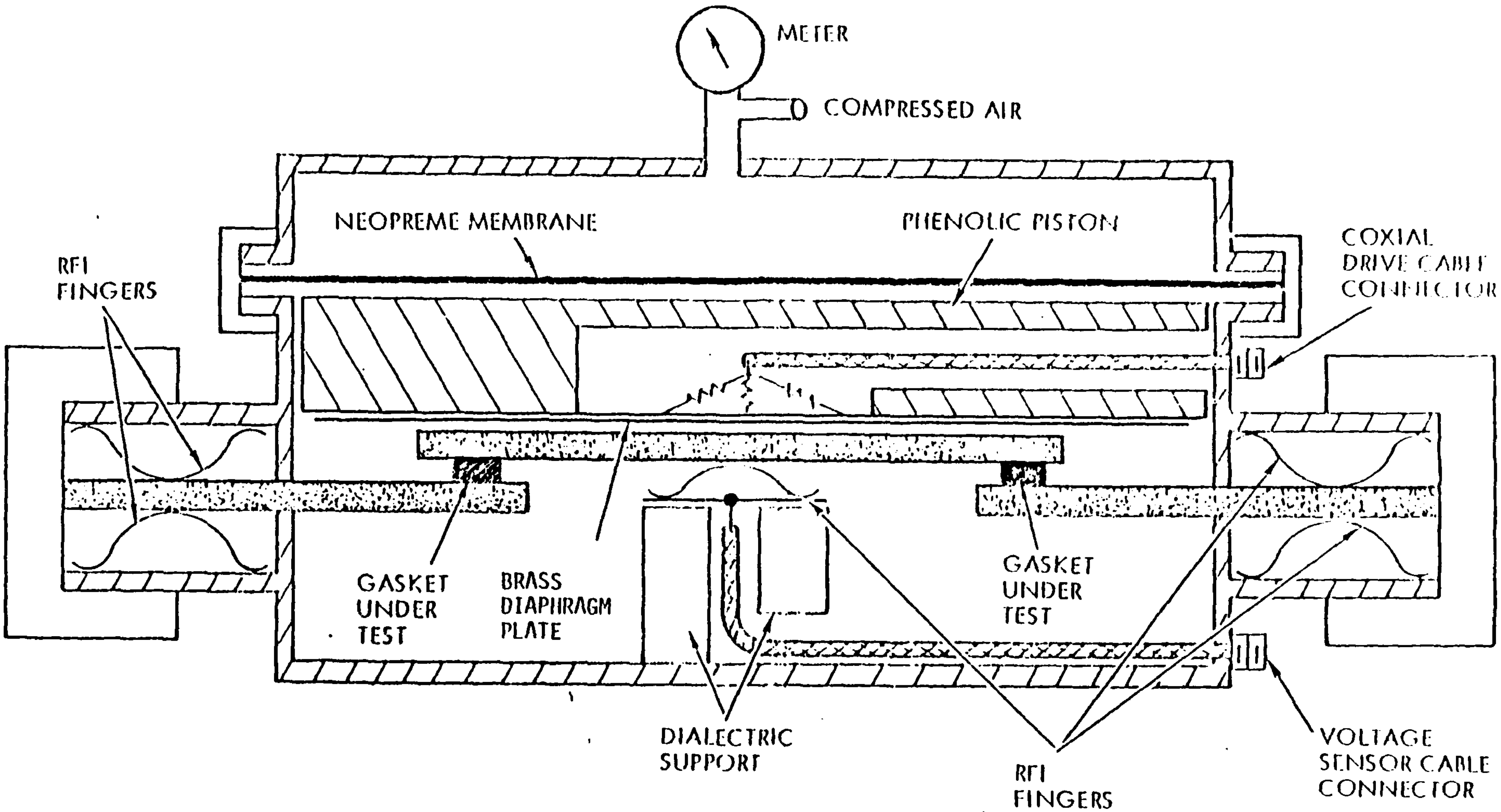


Figure 3.25 TRW's Test Fixture for Transfer Impedance Measurements of RFI Gasket Materials [3.14]

between the bolts, and the amount of overlap.

These values of Z_s combined with (3.18) (transformed from frequency-domain to time-domain) can then be used to provide the driving fields for a solution of Maxwell's equations inside the enclosure [3.12]. In this fashion, the internal fields, current, voltage, power, and energy can be determined.

For purely resistive $Z_s(\omega)$ the time-domain equivalent of (3.18) is

$$V(t) = R_s \cdot J_s(t), \qquad (3.20)$$

while for a purely inductive $Z_s(\omega)$, one has

$$V(t) = L_s \cdot \frac{dJ_s}{dt}, \qquad (3.21)$$

where R_s and L_s are the transfer resistance and inductance, respectively.

Figures 3.26 through 3.30 give examples of the seam transfer impedance for various gaskets and plates as measured by Madle [3.13]. In Figure 3.26 the cases of Aluminum-Aluminum and Brass-Brass contact (no gasket) are shown along with the results for deliberately bad configurations where the plates are separated by a neoprene spacer. These latter examples are generally not practical in that no designer would adopt such configurations in a situation where a high level of shielding is desired. However, they do illustrate a situation where the transfer impedance consists of the conductivity and self-inductance due to the screws used to hold the panels together and of the capacitance due to the overlapping neoprene-insulated metal panels.

Figure 3.31 illustrates the effect on the seam transfer impedance of plating the aluminum plates and of aging ("shelf-aging") the gaskets as measured by Kunkel [3.16]. On the other hand, Figures 3.32 through 3.34 illustrate the effects on seam polarizability of bolt torque, bolt spacing, and panel overlap [3.17].

Figure 3.35 through 3.44 present some recent measurements by Lowell [3.14] at the TRW transfer impedance measurement facility. Figures 3.35 through 3.38 show the effect of applied pressure, panel metal type, and environment (temperature/humidity and salt - per MIL-STD-810C, Methods 507 and 509, and MIL-STD-202, Method 106B) on a Monel gasket (Tecknit Elastomet #82-55312), while Figures 3.39 and 3.40 illustrate similar effects for a 1/8" x 1/4" Silver Consil-R gasket (Tecknit #85-10447). One should note that the Consil-R gasket has the highest transfer impedance of all those measured [3.14], and thus can be used as a worst-cast situation.

Finally, Figures 3.41 through 3.44 illustrate the effects of bolt spacing, environment (as above), panel overlap, panel thickness (rigidity), and conductive caulk on an aluminum-aluminum seamed (ungasketed) panel.

As can be seen, typical seam transfer impedances range from roughly 10^{-5} ohm-meters to sometimes as high as 10 or so ohm-meters.

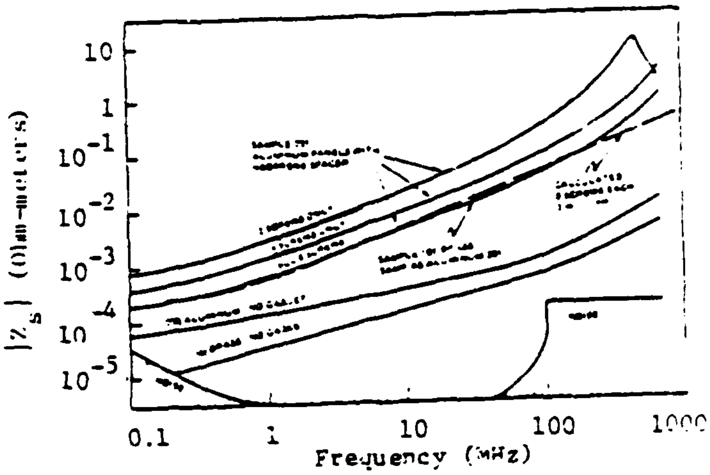


Figure 3.26 Aluminum and Brass Panels with no Gaskets with 2.5 Inch Seam Overlap Fastened by #10-32 Screws (8 if not specified). [3.13]

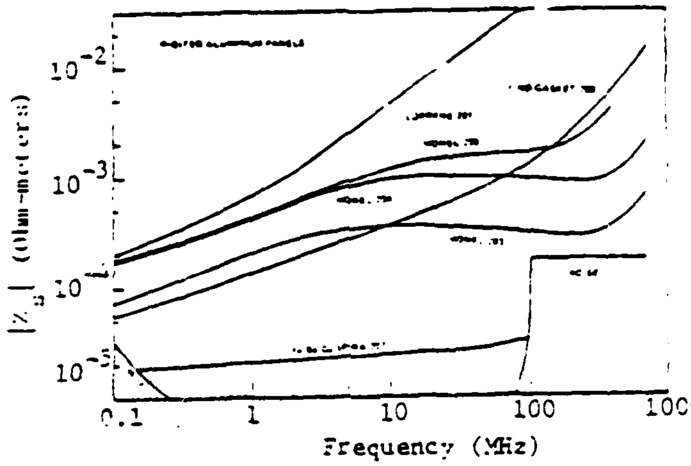


Figure 3.27 Aluminum Panels with Monel and Tin Gaskets with 2.5 Inch Seam Overlap Fastened by 8 #10-32 Screws [3.13]

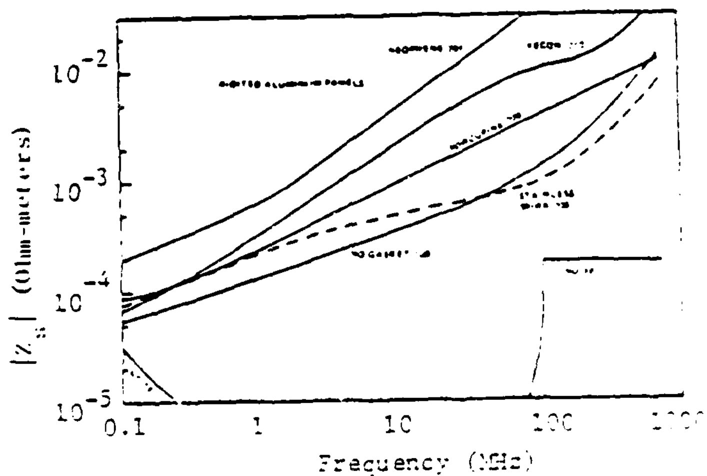


Figure 3.28 Aluminum Panels with Other Types of Gaskets with 2.5 Inch Seam Overlap Fastened by 8 #10-32 Screws [3.13]

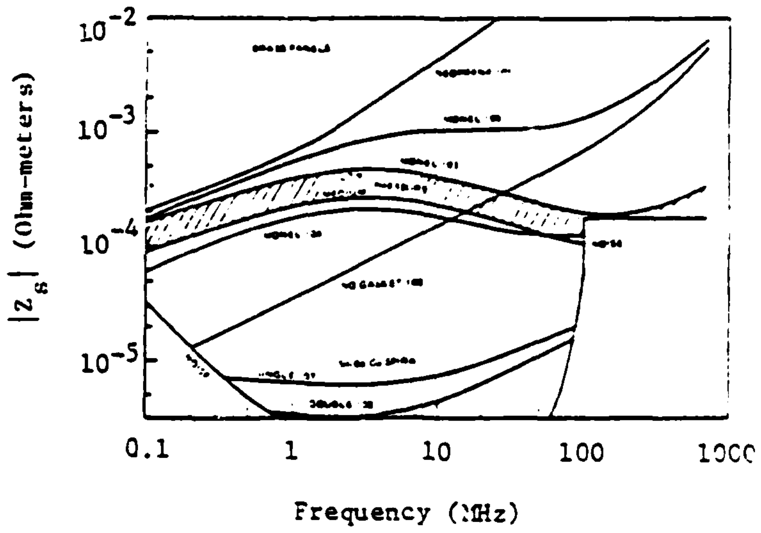


Figure 3.29 Brass Panels with Monel and Tin Gaskets with 2.5 Inch Seam Overlap Fastened by 8 #10-32 Screws [3.13]

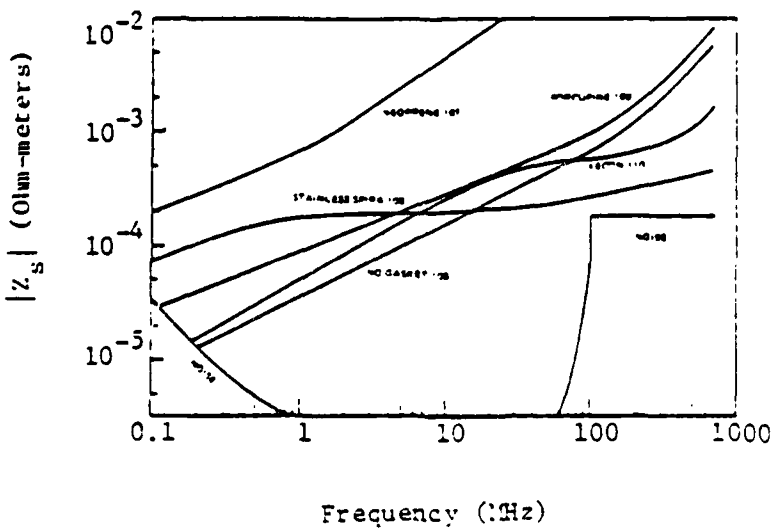
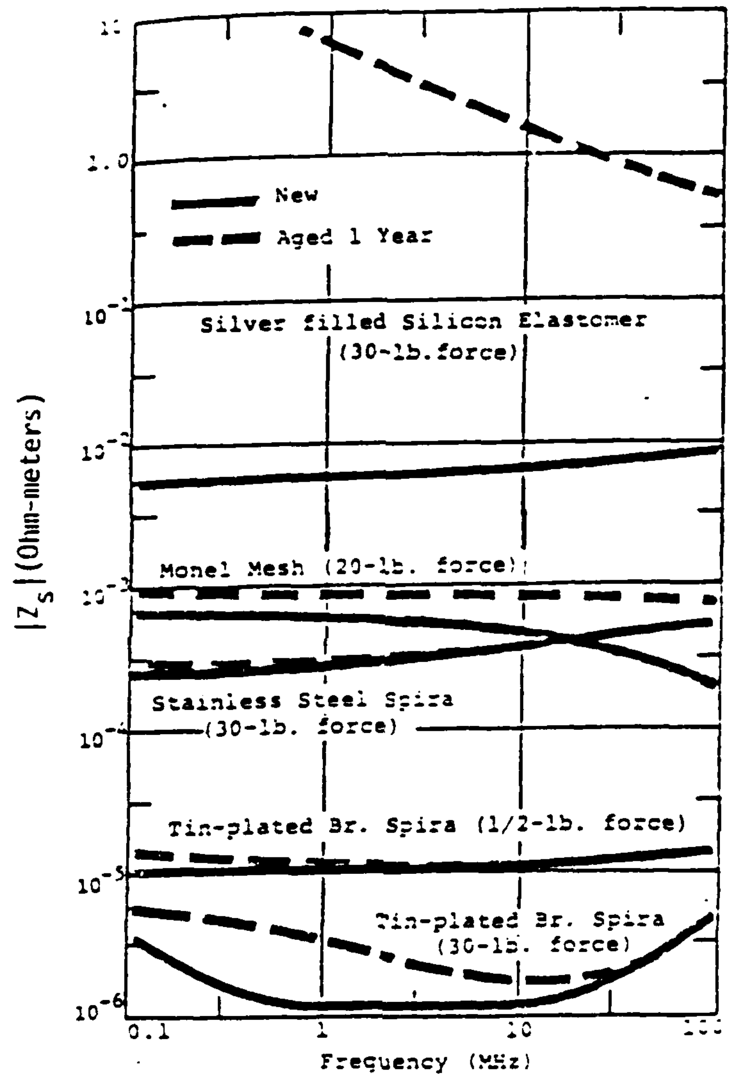
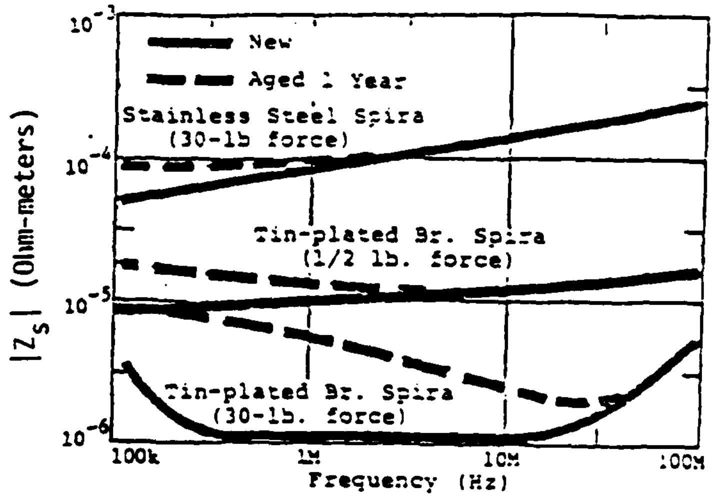


Figure 3.30 Brass Panels with Other Types of Gaskets with 2.5 Inch Seam Overlap Fastened by 8 #10-32 Screws [3.13]

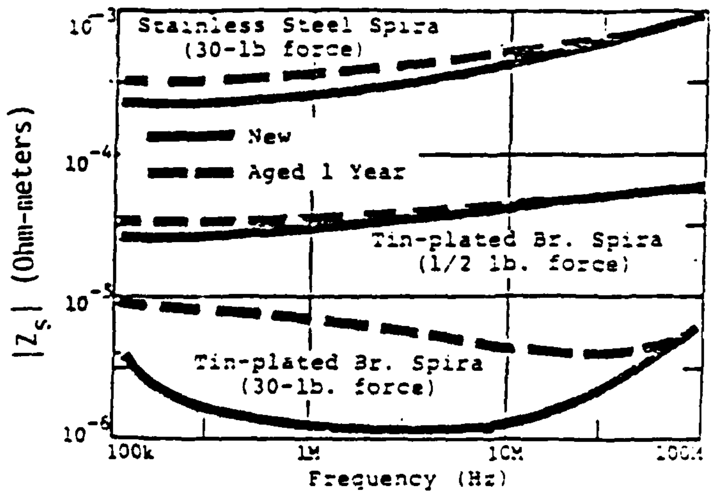


(a) Iridited Aluminum Plates

Figure 3.31 The Effects of Plating, Applied Force, and Aging on Typical Gaskets [3.16]

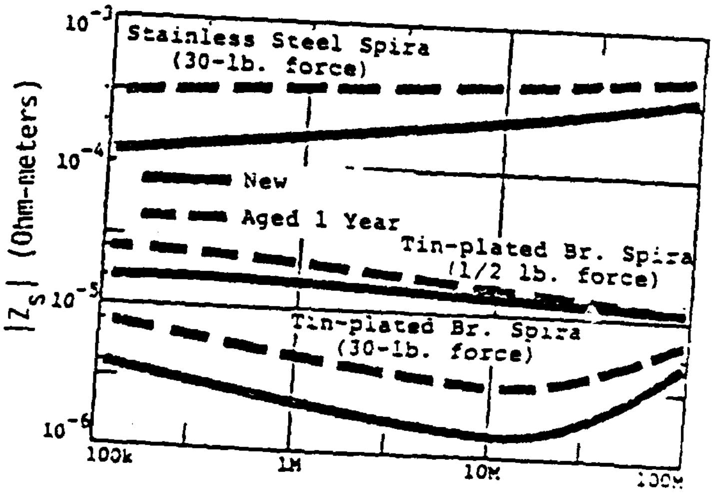


(b) Tin-Plated Aluminum Plates



(c) Cadmium-Plated Aluminum Plates

Figure 3.31 (cont'd) The Effects of Plating, Applied Force, and Aging on Typical Gaskets [3.16]



(d) Nickel-Plated Aluminum Plates

Figure 3.31 (cont'd) The Effect of Plating, Applied Force, and Aging on Typical Gaskets [3.16]

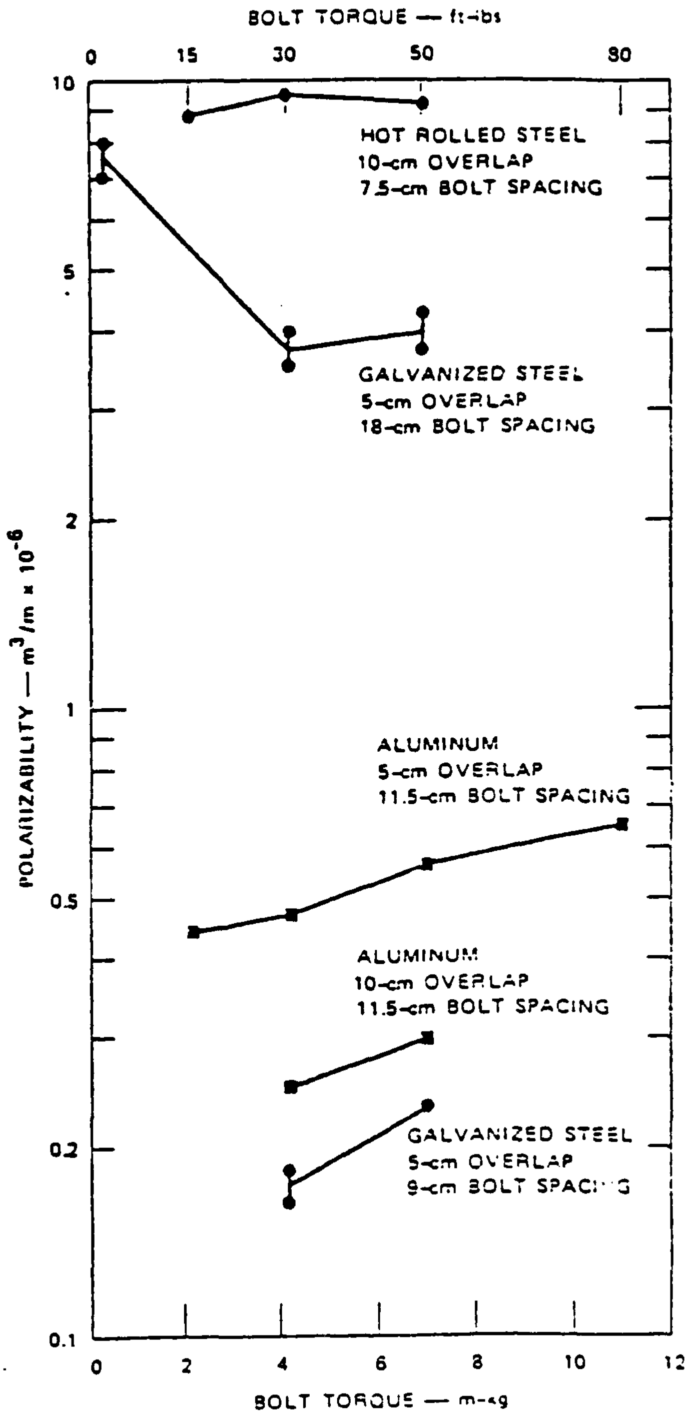


Figure 3.32 Variation in Polarizability with Bolt Torquing [3.17]

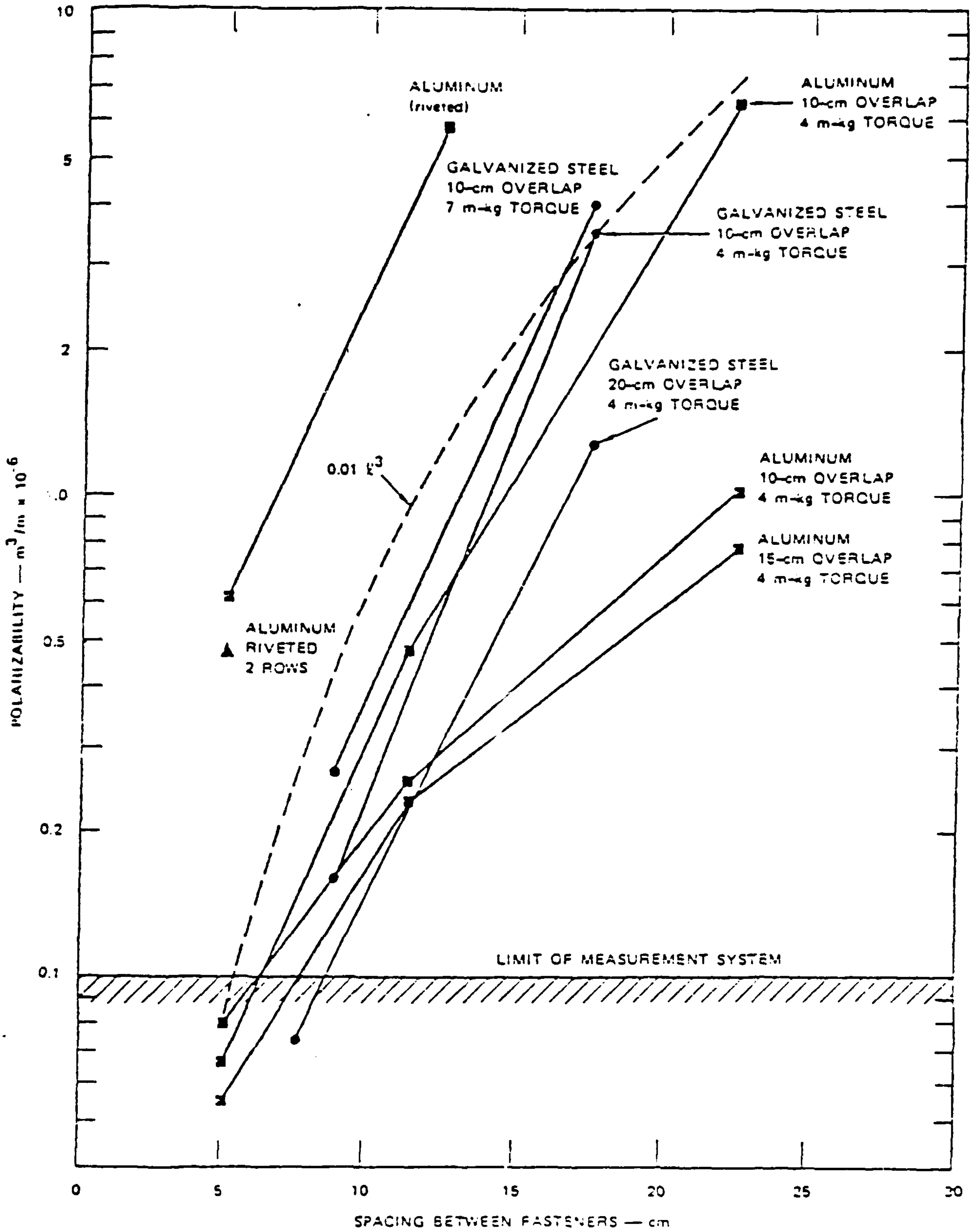


Figure 3.33 Variation in Polarizability with Spacing Between Fasteners [3.17]

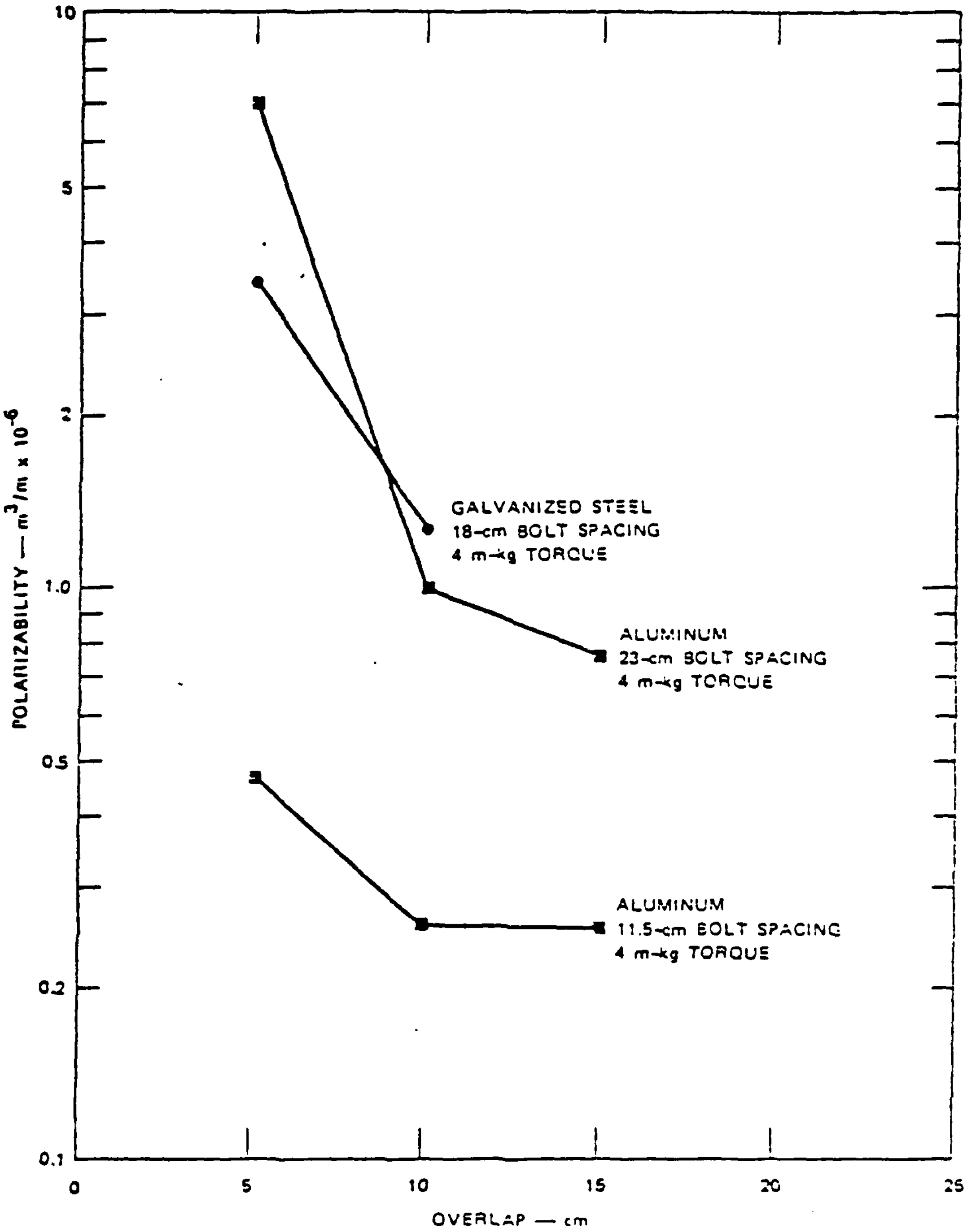


Figure 3.34 Variation in Polarizability with Joint Overlap [3.17]

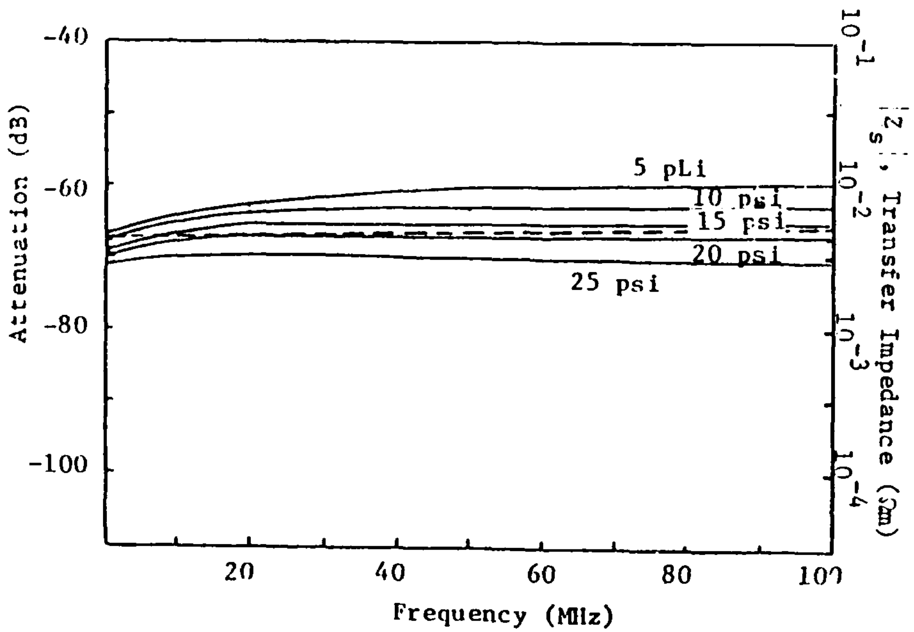


Figure 3.35 The Transfer Impedance of a Monel Gasket (Tecknit Elastomat #82-55312 Versus Frequency and Applied Pressure for an Aluminum Plate [3.14]

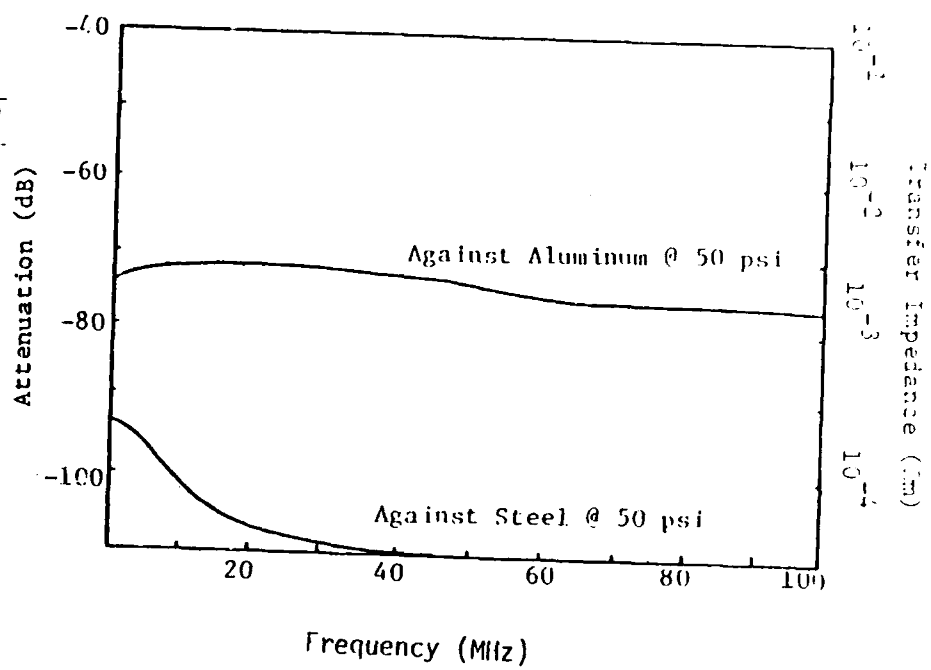


Figure 3.36 The Transfer Impedance of a Monel Gasket (Tecknit Elastomat #82-55312) Versus Frequency at 50 psi for an Aluminum and Steel Plate [3.14]

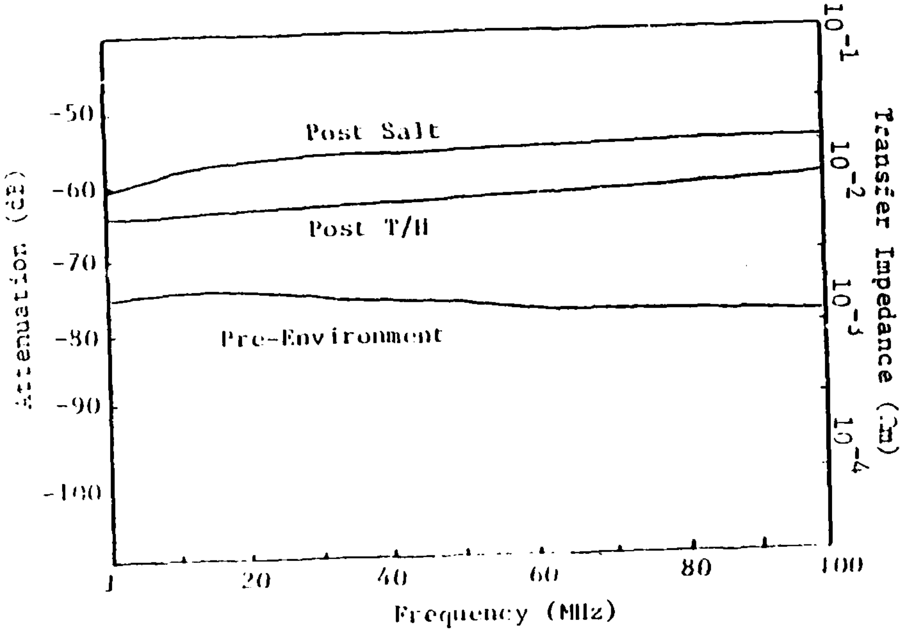


Figure 3.37 The Effects of Temperature/Humidity and Salt Environments on a Monel Gasket (Tecknit Elastomet #82-55312 on an Aluminum Plate), [3.14]

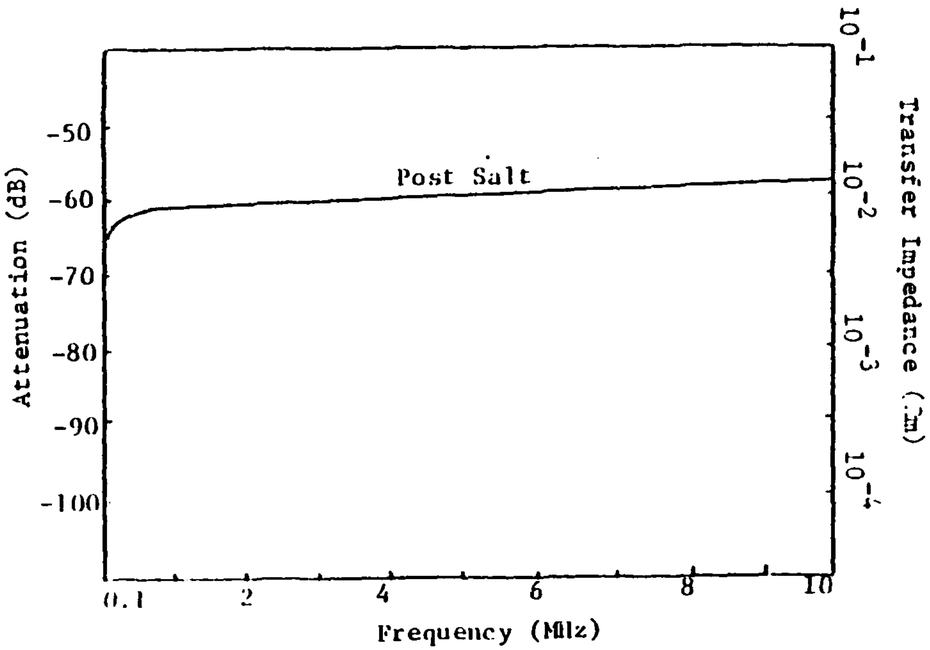


Figure 3.38 The Effects of a Salt Environment on a Monel Gasket (Tecknit Eleastomat #82-55312 on an Aluminum Plate, 0.1 x 10 MHz) [3.14]

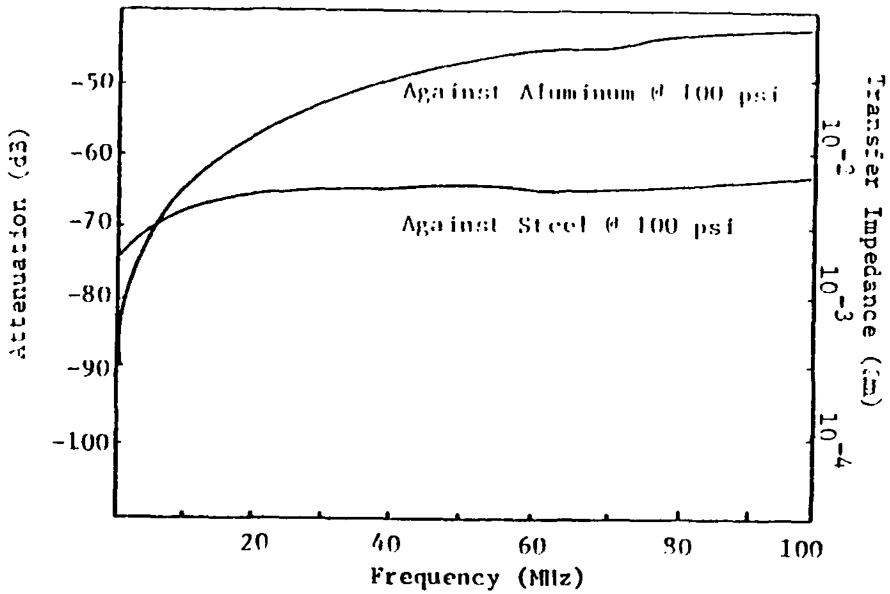


Figure 3.39 The Transfer Impedance of a 1/8" x 1/4" Silver Consil-R Gasket (Tecknit #85-10447) versus Frequency at 100 psi for an Aluminum and a Steel Plate [3.14]

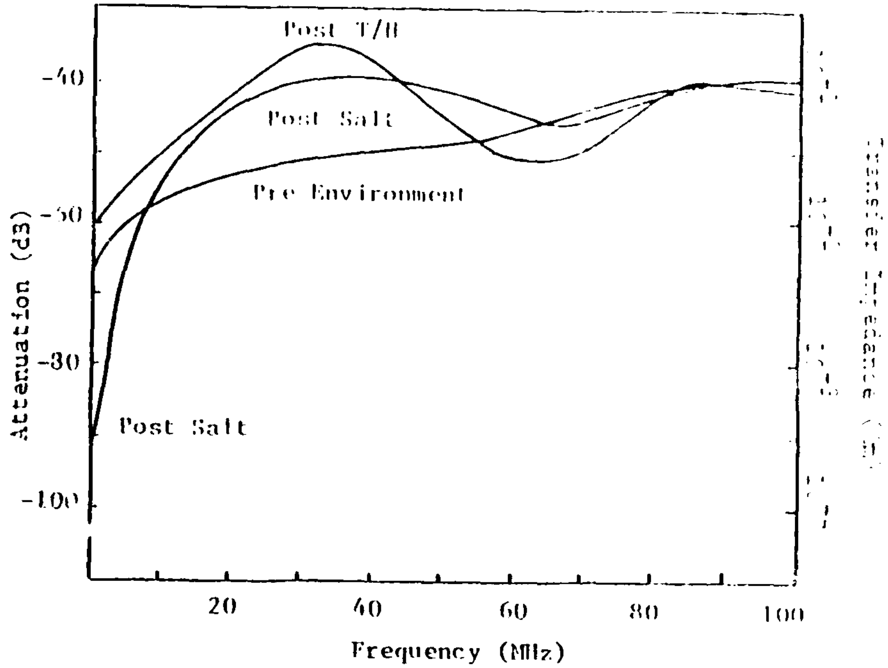


Figure 3.40 The Effects of Temperature/Humidity and Salt Environments on a 1/8" x 1/4" Silver Consil-R Gasket (Tecknit #85-10447) for an Aluminum Plate [3.14]

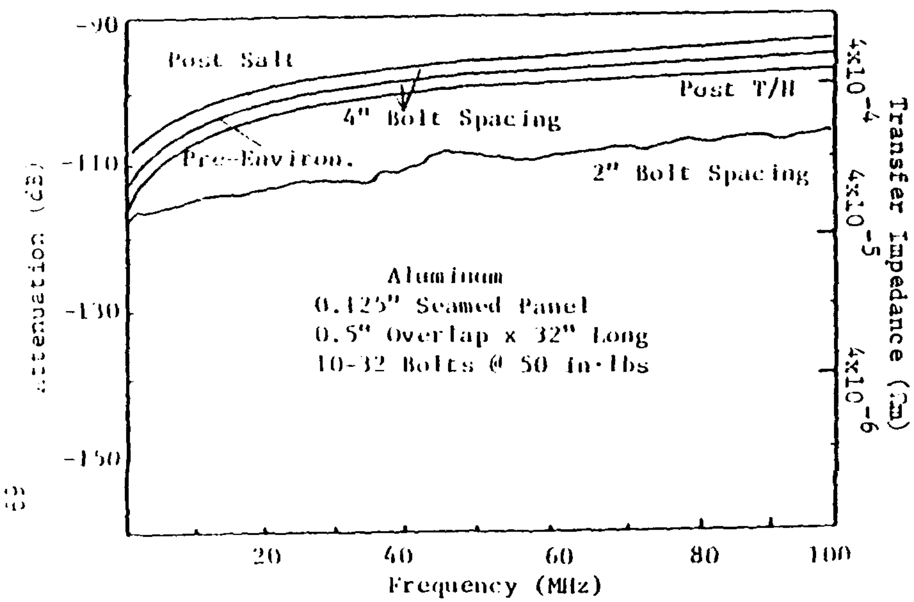


Figure 3.41 The Effects of Bolt Spacing and Environment (Temperature/Humidity and Salt) on a 0.125" Aluminum-Aluminum Seamed Panel with a 0.5" Overlap [3.14]

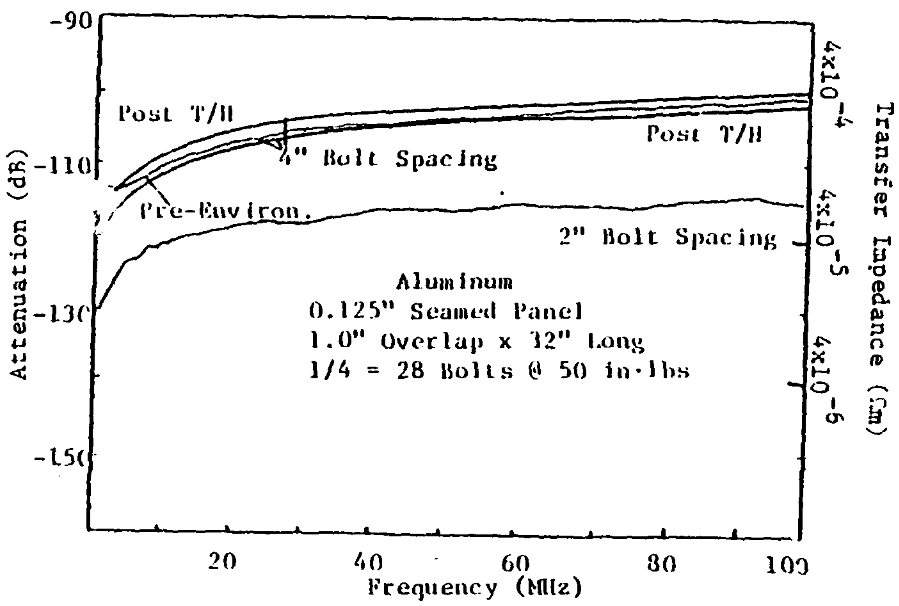


Figure 3.42 The Effects of Bolt Spacing and Environment (Temperature/Humidity and Salt) on 0.125" Aluminum-Aluminum Seamed Panel with a 1.0" Overlap [3.14]

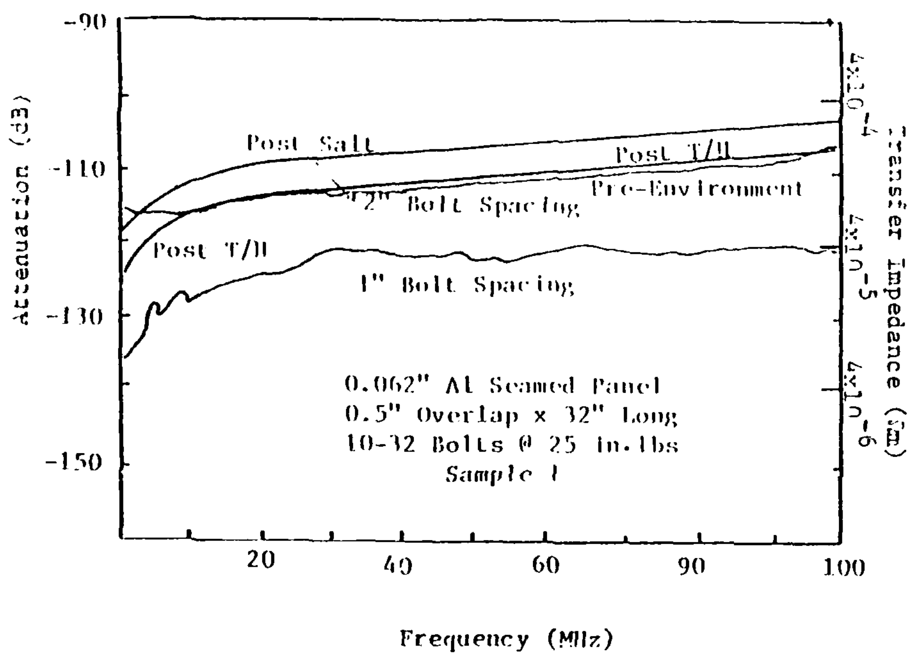


Figure 3.43 The Effects of Bolt Spacing and Environment (Temperature/Humidity and Salt) on a 0.062" Aluminum-Aluminum Seamed Panel with a 0.5" Overlap [3.14]

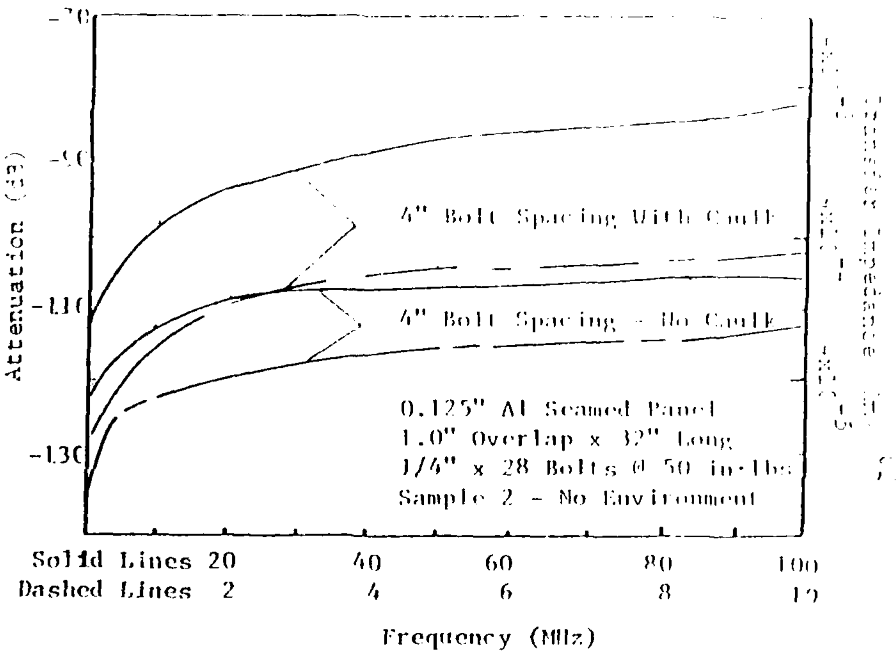


Figure 3.44 The Effects of Conductive Caulk on a 0.125" Aluminum-Aluminum Seamed Panel with 1.0" Overlap (Tecknit #72-00014) [3.14]

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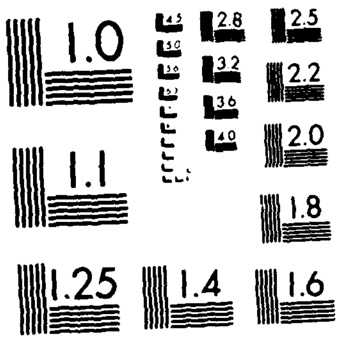

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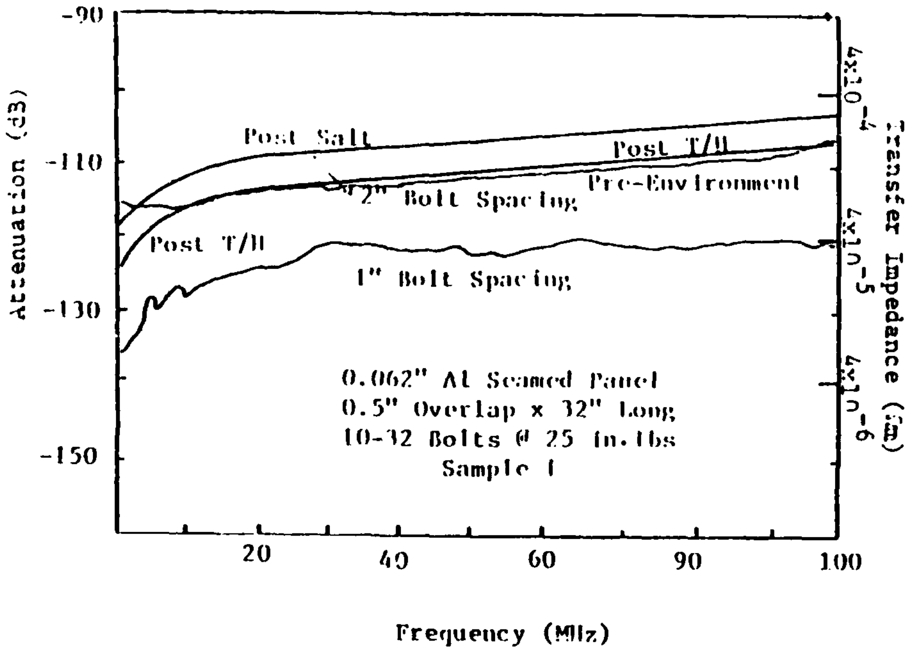


Figure 3.43 The Effects of Bolt Spacing and Environment (Temperature/Humidity and Salt) on a 0.062" Aluminum-Aluminum Seamed Panel with a 0.5" Overlap [3.14]

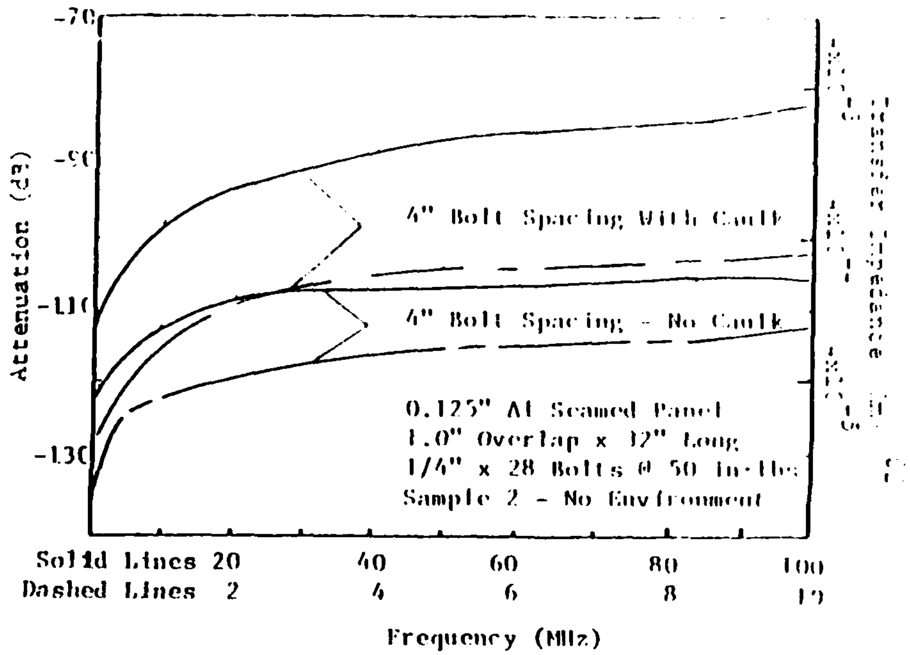


Figure 3.44 The Effects of Conductive Caulk on a 0.125" Aluminum-Aluminum Seamed Panel with 1.0" Overlap (Tecknit #72-00014) [3.14]

3.3.2 Shielding from Exterior Fields

In this case two problems had to be solved by numerical three-dimensional finite-difference solution of Maxwell's equations - the exterior problem (i.e. fields exterior to the cabinet) and the interior problem (i.e. fields inside the cabinet). First, the 6'H x 2'W x 3'D cabinet was illuminated by the plane wave specified in (2.4) and the (short-circuit) surface current density on the exterior surface of the cabinet was determined. Next, this surface current density was used along with equation (3.20a) (and, separately, 3.20b) to excite the interior of the cabinet. From this latter "interior model", then, the interior fields were determined as functions of space and time. These were, in turn, used to determine (see Figure 3.45): 1) I_{sc}, the peak short-circuit current in a 6' wire 7.6 cm from and perpendicular to the seam (this wire was short-circuited at each end to the top and bottom of the cabinet), V_{oc}, the peak open-circuit voltage in a roughly 3' x 6' loop oriented with its plane perpendicular to the direction of the seam, and 3) P and E, the peak power and energy dissipated in a resistively terminated (instead of shorted) 6' wire. The resistive termination at each end of the wire is equal to the characteristic impedance of the wire in order to ensure maximum power and energy transfer. These results can be found in Table 3.4 in the four columns labeled "Exterior Field". The values for the resistive seam are for an R_s value of 1 milliohm-meter, while the values for the inductive seam are for an L_s value of 10 picohenry-meters. As can be seen from Figures 3.25 - 3.44, these are not atypical peak values. However, the values in Table 3.4 can be scaled to other values of R_s (in $\Omega\cdot$m) and L_s (in H$\cdot$m) as follows:

$$\begin{aligned} I_{sc}(R_s) &= I_{sc} \cdot (R_s(\Omega\cdot m)/1 \times 10^{-3}), \\ V_{oc}(R_s) &= V_{oc} \cdot (R_s(\Omega\cdot m)/1 \times 10^{-3}), \\ P(R_s) &= P \cdot (R_s(\Omega\cdot m)/1 \times 10^{-3})^2, \\ E(R_s) &= E \cdot (R_s(\Omega\cdot m)/1 \times 10^{-3})^2 \end{aligned} \tag{3.21a}$$

$$\begin{aligned} I_{sc}(L_s) &= I_{sc} \cdot (L_s(H\cdot m)/1 \times 10^{-11}), \\ V_{oc}(L_s) &= V_{oc} \cdot (L_s(H\cdot m)/1 \times 10^{-11}), \\ P(L_s) &= P \cdot (L_s(H\cdot m)/1 \times 10^{-11})^2, \\ E(L_s) &= E \cdot (L_s(H\cdot m)/1 \times 10^{-11}) \end{aligned} \tag{3.21b}$$

The rack size of 6' x 3' x 2' should bound the size of most equipment enclosures and hence the peak responses. For enclosures with more numerous seams, a worst case response for multiple seams would be if the single seam responses added constructively. That is, six seams would give six time the single seam response.

In spite of the fact that reasonably large values of R_s and L_s were used in the numerical calculations, one can see that the values of V,I,P and E in Table 3.4 are not large enough to cause damage. In the case of the resistive seam, the induced current and voltage is at most 8mA and 0.17V, while P and E are roughly 15 microwatts and 1 nanojoule, respectively. In the case of the inductive seam, the values of I_{sc} and V_{oc} are roughly 1mA and 0.35V, while P and E are about

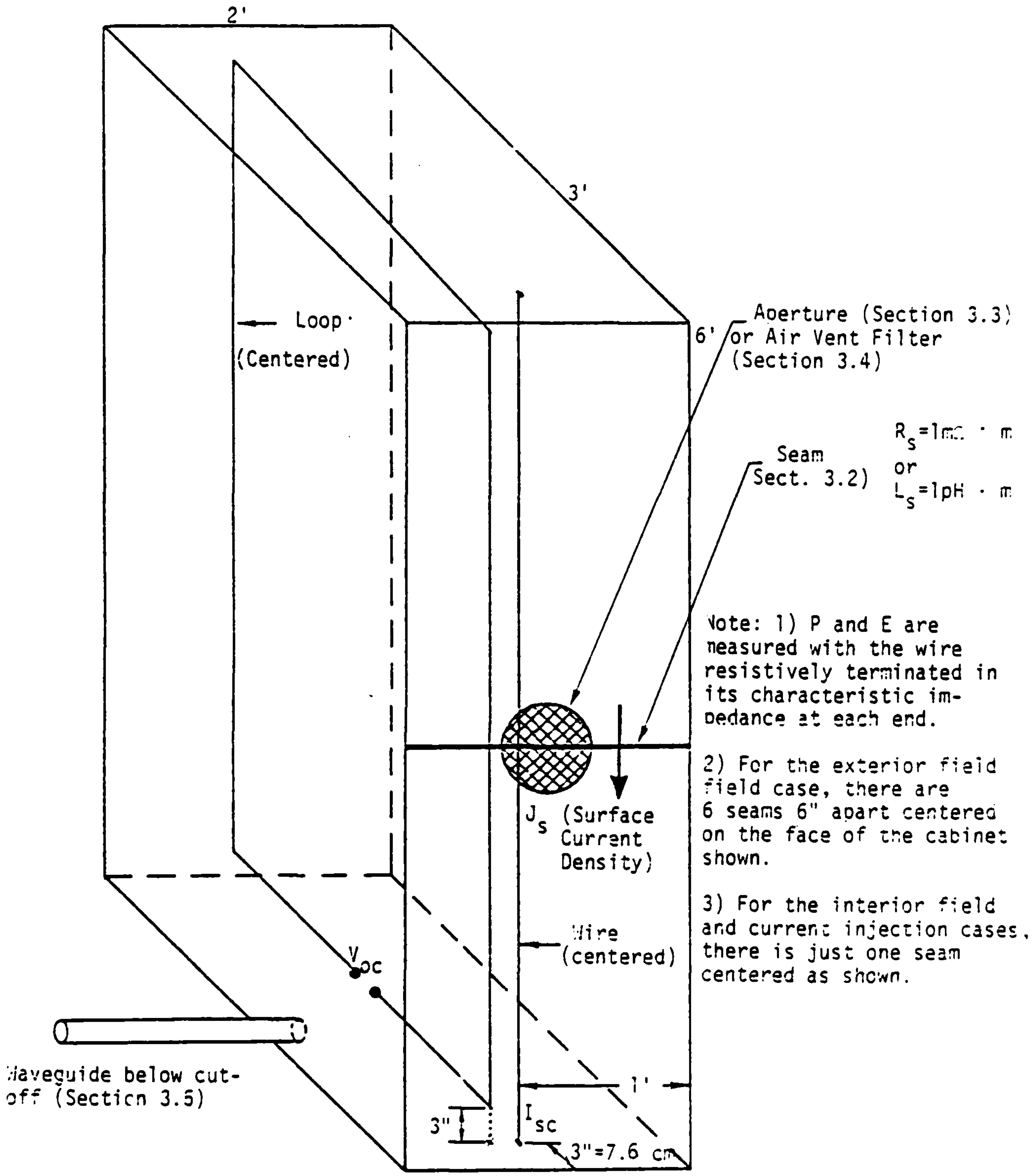


Figure 3.45 The Determination of I_{sc}, V_{oc}, P and E Inside a 6'H x 2'W x 3'D Cabinet with a Seam (etc.)

Table 3.4 Results of Numerical Three-Dimensional Finite Difference Solution of Maxwell's Equations for a 6'Hx2'Wx3'D Enclosure With A Resistive or Inductive Seam 2' Long

Table 3.4 Results of a Numerical Three-Dimensional Finite-Difference Solution of Maxwell's Equations for a 6'Hx2'Wx3'D Enclosure With A Resistive or Inductive Seam 2' Long

Type of Seam	Frequency of Current	Exterior Field: 50 kV/meter (Not Frequency Dependent - equation 2.4) J_s=332.5 Amperes/meter across the seam				Interior Field: 10A Current (Frequency Dependent - equation 2.2) J_s=3 Amperes/meter across the seam				Current Injection: 10A Current (Frequency Dependent - equation 2.2 J_s=5 Amperes/meter across the seam			
	MHz	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)
Resistive	0.5	0.008	0.17	1.45×10^{-5}	8.70×10^{-13}	-	-	-	-	-	-	-	-
Seam of	2					1.58×10^{-5}	1.31×10^{-3}	1.20×10^{-9}	$>1.50\times10^{-16}$	2.64×10^{-5}	2.18×10^{-3}	3.34×10^{-9}	$>4.18\times10^{-16}$
1mΩ-meter	10					3.17×10^{-5}	2.02×10^{-3}	1.20×10^{-9}	2.15×10^{-16}	5.28×10^{-5}	3.36×10^{-3}	3.34×10^{-9}	6.96×10^{-16}
Inductive	0.5	0.001	0.35	5.8×10^{-5}	2.03×10^{-13}	-	-	-	-	-	-	-	-
Seam of	2					1.01×10^{-5}	3.60×10^{-4}	3.01×10^{-11}	$>3.01\times10^{-18}$	1.68×10^{-5}	6.00×10^{-4}	8.35×10^{-11}	$>8.35\times10^{-18}$
10pH-meter	10					1.19×10^{-5}	1.91×10^{-3}	7.52×10^{-10}	7.52×10^{-16}	1.99×10^{-5}	3.19×10^{-3}	2.09×10^{-9}	2.09×10^{-15}

Notes:

1) The exterior field is not explicitely frequency dependent, whereas the interior and current-injected fields are (via equation 2.2).
2) The values for 0.5 MHz are not supplied here, since those available showed quite clearly that the trend above of decreasing values with decreasing frequency continues to hold at 0.5 MHz also. The 10 MHz values provide worst-case estimates, while those coupled with the values at 2 MHz give a clear indication of the trend with frequency.
3) The values of I_{sc} are for a 6' wire shorted to the top and bottom of the equipment cabinet and roughly 7.6 cm (3") from and pendicular to the seam. The wire radius is 5x10-4 meters. The values of V_{oc} are for a roughly 3' x 6' loop oriented with its plane perpendicular to the seam direction. The values of P and E are for the 6' wire again, but this time it is terminated at each end in a resistance equal to its characteristic impedance (see Figure 3.45). The Exterior Field case has 6 seams, while the others only have one seam.
4) The values of I_{sc} and V_{oc} scale linearly with inductance and resistance, while P and E scale quadratically with these parameters (see equations 2.2)

58 microwatts and 0.2 nanojoules, respectively. It can be seen from Reference 3.6 (Chapter 6) that these levels are highly unlikely to cause damage in even the most sensitive electronic equipment since the threshold for such damage is at worst typically 1-10 microjoules.

3.3.3 Shielding from Interior Fields

As with exterior (plane-wave) fields, the problem of interior (non-plane-wave) fields also had to be solved in two phases - the exterior problem and the interior problem. The exterior model was driven by a current given by (3.2) imposed on a wire 1 meter from the 6'H x 2'W x 3'D equipment cabinet as shown in Figure 3.1. From this exterior model, the (short-circuit) surface current density was obtained. It was then used to drive the interior model, as described in the previous section, and thereby again determine I_{sc}, V_{oc}, P and E. These results are shown in Table 3.4. Although these are time-domain results, they are "frequency-dependent" (as Table 3.4 shows) due to the frequency dependence of the time-domain expression for the damped sinusoidal current of (3.2). Here, again, the sames values of R_s and L_s were used as in the previous section, and the results can also be scaled per (3.23).

As can be seen from the results in Table 3.4, the values of I_{sc} and V_{oc} are roughly 2 to 3 orders of magnitude smaller than those for the external field, while P and E are roughly 3 to 6 orders of magnitude smaller. Reference 3.6 again implies that these levels are well below the threshold of damage.

3.3.4 Shielding from Cable Currents (Current Injection)

The numerical solution here proceeds exactly as described in the previous two sections. The driving current for the exterior problem here, however, is the same one used in the previous section, but directly injected onto the cabinet face containing the seam (one foot from the seam). The resulting exterior surface current across the seam was then again used to drive the interior model.

As before, the values for R_s and L_s and the results can be found in Table 3.4. Because the results here are only roughly 1.6-2.8 times larger than those for the interior field case (because the results scale with the surface current density similar to the way they do for R_s and L_s), the levels are, again well below the damage thresholds.

3.3.5 Summary

As can be seen from the results presented in Section 3.3.2 - 3.3.4, the comment of Section 3.3.1 is borne out: properly designed and installed seams and joints easily provide the required amount of shielding to ensure that no damage will occur in even the most sensitive electronic equipment because the energy values in Table 3.4 are well below the typical worst-case threshold for damage of 1-10 microjoules.

3.4 Openings in Volume Shields (Apertures)

3.4.1 Background

Just as an enclosure cannot be realistically manufactured out of a single

monolithic piece of metal, thus giving rise to seams and joints, neither can it be manufactured without any openings. These openings facilitate access, viewing, lighting, and ventilation. Because such openings (or apertures) can also be the entry points into the enclosure for large amounts of EMP energy, it is necessary either to keep them as small as possible or to additionally harden them by the use of covering materials such as wire screen, or honeycomb. This latter case is discussed in the next section, while this section discusses ways of estimating the amount of EM leakage through openings which cannot be covered with such hardening materials.

The earliest applicable work on this subject is that by Bethe [3.18] where he investigated the coupling of EM energy into and out of a cavity by means of a small hole. In Bethe's "small hole" theory, it is shown that (to the lowest, or zeroth order) the effects of the aperture can be represented by a magnetic dipole lying in the plane of the aperture and an electric dipole perpendicular to the aperture. Then, the fields on the side of the aperture opposite the incident field can be obtained from the dipole moments of these two dipoles. Further, these moments can, in turn, be obtained from the short-circuit electric and magnetic fields that would exist at the location of the aperture in the absence of the opening. The proportionality factors in these latter relationships are known as the electric and magnetic polarizabilities, and, in general, they are dyads (tensors of order 2). In most applications, however, the electric polarizability has only one component ($\alpha_{e,zz}$) while the magnetic polarizability has two ($\alpha_{m,xx}$ and $\alpha_{m,yy}$). This is basically due to the fact that both the electric dipole moment and short-circuit electric field are perpendicular to the hole, while the magnetic dipole moment and its direction are not only a function of the tangential short-circuit magnetic field (and its direction) but also of the shape of the hole (and the direction of its largest dimension).

The next order approximation can be found fully discussed in Van Bladel [3.19], however, these higher order multiple moments are far too complicated for the simple engineering design approach that we propose to present here. Other work and other approaches can be found not only in [3.21], but also in [3.20].

It should be noted that the "small hole" theory is only applicable to "small" holes, namely, those apertures whose largest dimension is approximately less than or equal to one-tenth of a wavelength. For larger apertures, other techniques must be used, for example, the Kirchhoff-Huygens approximation, wherein the field in the aperture is just taken to be the incident field. Additionally, there is the problem of enclosure geometry to consider ! The fields predicted by either the Bethe or the Kirchhoff-Huygens methods are reasonable approximations for an aperture in an infinite flat conducting sheet, but are <u>not</u> adequate far from the aperture for any type of enclosure. Consequently, either of these two methods can be used to specify the fields at the inside surface of an aperture in an enclosure. These fields can then, in turn, drive a numerical three-dimensional finite-difference solution of Maxwell's equations [3.12], as has been described earlier herein. It is just this approach which will be used here. The polarizabilities will be used to parameterize the results, and, consequently, to allow the results to be "scaled" to other aperture sizes and shapes. The problem of the inapplicability of the polarizability representation will not arise here due to the frequencies considered and the basic enclosure size (6'H x 2'W x 3'D). For 0.5, 2, and 10 MHz, one-tenth of a wavelength is 60 m (196.85'), 15 m (49.21'), and 3 m (9.84'), respectively. Obviously, the

enclosure considered here will not physically permit such aperture dimensions. Even at 100 MHz one-tenth of a wavelength is only 0.3 m (0.98'), and typical cabinet louvers are of roughly this size in their largest dimension. Thus the "small hole" theory is sufficient to the needs considered herein.

Expressions for the polarizability of some simple common shapes can be found in Table 3.5 while plots of the polarizability for these and some other simple shapes can be found in Figures 3.46 - 3.49. As can be seen from these figures, the polarizabilily seems to vary quite widely with not only the width-to length ratio, but also with shape. However, if the polarizability is first "properly" normalized by the area of the aperture [3.23], then one finds that this "normalized polarizability" is not strongly dependent upon the shape of the aperture, but rather depends almost entirely upon the width-to-length ratio w/ℓ. This is illustrated in Figures 3.50 - 3.53. Except for the cross-shaped aperture and magnetic polarizability, the plots of normalized polarizability are very similar for the various shapes. It should be noted that because the results for the ellipse and the rectangle with the rounded ends are almost identical in the case of Figure 3.52, the former is not shown here.

The above illustrated shape independence brings to mind the question of whether it is possible (much as for diffusion) to present a shape independent curve for the various polarizabilities. Figures 3.50 - 3.52 would appear to indicate that it is. However, the question has not yet been theoretically resolved. All that is known on the subject is that:

1) Latham [3.24] has shown that for an elliptical aperture

$$(P/A^2)\,\alpha_{e,zz} = 4/3\pi \qquad (3.22)$$

where P is the perimeter and A is the area. Note that this expression <u>does not</u> depend upon the eccentricity of the ellipse.

2) Latham [3.24] also noted that for a rectangular aperture

$$(P/A^2)\,\alpha_{m,yy} \doteq (\pi/8)\cdot(1+0.55\cdot w/\ell) \qquad (3.23)$$

where w is the width (the smaller dimension) and ℓ is the length of the aperture. When $(w/\ell) < 0.5$, this is accurate to better than 3%.

3) Jaggard and Papas [3.44] have presented the following bounds simple apertures with small eccentricity $\left[e = \sqrt{1-(w/\ell)^2} \ll 1\right]$:

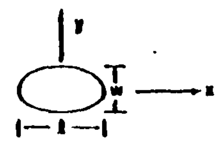
$$\frac{16}{3\pi}\left(\frac{A^2}{P}\right) \leq \alpha_e \leq \frac{8}{3}\left(\frac{A}{\pi}\right)^{3/2}, \qquad (3.24)$$

$$\frac{16}{3}\left(\frac{A}{\pi}\right)^{3/2} \leq \left(\frac{\alpha_{m,xx}+\alpha_{m,yy}}{2}\right) \leq \frac{16}{3}\left(\frac{P}{2\pi}\right)^{3} \qquad (3.25)$$

Table 3.5 Aperture Polarizabilities for Some Common Shapes

Shape	$\alpha_{e,zz}$	$\alpha_{m,xx}$	$\alpha_{m,yy}$	Ref.
Circle (d = Diameter)	$\frac{1}{12} d^3$	$\frac{1}{6} d^3$	$\frac{1}{6} d^3$	10
Ellipse*	$\frac{\pi}{24} \frac{w^2 \ell}{E(m)}$ *	$\frac{\pi}{24} \frac{\ell^3 m}{K(m) - E(m)}$ *	$\frac{\pi}{24} \frac{\ell^3 m}{(\ell/w)^2 E(m) - K(m)}$ *	10
Narrow Ellipse ($w \ll \ell$)	$\frac{\pi}{24} w^2 \ell$	$\frac{\pi}{24} \frac{\ell^3}{\ln(4\ell/w) - 1}$	$\frac{\pi}{24} w^2 \ell$	10
Narrow Slit ($w \ll \ell$)	$\frac{\pi}{16} w^2 \ell$	$\frac{\pi}{24} \frac{\ell^3}{\ln(4\ell/w) - 1}$	$\frac{\pi}{16} w^2 \ell$	10
Square of side ℓ	$0.1137\ \ell^2$	$0.259\ \ell^3$	$0.259\ \ell^3$	21
Rectangle, w/ℓ=0.75	$0.0731\ \ell^3$	$0.2096\ \ell^3$	-	21
Rectangle, w/ℓ=0.50	$0.0370\ \ell^3$	$0.1575\ \ell^3$	-	21
Rectangle, w/ℓ=0.20	$0.0070\ \ell^3$	$0.0906\ \ell^1$	-	21
Rectangle, w/ℓ=0.10	$0.0019\ \ell^3$	$0.0645\ \ell^3$	-	21

*Ellipse eccentricity $e = \sqrt{1 - (w/\ell)^2}$.



K and E are the complete elliptic integrals of the first and second kind, $m = e^2$ (See [3.22] 17.3.33-17.3.36, pp. 591-592; also Table 17.1, pp. 608-609)

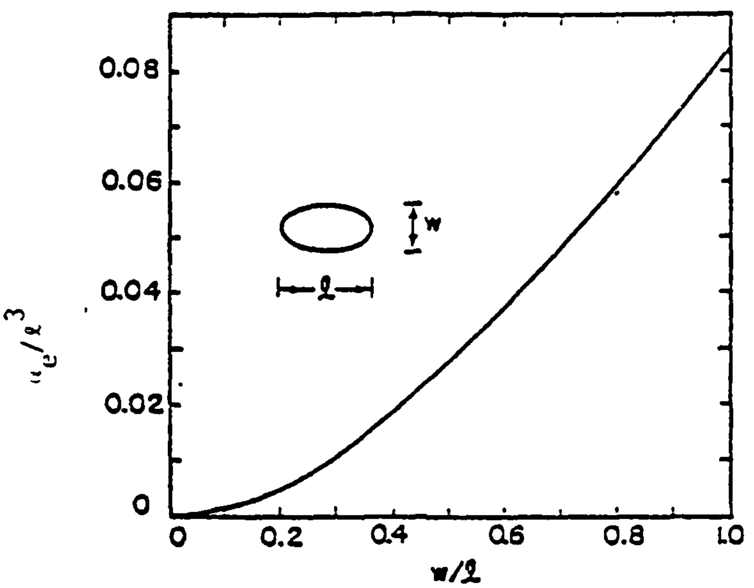


Figure 3.46 Normalized Electric (Imaged) Polarizability of an Elliptical Aperture [3.10]

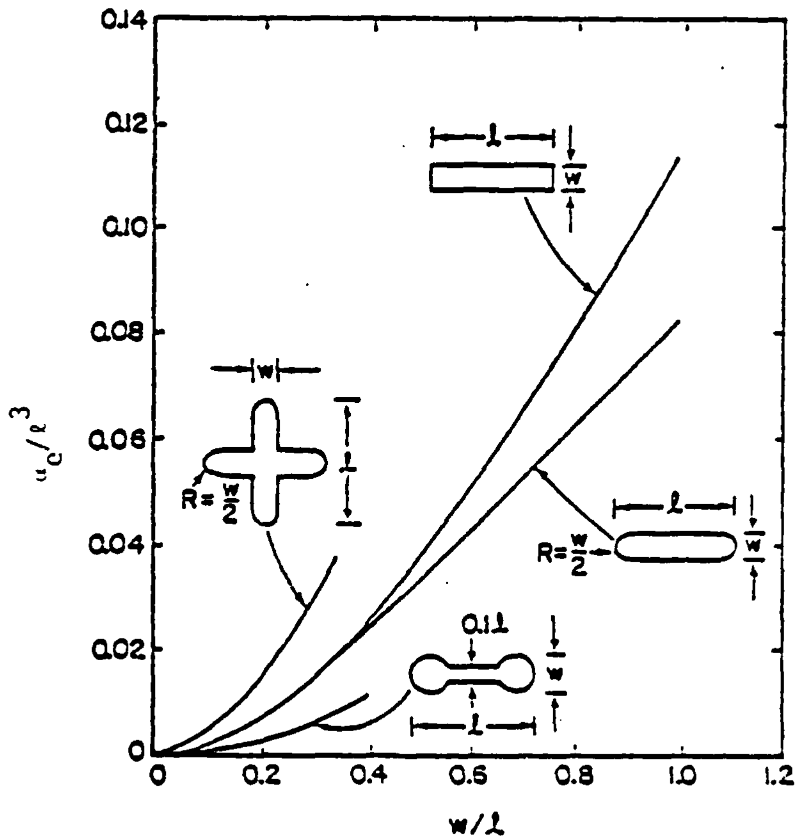


Figure 3.47 Normalized Electric (Imaged) Polarizabilities for Four Aperture Shapes [3.10]

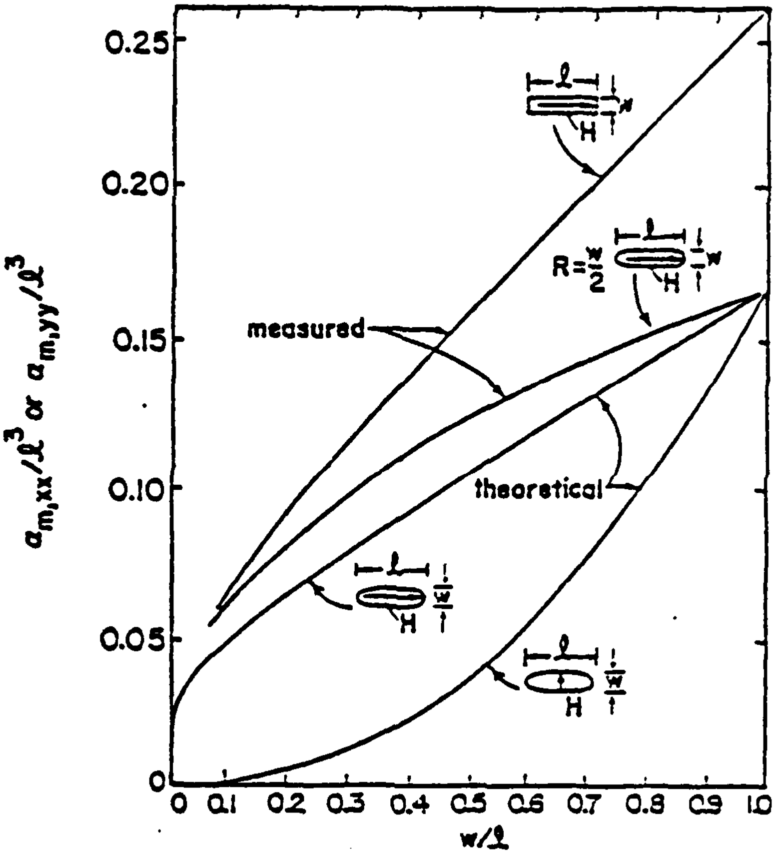


Figure 3.48 Normalized Magnetic (Imaged) Polarizabilities for Elliptical, Rectangular, and Rounded Rectangular Apertures [3.10]

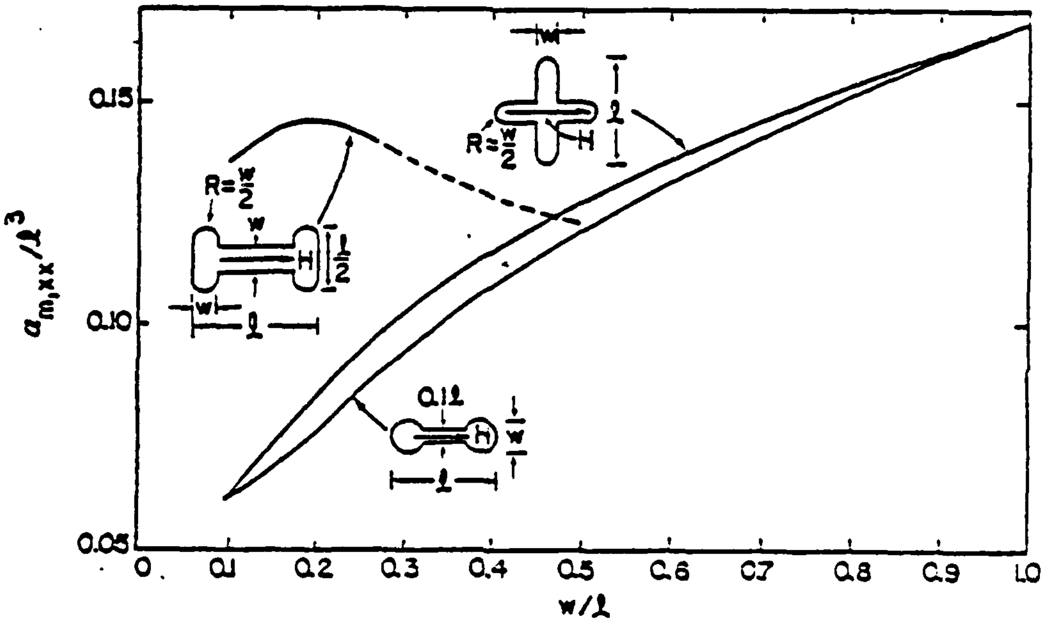


Figure 3.49 Normalized Magnetic (Imaged) Polarizabilities for Three Aperture Shapes [3.10]

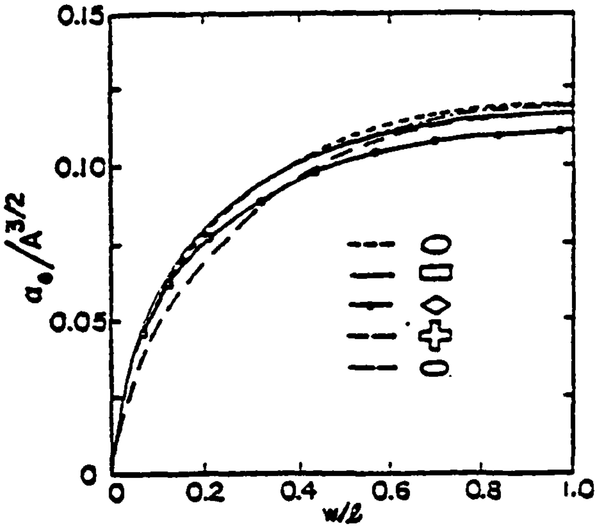


Figure 3.50 Normalized Electric (Imaged) Polarizabilities of Various Apertures [3.10]

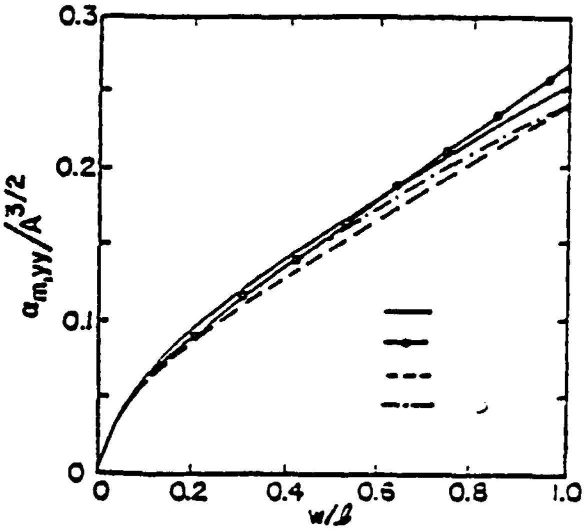


Figure 3.51 Normalized Magnetic (Imaged) Polarizabilities of Various Apertures [3.10]

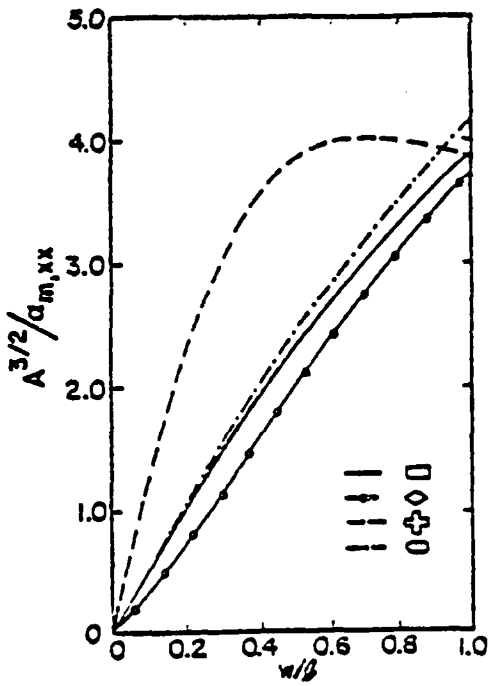


Figure 3.52 Normalized Reciprocal Magnetic (Imaged) Polarizabilities of Various Apertures [3.10]

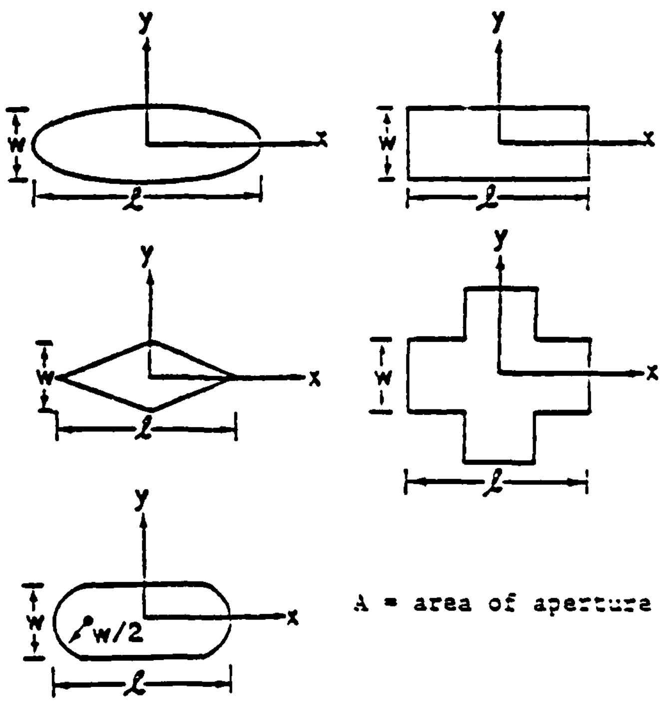


Figure 3.53 Definition of the Dimensions of the Various Apertures [3.10]

Lee [3.10] also gives expressions for some typical hatch apertures (see Figure 3.54), both ungasketed and gasketed. These expressions can be found in Tables 3.6 and 3.7, respectively, and can be used to calculate the polarizabilities of these apertures for the purpose of "scaling" the results presented in the following sections.

3.4.2 Shielding from Exterior Fields

As was the case with seams, the exterior problem had to first be solved, and then, the results from that, along with the polarizabilities, used to drive the interior problem. This, again, allowed calculation of I_{sc}, V_{oc}, P and E. The enclosure, aperture, wire, and loop dimensions and locations are all shown in Table 3.8 and Figure 3.45. The results can be "scaled" to other sizes of circular holes or even approximately to other hole shapes as follows:

1) Calculate $\alpha_{e,zz}$, $\alpha_{m,xx}$, $\alpha_{m,yy}$, and A for the desired aperture, then calculate

$$
\begin{aligned}
X_1 &= (\alpha_{e,zz}/A^{3/2}) \,/\, (1.20 \times 10^{-1}) \\
X_2 &= (\alpha_{m,yy}/A^{3/2}) \,/\, (2.39 \times 10^{-1}) \\
X_3 &= (A^{3/2}/\alpha_{m,xx}) \,/\, (4.18) \\
X &= \text{Maximum of } X_1, X_2, X_3.
\end{aligned}
\tag{3.26}
$$

2) Next, scale the results from Table 3.8 using

$$
\begin{aligned}
I_{sc}(\alpha) &= I_{sc} \cdot X, \\
V_{oc}(\alpha) &= V_{oc} \cdot X, \\
P(\alpha) &= P \cdot X^2, \\
E(\alpha) &= E \cdot X^2.
\end{aligned}
\tag{3.27}
$$

The values in Table 3.8, being for a reasonably large hole (6" diameter), are expected, in some sense, to be worst-case results. Consequently, it can be seen that the energy here is still roughly a factor of 10^2 below the damage thresholds set forth in [3.6]. The circuit voltage of 296V could damage some dielectric sensitive devices.

3.4.3 Shielding from Interior Fields

The numerical calculations here proceed very similarly to those described in the previous section and in Section 3.3.3 on seams. The values of I_{sc}, V_{oc}, P and E so determined can be found in Table 3.8, and can be, again, scaled per (3.26) and (3.27).

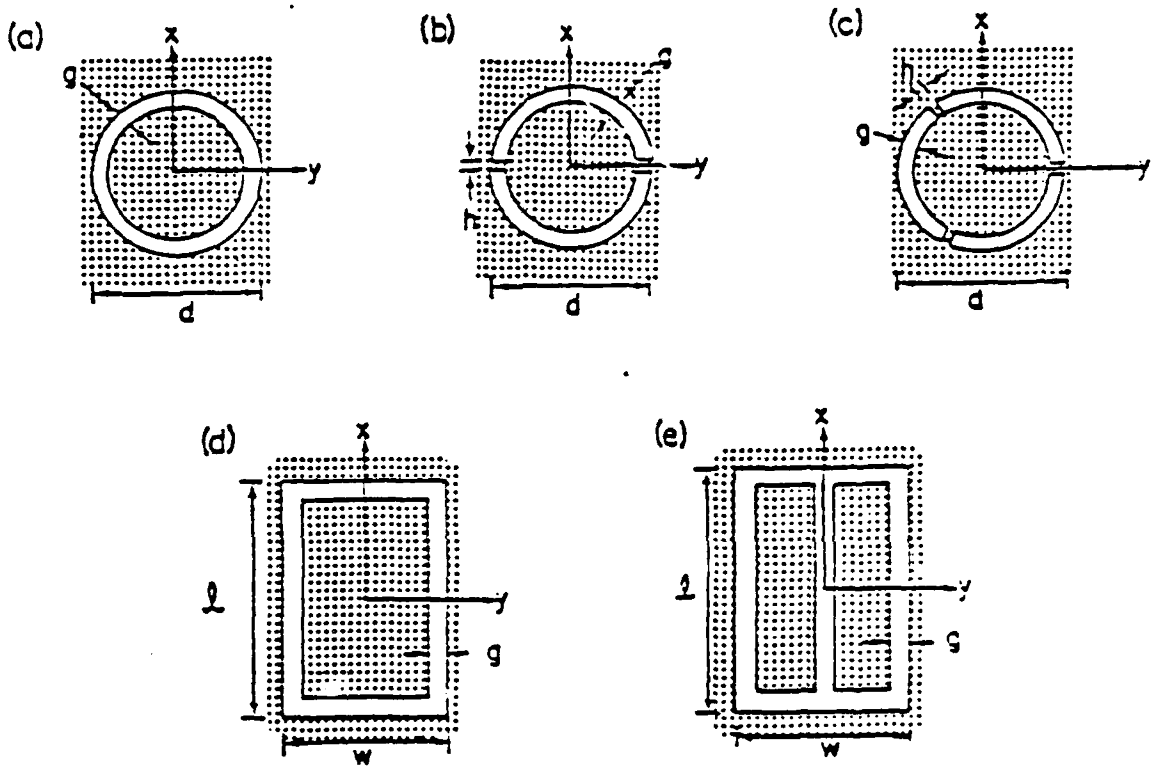


Figure 3.54 Typical Hatch Apertures [Note the presence of hinges and latches of dimension "h" in (b) and (c)] [3.10]

Table 3.6 Polarization of Some Typical Ungasketed Hatch Apertures [3.10]

Aperture in Fig. 3.54	α_e	$\alpha_{m,xx}$	$\alpha_{m,yy}$
(a)	$\frac{\pi^2}{32}\frac{d^3}{\ln(16\,d/g)-2}$	$\frac{\pi^2}{16}\frac{d^3}{\ln(16\,d/g)-2}$	$\frac{\pi^2}{16}\frac{d^3}{\ln(16\,d/g)-2}$
(b)	$\frac{\pi^2 d^3}{16\Omega}\frac{\pi^2\mu\varepsilon}{\pi^2\mu\varepsilon+128h/(\pi\Omega d g^2)}$	$\frac{\pi^2 d^3}{8\Omega}\left[1-\frac{8/\pi^2}{1+\Omega g^2/(8\pi d h)}\right]$	$\frac{\pi^2}{16}\frac{d^3}{\ln(16\,d/g)-2}$
(c)	$\frac{\pi^2 d^3}{16\,\Omega}\frac{\pi^2\mu\varepsilon}{\pi^2\mu\varepsilon+192h/(\pi\Omega d g^2)}$	$\frac{\pi^2 d^3}{8\Omega}\left[1-\frac{27/(4\pi^2)}{1+9\Omega g^2/(64\pi d h)}\right]$	$\frac{\pi^2 d^3}{8\Omega}\left[1-\frac{27/(4\pi^2)}{1+9\Omega g^2/(64\pi d h)}\right]$
(d)	$\frac{\pi}{4}\frac{\ell^2 w}{(1+\ell/w)\ln[4(\ell+w)/g]}$	$\frac{\pi}{12}\frac{\ell^3[1+3(w/\ell)]}{\ln[4(\ell+w)/g]}$	$\frac{\pi}{12}\frac{w^3[1+3(\ell/w)]}{\ln[4(\ell+w)/g]}$
(e)	$\frac{\pi}{4}\frac{\ell^2 w}{(1+\ell/w)\ln[4(\ell+w)/g]}$	$\frac{\pi}{24}\frac{\ell^3[8/3+7(w/\ell)+2(w/\ell)^2]}{\ln[4(\ell+w)/g]}$	$\frac{\pi}{12}\frac{w^3[1+3(\ell/w)]}{\ln[4(\ell+w)/g]}$

Note: $\Omega = 2[\ln(16d/g) - 2]$

Table 3.7 Polarizabilities of Some Typical Gasketed Hatch Apertures [3.10]

Aperture in Fig. 3.54	$\alpha_e(s)$	$\alpha_{m,xx}(s)$	$\alpha_{m,yy}(s)$
(a)	$\frac{\pi^2 s\varepsilon}{16} \frac{d^4}{2G_c + sC_c}$	$\frac{\pi^2}{4\mu} \cdot \frac{d^2}{1/L_c + sG_c}$	$\frac{\pi^2}{4\mu} \cdot \frac{d^2}{1/L_c + sG_c}$
(b)	$\frac{\pi^2 s\varepsilon}{16} \cdot \frac{d^4}{2G_c + sC_c + 2/sL_h}$		$\frac{\pi^2}{4\mu} \cdot \frac{d^2}{1/L_c + sG_c}$
(c)	$\frac{\pi^2 s\varepsilon}{16} \cdot \frac{d^4}{2G_c + sC_c + 3/sL_h}$		
(d)	$\frac{s\varepsilon\ell^2 w^2}{G + sC}$	$\frac{1}{1 + sL_x G_x} \alpha_{m,xx}(0)$	$\frac{1}{1 + sL_y G_y} \alpha_{m,yy}(0)$
(e)	$\frac{s\varepsilon\ell^2 w^2}{G + sC}$	$\frac{1}{1 + s(L_x + L_a)G'_x} \alpha_{m,xx}(0)$	$\frac{1}{1 + sL_y G_y} \alpha_{m,yy}(0)$

<u>Notes:</u> (i) Δ = gasket thickness; σ = gasket conductivity.

(ii) The static polarizabilities $\alpha_{m,xx}(0)$ and $\alpha_{m,yy}(0)$ in the table entries are those of the corresponding hatch aperture without gasket found in Table 3.6.

(iii) Constants: $G = 2\sigma\Delta(\ell + w)/g$; $C = 2\varepsilon\Omega(\ell + w)/\pi$; $\Omega = 2\ln[4(\ell + w)/g]$; $L_x = \mu\pi\ell(1 + 2w/\ell)/8\Omega$;
$L_y = \mu\pi w(1 + 2\ell/w)/8\Omega$; $G_x = \sigma\Delta\ell/g$; $G'_x = G_x/(1 + w/3\ell)$; $L_a = (\pi\mu\ell/24\Omega)w^2/\ell^2$;
$G_y = \sigma\Delta w/g$; $G_c = \pi\sigma\Delta d/2g$; $L_c = \mu d/[4\ln(16d/g) - 8]$; $L_h = \mu\pi g^2/(64h)$;
$C_c = 2\varepsilon d[\ln(16d/g) - 2]$.

Table 3.8 Results of a Numerical Three-Dimensional Finite-Difference Solution of Maxwell's Equations for a 6'H x 2'W x 3'D Enclosure with a 6" Diameter Circular Aperture

Frequency of Current (MHz)	Exterior Field: 50 kV/meter (Not Frequency Dependent - equation 2.4) J_s = 132.5 Amperes/meter across the Aperture				Interior Field: 10A current (Frequency Dependent - equation 2.2) J_s = 3 Amperes across the aperture				Current Injection: 10A current (Frequency Dependent - equation 2.2) J_s = 5 Amperes/meter across the aperture			
	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)
0.5	0.2	296	3.19	1.74×10^{-8}	-	-	-	-	-	-	-	-
2.0					1.84×10^{-3}	3.89×10^{-1}	1.25×10^{-6}	1.35×10^{-13}	3.06×10^{-3}	6.48×10^{-1}	3.48×10^{-6}	3.76×10^{-13}
10					2.54×10^{-3}	1.87	3.16×10^{-5}	4.00×10^{-12}	4.08×10^{-3}	3.12	8.77×10^{-5}	1.11×10^{-11}

Notes:

1) The exterior field is not explicitely frequency dependent, whereas the interior and current-injected fields are (via equation 2.2)

2) The values for 0.5 MHz are not supplied here, since those available showed quite clearly that the trend above of decreasing values with decreasing frequency continues to hold at 0.5 MHz also. The 10 MHz values provide worst-case estimates, while those coupled with the values at 2 MHz give a clear indication of the trend with frequency.

3) The values of I_{sc} are for a 6' wire shorted to the top and bottom of the equipment cabinet and roughly 7.6 cm (3") from (and centered behind) the aperture. The wire radius is 5×10^{-4} meters. The values of V_{oc} are for a roughly 3' x 6' loop oriented with its plane perpendicular to the plane of the aperture. The values of P and E are for the 6' wire again, but this time it is terminated at each end in a resistance equal to its characteristic impedance (see Figure 3.45).

4) The values of I_{sc} and V_{oc} scale linearly with polarizability, while P and E scale quadratically (see (3.26 and (3.27) the exact rule in this case).

5) Here $\alpha_{e,zz} = 2.95 \times 10^{-4}$ m^3, $\alpha_{m,xx} = \alpha_{m,yy} = 5.90 \times 10^{-4}$ m^3, and $A = 1.82 \times 10^{-2}$, hence $A^{3/2} = 2.46 \times 10^{-3}$ and $(\alpha_{e,zz}/A^{3/2}) = 1.20 \times 10^{-1}$, $(\alpha_{m,yy}/A^{3/2}) = 2.39 \times 10^{-1}$, $(A^{3/2}/\alpha_{m,xx}) = 4.18$.

The values in Table 3.8 again show that the power and energy are at levels far below the damage thresholds [3.6]. The short-circuit currents are at most a few milliamperes and should generally pose no problem, as is also the case for the open-circuit voltages of a few volts.

3.4.4 Shielding from Cable Currents (Current Injection)

It should be clear from the previous two sections, along with Section 3.3 on seams, exactly how the numerical calculations proceed here. Table 3.8 contains the results of these calculations, namely I_{sc}, V_{oc}, P and E, which can again, be scaled via equations (3.26) and (3.27). The magnitude of these results are such that the comments of Section 3.4.3 apply here also. No problems appear to be predicted.

3.4.5 Summary

The results of Sections 3.4.2 - 3.4.4 clearly show that the energy levels are all well below the damage thresholds [3.6]. For the interior and current-injected fields, it is also the same as regards I_{sc}, V_{oc}, and P (except for possibly CMOS devices). In the exterior field case, however, the large peak currents, voltages and powers may quite probably cause damage in some equipment. The solutions are: 1) harden the circuits, 2) don't put large apertures on external equipment, and 3) if such apertures are necessary, harden them with such c vering as wire mesh, and so on. These latter materials are, in fact, the topic of the next section.

3.5 Air Vents

3.5.1 Background

As was pointed out at the beginning of Section 3.4.1, an enclosure cannot generally be utilized without any openings. Such openings facilitate access, viewing, natural lighting, ventilation, and entry for cables. Some of these openings, such as hatches and doors, can be covered (closed) for protection, while others, for example, ventilation openings, cannot. Those openings in this latter category, however, can often be covered by materials such as wire screen and metal honeycomb in order to provide some additional hardening to EMP energy without restricting their use.

The electric field ($\vec{E}_t$) on the inside surface of an air vent cover can be expressed (in the frequency domain) as [3.25 - 3.27]

$$\vec{E}_t(\omega) = \vec{\vec{Z}}_T(\omega) \cdot \vec{J}_s(\omega) \tag{3.28a}$$

where $\vec{J}_s(\omega)$ is the surface current density on the outside surface of the air vent cover panel, and $\vec{\vec{Z}}_T(\omega)$ is the surface transfer impedance dyad (tensor of rank 2). In the case of isotropic surfaces, Z_T is just a scalar quantity (a single quantity), while for anisotropic surfaces $\vec{\vec{Z}}_T$ is a dyadic expression which is represented in component form by a 3 x 3 matrix. The dyadic nature

of $\bar{\bar{Z}}_T$ in the latter case is required by the fact that $\bar{E}_t$ and $\bar{J}_s$ may not "point" in the same direction due to the anisotropic nature of the surface. For the surfaces considered here, the isotropic assumption will suffice, and, consequently, we have that

$$\bar{E}_t(\omega) = Z_T(\omega)\ \bar{J}_s(\omega). \tag{3.28b}$$

Generally, such surfaces as wire screen and metallic honeycomb are inductive and hence

$$Z_T(\omega) = j\omega L_T, \tag{3.29}$$

where j is $\sqrt{-1}$, ω is the angular frequency, and L_T is the surface transfer inductance. In the time domain, then (3.28) and (3.29) combined become

$$\bar{E}_t(t) = L_T\ \frac{\partial \bar{J}_s(t)}{\partial t}\ . \tag{3.30}$$

Therefore, given the surface current density $\bar{J}_s(t)$ on the outside surface of the air vent cover and the surface tranfer inductance L_T, one can determine the electric field $\bar{E}_t(t)$ "transmitted" to the inside surface of the air vent cover. This electric field can, in turn, be used to "drive" a numerical three-dimensional finite-difference solution of Maxwell's equations inside of the enclosure. $\bar{J}_s(t)$, as before, is obtained by solving the "exterior problem" using similar numerical techniques.

Although a reasonable amount of effort has been directed toward the analytical determination of the surface transfer impedance of braided cables [3.28, 3.29] and planar wire mesh [3.29], little such effort has been directed at other planar surfaces such as metallic honeycomb. Except for the aforementioned work and that of Casey [3.30 - 3.31] on composite surfaces and mesh-loaded circular apertures, of Bereuter [3.32] on metallic honeycombs, and of Rosich et al [3.25 - 3.27] on a general dyadic expression for electrically thin planar surfaces of infinite extent, little of direct relevance here could be found in the literature. Some data from typical shielding effectiveness measurements of wire mesh [3.33 - 3.35] and metallic honeycomb [3.35] are available. Also analytic treatments for wire mesh [3.36 - 3.38] and metallic honeycomb [3.37 - 3.38] using Bethe's polarization theory [3.18], Schelkunoff Theory [3.5] and Rayleigh Theory [3.39, 3.40], can be found. However, none of these exist in the form required here, namely as surface transfer impedances.

Little theoretical work is available on the surface transfer of wire mesh and metallic honeycomb (except for that referenced in [3.29] on wire mesh), and the only experimental results in this format are those of Madle [3.13] for honeycomb and Lowell [3.14] for wire mesh, honeycomb, gaskets, and seams. However, there are a reasonable number of results in the literature which characterize various surfaces in terms of transmission and reflection coefficients. These, coupled with the work of Rosich et al. [3.25 - 3.27], permit analytic computation of L_T. Although a complete discussion of this method can be found [3.25 - 3.27], some analytical [3.27] and experimental [3.14] results can be found compared in Figures 3.55 and 3.56, while the associated physical dimensions and analytically predicted values of L_T can be found in Tables 3.9 and 3.10.

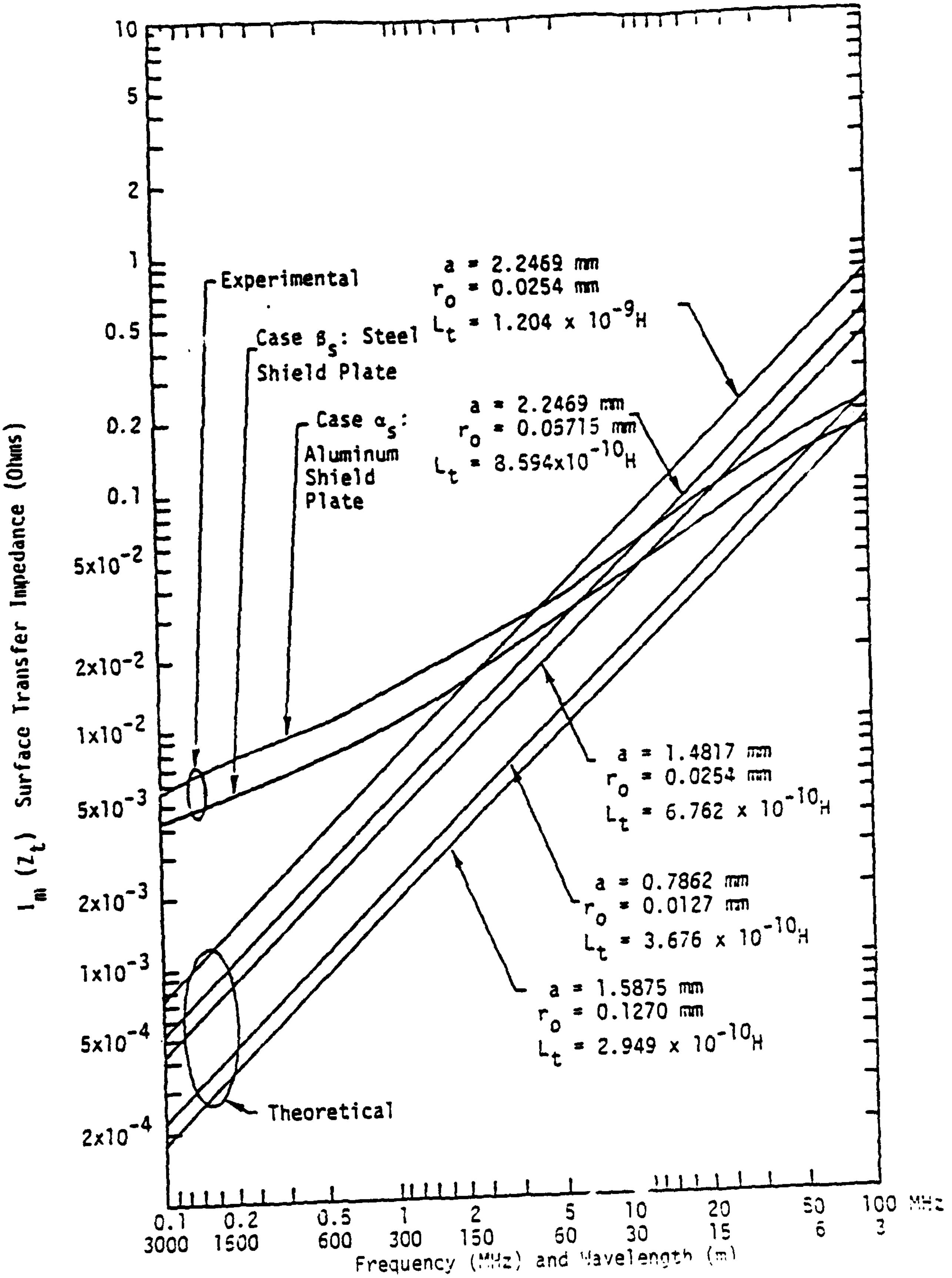


Figure 3.55 The Surface Transfer Impedance of Planar Square Bonded Wire Mesh (Analytical and Experimental) (Note that Z is for a Single-Layer Mesh; For an n-Layer Mesh: $Z_n = \frac{1}{n} Z_1$) [3.27]

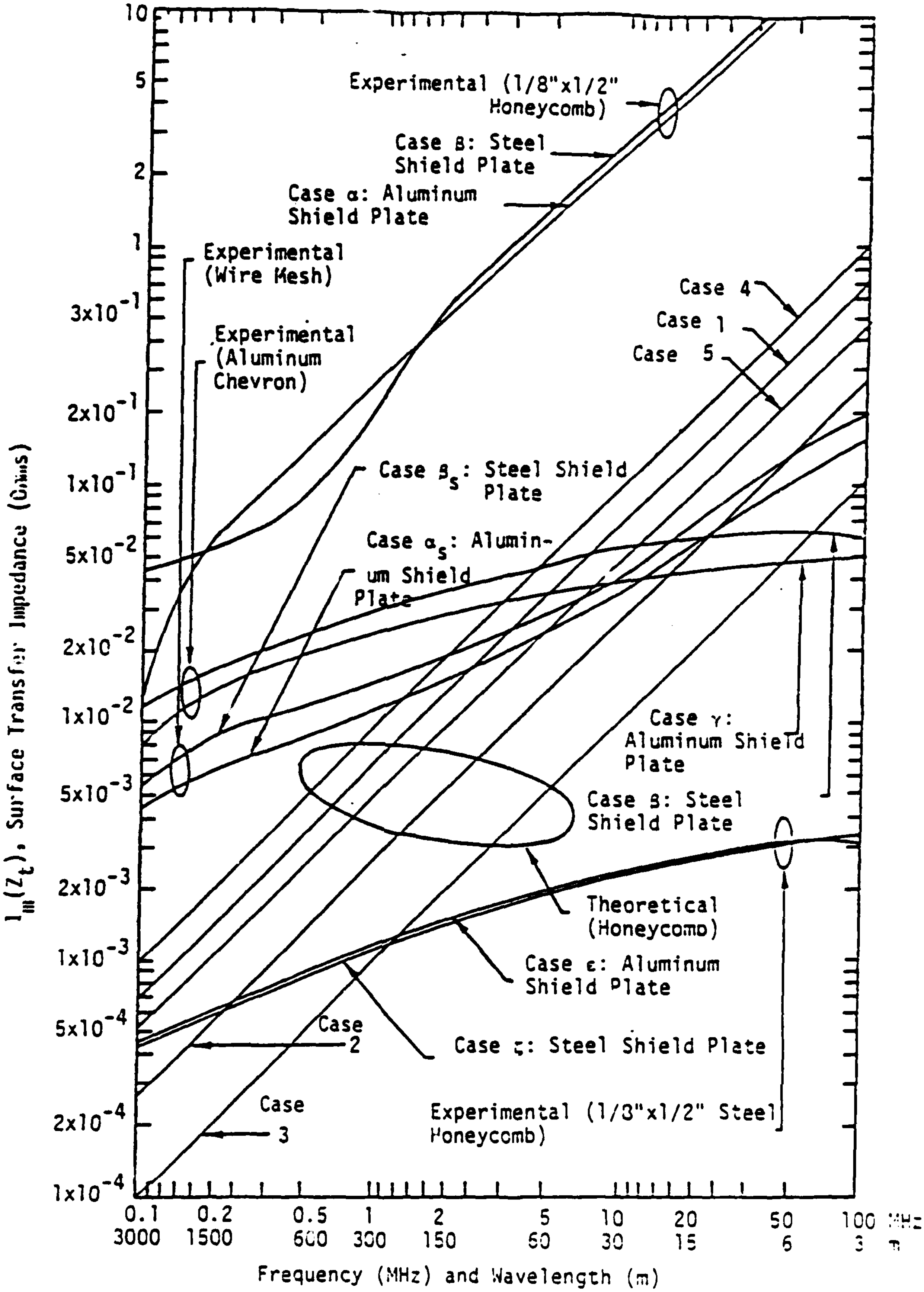


Figure 3.56 The (Analytical and Experimental) Surface Transfer Impedance of Metallic Honeycomb [3.27](See Table 3.10 for the Values of W, T, t_f, and L_T)

Table 3.9 Various Sizes of Wire Mesh and Their Values of L_T

Case:	1	2	3	4	5
a(mm):	0.7862	1.4817	2.2469	2.2469	1.5875
r_o(mm):	0.0127	0.0254	0.0254	0.05715	0.1270
No.Openings/in.:	-32	-17	-11	-11	16
L_T(H.):	3.676×10^{-10}	6.762×10^{-10}	1.204×10^{-9}	8.594×10^{-10}	2.949×10^{-10}

Note that (Ref. [3.27])

$$Z_T = j \left|-\frac{120\pi a}{1000\lambda} \ln \left|1 - \exp(-2\pi r_o/a)\right|\right| = j\omega \left|\frac{-6a}{100c} \ln \left|1 - \exp(-2\pi r_o/a)\right|\right|$$

$$= j\omega L_T ,$$

where

a = the wire-center to wire-center distance for a single opening in the wire mesh; mm. implies the value listed is in millimeters,

r_o = the radius of the wire; mm. implies the value listed is in millimeters,

λ = the wavelength,

$\omega = 2\pi f$,

Z_T = the surface transfer impedance,

L_T = the surface transfer inductance; H. implies the value listed is in Henries,

c = the velocity of light.

Table 3.10 Various Sizes of Metallic Honeycomb and Their Values of L_T

Case:	1C	2C	3C	4C	5C
W(in.):	1/8	1/8	1/8	3/16	3/16
T(in.):	1/2	3/4	1	3/4	1
t_f(in.):	.0015	.0015	.0015	.0020	.0020
L_T(H.):	1.102×10^{-9}	4.364×10^{-10}	1.735×10^{-10}	1.654×10^{-9}	8.911×10^{-10}

Notes: $Re(Z_T)$ is identically zero.

Z_T = Surface transfer impedance.

W = Hexagonal cell width between two opposite field faces.

T = Honeycomb panel thickness.

t_f = Honeycomb foil thickness.

a = Radius of (model) circular holes.

d = Center-to-center (model) hole spacing.

ℓ = Half-thickness of (model) panel.

L_T = Surface transfer inductance.

3.5.2 Shielding from Exterior Fields

As was noted in Section 3.5.1, the exterior problem is solved first, and then, its results used to drive the interior problem using (3.30). From the solution to the interior problem, I_{sc}, V_{oc}, P and E are obtained. The enclosure and its associated dimensions can be found in Figure 3.45, while the results can be found in Table 3.11. The results in the table can be scaled to other hole shapes and filter materials (characterized by their surface transfer inductance L_T) as follows:

$$\begin{aligned} I_{sc}(X) &= I_{sc} \cdot X, \\ V_{oc}(X) &= V_{oc} \cdot X, \\ P(X) &= P \cdot X^2, \\ E(X) &= E \cdot X^2, \end{aligned} \tag{3.31}$$

where X, in turn, is given by

$$X = L_T \times 10^9 \tag{3.32}$$

for the case of scaling by surface transfer inductance L_T, or by (3.26) for the case of scaling by the aperture area and shape. To scale on both L_T and area, shape, etc., scale first by the bigger X value, and then by the other.

As can be seen from Tables 3.9 and 3.10, an L_T value of 1 nH is essentially a worst-case estimate, as is also a 6" diameter air vent filter. Therefore, the results in Table 3.11 are reasonably worst-case values themselves. As can be seen, they are larger than the values for diffusion and seams, but they are smaller than those for the open (unhardened) aperture - as one would expect. Therefore, proper use of air vent filters appears to allow for sufficient shielding.

3.5.3 Shielding from Interior Fields

Just as for the previous section, the results here can be found in Table 3.11. The power and energy levels, again, are well below any damage thresholds [3.6], and, in addition, the current and voltage levels are small enough to not pose any problem.

3.5.4 Shielding from Cable Currents (Current Injection)

The numerically predicted worst-case values for I_{sc}, V_{oc}, P and E can be found in Table 3.11, and again, no real problem seems to exist.

3.5.5 Summary

The results of Sections 3.5.2 - 3.5.4 clearly show that the energy levels are all well below the known damage thresholds [3.6]. In addition, a comparison between Sections 3.4 and 3.5 will show a worst-case increase in the shielding effectiveness of between 30-40 dB due to the addition of a material such as wire screen or honeycomb to an aperture.

Table 3.11 Results of a Numerical Three-Dimensional Finite-Difference Solution of Maxwell's Equations for a 6'H x 2'W x 3'D Enclosure with a 6" Diameter Circular Air Vent Filter (L_T = 1 nH)

Frequency of Current	Exterior Field: 50 kV/Meter (Not Frequency Dependent-equation (2.4) J_s = 332.5 Amperes/Meter Across Air Vent Filter				Interior Field: 10A Current (Frequency Dependent- equation 2.2) J_s=3 Ampere/meter Across Air Vent Filter				Current Injection: 10A Current (Frequency Dependent- equation (2.2) J_s=5 Ampere/Meter Across Air Vent Filter			
MHz	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)	I_{sc} (Amperes)	V_{oc} (Volts)	P (Watts)	E (Joules)
0.5	3.79×10^{-3}	5.61	1.14×10^{-3}	6.24×10^{-12}	-	-	-	-	-	-	-	-
2.0					3.49×10^{-5}	7.37×10^{-3}	4.48×10^{-10}	4.84×10^{-10}	5.80×10^{-5}	1.23×10^{-2}	1.25×10^{-9}	1.35×10^{-16}
10					4.64×10^{-5}	3.54×10^{-2}	1.13×10^{-8}	1.44×10^{-15}	7.73×10^{-5}	5.91×10^{-2}	3.15×10^{-8}	3.98×10^{-15}

Notes:

1) The exterior field is not frequency dependent, whereas the interior and current-injected fields are (via equation 2.2).

2) The values for 0.5 MHz are not supplied here, since those available showed quite clearly that the trend above of decreasing values with decreasing frequency continues to hold at 0.5 MHz also. The 10 MHz values provide worst-case estimates, while those coupled with the values at 2 MHz give a clear indication of the trend with frequency.

3) The values of I_{sc} are for a 6' wire shorted to the top and bottom of the equipment cabinet and roughly 7.6 cm (3") from (and centered behind) the air vent filter. The wire radius is 5×10^{-4} meters. The values of V_{oc} are for a roughly 3' x 6' loop oriented with its plane perpendicular to the plane of the air vent filter. The values of P and E are for the 6' wire again, but this time it is terminated at each end in a resistance equal to its characteristic impedance (see Figure 3.45).

4) The values of I_{sc} and V_{oc} scale linearly with surface transfer impedance, while P and E scale quadratically (see equations 3.31 and 3.32), and similarly with area.

3.6 Waveguide Below Cut-Off Techniques

3.6.1 Background

For the propagation of waves inside a hollow cylinder of some uniform cross-section, it can be shown [3.41] that Maxwell's equations and the boundary conditions imply that waves of only certain frequencies will propagate inside the waveguide (as opposed to being strongly attenuated with distance into the guide). This is due to the fact that since the solution must be oscilliatory in both the space and time coordinates, only a certain range of frequencies will allow the boundary conditions to be satisfied at the walls of the guide. This usually evidences itself as a lower limit to the frequency of a wave which can propagate in the guide, or, equivalently, an upper limit to the wavelength.

It is then possible to provide an opening (for air, water, etc.) into an enclosure while still not permitting the entry of electromagnetic energy. Clearly one needs only to make the dimensions of the waveguide such that all of the frequencies of interest (roughly 0.1 - 100 MHz for EMP) are well below the cutoff frequency.

Thus a waveguide operating below its cutoff frequency can sometimes be used to attenuate fields through small apertures. The waveguide must be attached around the hole perimeter and it must protrude out of or into the interior of the enclosure. Figure 3.57 gives the attenuation ratio vs. frequency for a waveguide whose length-to-diameter ratio is unity [3.6]. To obtain the attenuation for other lengths, the attenuation ratio is multiplied by the length-to-diameter ratio. The length should be at least three times the diameter. For example, an 8 inch diameter waveguide 8 inches long has an attenuation of 26 dB at 500 MHz, while a waveguide 24 inches long would have an attenuation of 78 dB. The example points out that the length of the waveguide can become unwieldy for even medium size holes. Where the hole is penetrated by a metal shaft or cables, the resulting configuration is not a waveguide operating below cutoff, because it will support low-frequency propagating TEM WAVES [3.42, 3.43].

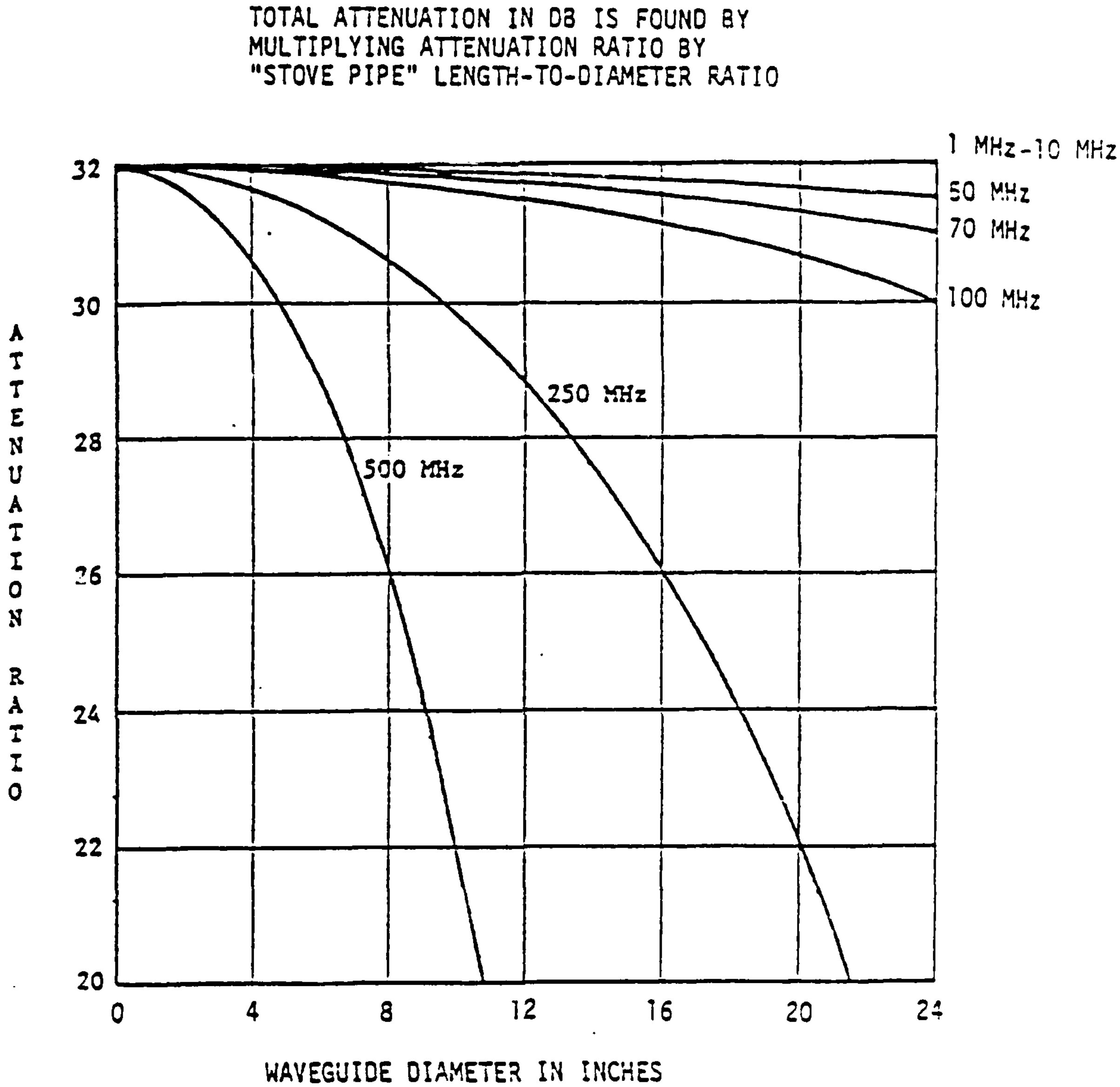
A variation on the cutoff waveguide approach is the use of honeycomb panels. These panels, which consist of an array of small waveguides operating below cutoff, provide shielding by both reflection and waveguide below-cutoff effects and were the subject of Section 3.5.

3.6.2 Shielding from Exterior and Interior Fields and Cable Currents

Consider the enclosure and the waveguide shown in Figure 3.45, and let the waveguide be 6 inches in diameter and 24 inches long - for comparison to the 6" aperture examined. From Figure 3.57 we find that the attenuation is roughly 128 dB over the frequency range 0 - 100 MHz. A simple estimate of the internal coupling could be made by simply attenuating the voltage and current of Table 3.8 by 128 dB. This brings the responses down to an insignificant level.

3.7 Volume Shielding in Summary

In the process of proceeding through this chapter, various ways that EM energy can penetrate into enclosures were presented and discussed. Also considered were the field, current, voltage, power and energy levels to be expected for typical worst-case examples of these penetrants. In addition, ways to avoid some of the particularly troublesome problems were presented.



NOTE: Attenuation in db represents attenuation of fields in propagating through the short waveguide.

Figure 3.57 Waveguide Attenuation Ratio at Selected Frequencies versus Waveguide Diameter [3.6]

One can see in summary, then, that although electromagnetic fields can diffusibly penetrate enclosures to some extent at low frequencies, they are reduced to tolerable levels by metallic surfaces of common thicknesses used in construction. It was also seen that properly designed seams and joints will not allow excessive fields to enter their associated enclosure. However, if reasonable care is not taken in the design of these seams and joints, definite problems could occur. In the case of apertures, it was clear that their use should be avoided as much as possible due to the fact that they present the best possibility of relatively unobstructed entry of EM energy. Properly placed and designed, however, they need not be a problem except in the case of exterior fields. Where possible, however, these apertures can be quite effectively hardened by the use of air vent filter panels or waveguides below cutoff.

The entry of EMP energy into enclosures is not difficult to prevent if reasonable design precautions are taken at the outset. Ignored, however, problems can arise.

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CHAPTER 4

CABLE SHIELDING AND CONNECTORS

4.0 Executive Summary

Chapter 4 discusses the use of shielded cables and connectors as an EMP hardening practice. Shielded cables and connectors form an integral part of the hardening design, and a bad cable, connector, or installation practice can result in unhardened equipment. The object of this chapter is to help the equipment manufacturer choose cabling and connectors necessary for interfacing their equipment with other shipborad equipment.

4.1 Background

Cables and other conductors such as pipes and conduits for electrical wiring receive and efficiently transmit EMP induced current and voltage transients. These spurious signals can penetrate shielded areas on board ship and energy can be deposited into the circuitry of sensitive equipment. The energy associated with the transient can cause mission failure due to permanent damage or temporary upset of shipboard equipment. Knowledge of the mechanisms which couple EMP energy onto cables should give the design engineer insight into the protective measures necessary for mitigation. For this reason, it is important to understand the mechanism through which EMP couples to cables.

Coupling to cables can be analyzed by transmission line theory. In an equivalent transmission line model, the current I flowing on the metal conductor is related to the voltage V between the conductor and a reference point by the telegrapher's equations:

$$\frac{\partial V(z,\omega)}{\partial z} = -Z(\omega)I(z,\omega) + E_z^{inc}(z,\omega) \tag{4.1}$$

and

$$\frac{\partial I(z,\omega)}{\partial z} = -Y(\omega)\,V(z,\omega) + J_s(z,\omega) \tag{4.2}$$

where ω is the angular frequency, $Z(\omega)$ and $Y(\omega)$ are the incremental impedance and admittance of the equivalent line, and E^{inc} and J_s are the incident electric fields and impressed current density (as from a lightning stroke). The source terms E^{inc} and J_s in (4.1) and (4.2) ideally should be those associated only with normal operation of the transmission line. However, distributed voltage sources (E^{inc} in (4.1)) are naturally present in an EMP environment and they can be generated from the currents on the shield when cables are shielded. The distributed current sources which drive cables (J_s in (4.2)) are usually absent in an EMP environment; however, they can be generated from the electric fields that penetrate shielded cables. Further discussion of

these source terms and their relationship to the transfer impedance and transfer admittance are discussed in Section 4 2.1 and 4.3.1.

The transient levels on the cable interface pins specified in Section 2.4.4 define the stress that electronic equipment is expected to encounter in an EMP environment. Upon performing a circuit susceptibility analysis (Chapter 5), it may be found that further shielding (hardening) is necessary to reduce the current and voltage transients on the cable interface pins. This hardening could be attained by shielding the electrical cable.

This chapter provides a means of determining cable shielding. Tables and graphs are provided for use in determining shielding levels for many Navy cables (Section 4.2) and cable connectors (Section 4.3). Also provided is an analytical model for determining cable shielding when measured data are not available (Section 4.2).

4.2 Cable Shielding

4.2.1 Transfer Impedance and Shielding Effectiveness

The ability of a cable shield to isolate the internal volume from the shield current is indicated by several concepts in the literature. The most common concept is that of transfer impedance, in which either an internal electric field or voltage is related to the cable sheath current. Another concept is called shielding effectiveness, in which currents on wires within the shield are related to the shield current. The interior electric field provides a common mode excitation of all the internal conductors which allows the transfer impedance and shielding effectiveness concepts to be used in evaluating shielding of both single conductor as well as multiconductor cables. That is, the electric field drives each internal conductor separately. In the remainder of this subsection, the transfer impedance concept is presented, followed by a discussion on transfer admittance. The concept of shielding effectiveness is then presented along with the relationship between transfer impedance and shielding effectiveness.

Reference 4.1 defines the transfer impedance as

$$Z_T(\omega) = \frac{E_i(\omega)}{I(\omega)} \quad , \qquad (4.3)$$

where $E_i(\omega)$ is the Fourier transfer of the axial electrical field inside of the shield, and $I(\omega)$ is the Fourier transform of the shield current. The inner conductor currents can now be determined by using the transfer impedance and knowing how the internal electric field is related to the inner conductor current. The transfer impedance of single shielded cable is presented in Sections 4.2.2 and 4.2.3 followed by a discussion of multiply shielded cables in Section 4.2.4. Section 4.2.5 discusses the properties of cables containing twisted pairs.

Currents induced on the center conductor by the shield current can be calculated from the shield current. The transfer impedance relates the internal

electric field to the shield current by (4.3). The center connector current is related to the internal electric field as follows:

$$I_\ell(\omega) = \frac{E_i(\omega)\,\ell}{Z_0 + Z_\ell + j\omega\frac{Z_c \ell}{c}} \qquad \left(\ell \ll \frac{2\pi c}{\omega} = \lambda\right) \tag{4.4}$$

where $I_\ell(\omega)$ is the center conductor current, ℓ is the cable length, Z_0 is the source impedance, Z_ℓ is the load impedance, Z_c is the cable characteristic impedance, and c is the speed of light. This relation applies only to cables which are short in comparison to the wavelength of the highest frequency of interest.

For multiply shielded cables, the total transfer impedance can be determined if the transfer impedance of each shield is known. For example, a multiple shielded cable has the total transfer impedance [4.3] as

$$Z_T = \frac{Z_{T1}\,Z_{T2}}{Z_{01} + Z_{02} \pm j\omega L_{sp}} \qquad (\ell \ll \lambda) \tag{4.5}$$

where Z_{T1}, Z_{T2} = surface transfer impedance of the individual shields

Z_{01}, Z_{02} = intrinsic impedance of each shield

L_{sp} = mutual inductance of the space between shields.

More about multiple shielded cables is presented in Section 4.2.4.

EMP energy can couple onto the inner conductors through the shield due to mutual capacitance between the inner conductors (which is related to the transfer admittance) and the local external structure ground. Hence, the transfer admittance is dependent upon external surroundings of the cable and properties of the shield. Reference 4.4 defines the transfer admittance to be

$$Y_T = \frac{1}{V_0}\left.\frac{dI}{dz}\right|_{V=0} \tag{4.6}$$

where V_0 is the voltage between the inner conductors and the external structure. V is the voltage on the inner conductors, and dI/dz is the current per unit length flowing into the internal conductor from the external structure. The transfer admittance can then be used to determine the distributed current sources J(z) injected onto the internal conductor, i.e.

$$J(z) = -Y_T\,V_0$$

or alternatively

$$J(z) = -j\omega C_{12} V_o, \tag{4.8}$$

where C_{12} is the mutual capacitance between the internal conductor and the external structure ground. For complete optical coverage of the inner conductor, there is no mutual capacitance and consequently no distributed current sources. There are other circumstances where the transfer admittance can be neglected [4.4]. The transfer admittance can be neglected with respect to the transfer impedance term if $I_o Z_T >> V_o Y_T Z$ where I_o is the shield current, V_o is the shield voltage, Z_T is the transfer impedance, and Z is the load impedance at either end of the cable.

Shielding effectiveness, as defined in [4.3] is given by

$$\text{S.E. (dB)} = 20 \log \left(\frac{I_s}{I_t}\right), \tag{4.9}$$

where I_s is the total shield current and I_t the current induced in the inner conductor, under the condition that the cable is terminated at each end with a resistance equal to its characteristic impedance, R_o. This shielding effectiveness is related to the transfer impedance (expressed in db) by

$$Z_T(\text{db}) = 20 \log R_L - (\text{S.E.}), \quad (\ell << \lambda) \tag{4.10}$$

where the units are decibels referenced to one ohm, and R_L is the total resistance of the center conduct and its loads, i.e. $R_L \cong 2R_o$. An illustration of the relationship between shielding effectiveness and transfer impedance is shown in Figure 4.1. The relationship of shielding effectiveness to cable length can be derived from (4.4). This relationship was experimentally verified [4.3], i.e.

$$\Delta\text{S.E.} = 20 \log_{10} \frac{\ell_1}{\ell_2}, \qquad (\ell << \lambda) \tag{4.11}$$

where ΔS.E. is the decrease in shielding effectiveness resulting from increasing a cable of length ℓ_2 to length ℓ_1 ($\ell_1 > \ell_2$). Thus, the shielding effectiveness of a 100 meter cable is 40 dB less than that of a 1 meter cable. In addition to the definition of shielding effectiveness in (4.9) there are numerous other definitions. Each definition is strongly dependent upon the geometry of the test fixture, cable lengths, and cable loading. Hence, the usefulness of the shielding effectiveness concepts are generally limited to direct comparisons of cables tested in the same fixture under the same test conditions. The concept of transfer impedance is independent of testing and for this reason it is more general. Thus, the concept of transfer impedance is used in this chapter.

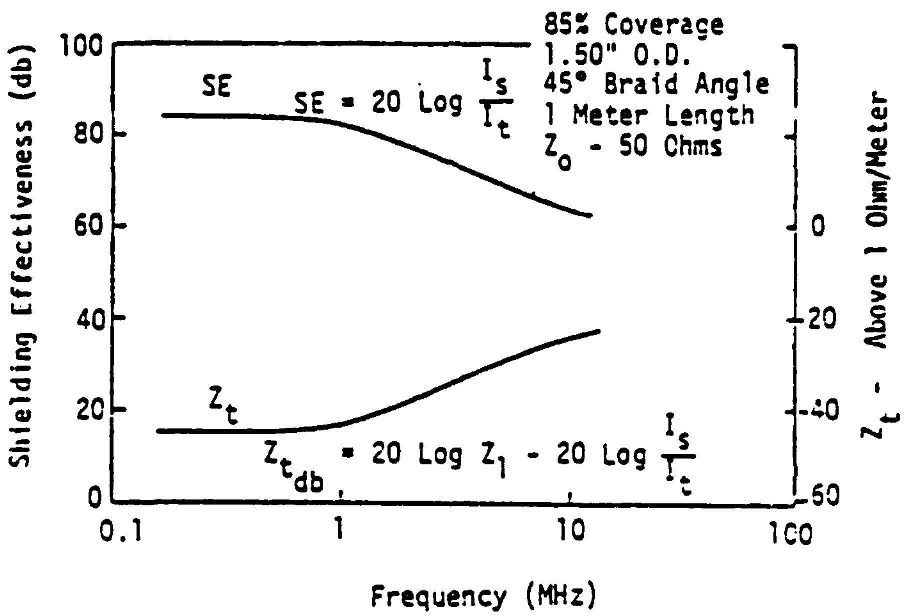


Figure 4.1 Shield Effectiveness and Transfer Impedance [4.3]

From the transfer impedance, a means of determining the transient level on inner conductors is possible. Whenever possible, the actual measured transfer impedance values should be employed in determining cable shielding. Measured data for many Navy cables is presented in Section 4.2.6. When measured data is not available, an approximate transfer impedance can be calculated. Section 4.2.2 discusses methods for determining the transfer impedance of solid shields. Section 4.2.3 discusses methods for calculating the transfer impedance of leaky shields. In Section 4.2.4, methods for calculating multiple shield transfer impedances are presented. Use of the transfer impedance in choosing interface cabling is illustrated through an example in Section 4.2.8.

4.2.2 Solid Shield Transfer Impedance

The transfer of energy from the solid shield onto the inner conductor is primarily through diffusion. For a solid shield of conductivity σ_c, the transfer impedance Z_T is given by

$$Z_T \approx \frac{1 + j}{2\pi r_o \sigma_c \delta} \; \frac{1}{\sinh \Gamma T} \qquad (4.12)$$

where

$$\Gamma = [j\omega\mu_o(\sigma_c + j\omega\varepsilon_c)]^{1/2}$$

$$T = \text{shield thickness, assuming also that } T << r_o \text{, the shield outer radius} \qquad (4.13)$$

$$\delta = \text{skin depth in the shield} = \sqrt{\frac{2}{\omega\mu\sigma_c}}$$

A plot of the normalized transfer impedance, $\frac{\Gamma T}{\sinh \Gamma T}$ and its phase, obtained from the plane-wave solution, is shown in Figure 4.2. Also shown in Figure 4.2 are the high frequency and low frequency approximations to the transfer impedance.

The results in Figure 4.2 are based on the following assumptions:

1. The shields are good conductors ($\sigma_c >> \omega\varepsilon_c$).
2. Diameter of the cable is small compared to the shortest wavelength of interest.
3. The current is uniformly distributed over the circumference of the cable.
4. The coupling between the core current and the outer shield current is loose, so that variations in the interior currents (associated with differences in their terminations) do not cause significant changes in the total cable current.

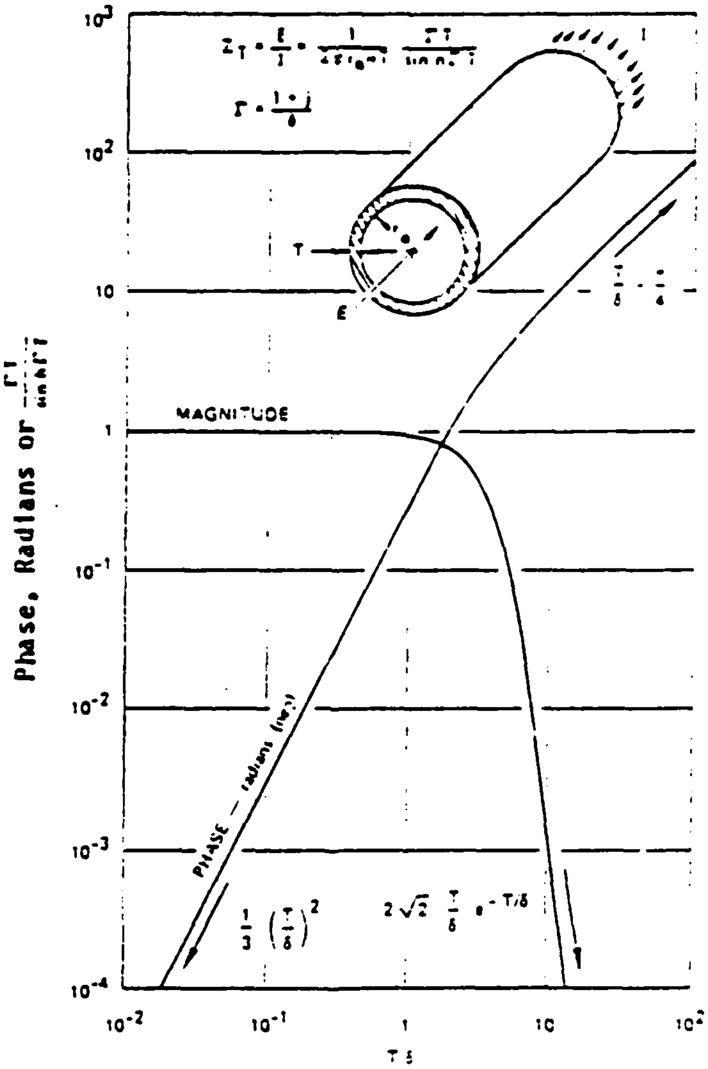


Figure 4.2 Normalized Transfer Impedance for Thin-Walled Solid Cylindrical Shields [1.1]

5. Radiation of the conductor can be neglected.

For reference purposes, the skin depth for various metals versus frequency is shown in Figure 4.3.

4.2.3 Transfer Impedance of Leaky Shields

4.2.3.1 Braided-Wire Shields

The most common type of shielded cable is the braided-wire shielded cable. An analytic determination of the transfer impedance and transfer admittance for braided-wire cable is possible by taking into account diffusion through the shield and direct field penetration through the numerous apertures in the cable shield.

The transfer impedance for a cable having a braided-wire shield is shown in Figure 4.4 and is given by [4.4].

$$Z_T = Z_d + j\omega M_{12} \tag{4.14}$$

where Z_d is the transfer impedance due to diffusion through a solid shield having the same DC resistance per unit length as the braided-wire shield, and M_{12} is the mutual inductance term. The mutual inductance term takes into account the direct magnetic field penetration through the numerous rhombic apertures in the braided-wire shield. The diffusion term and mutual inductance term are

$$Z_d \approx \frac{4}{\pi d^2 N C \sigma \cos\alpha} \frac{(1+j)d/\delta}{\sinh(1+j)d/\delta} \tag{4.15}$$

$$\left.\begin{aligned} M_{12} &\approx \frac{\pi\mu_o}{6C}(1-K)^{3/2}\frac{e^2}{E(e)-(1-e^2)K(e)} \qquad (\alpha < 45°) \\ &\approx \frac{\pi\mu_o}{6C}(1-K)^{3/2}\frac{e^2/\sqrt{1-e^2}}{K(e)-E(e)} \qquad (\alpha > 45°). \end{aligned}\right\} \tag{4.16}$$

where

d is the strand diameter,

δ is the skin depth in the shield at the frequency of interest,

N is the number of strands per carrier, (4.17)

C is the number of carriers,

σ is the conductivity of the wires,

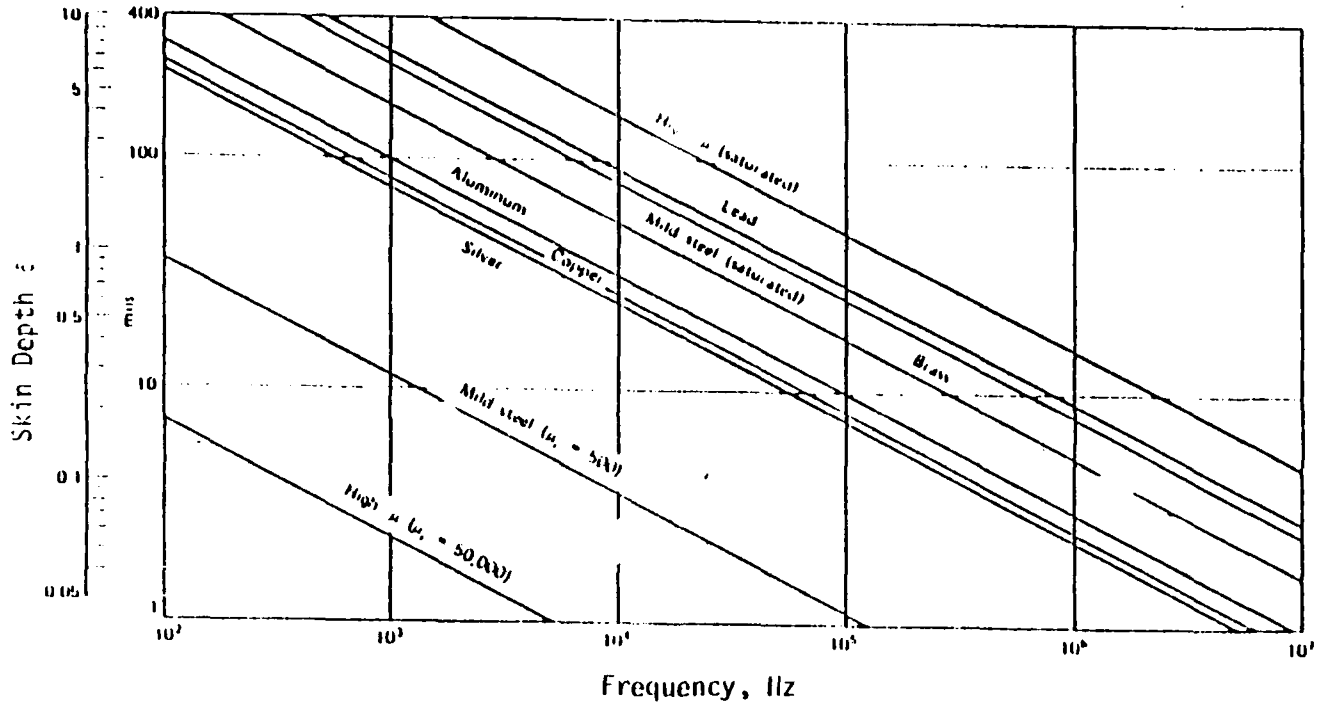


Figure 4.3 Frequency versus Skin Depth for Various Metals [4.4]

K is the optical coverage of the braid,

α is the weave angle, and

$K(e)$ and $E(e)$ are the complete elliptical integrals of the first and second kind, respectively, which are dependant upon the eccentricity.

The eccentricity of an elliptic aperture which approximates a rhombic hole is

$$e = \begin{cases} \sqrt{1 - \tan^2\alpha} & (\alpha<45°) \\ \sqrt{1 - \cot^2\alpha} & (\alpha>45°) \end{cases} \tag{4.18}$$

The optical coverage is

$$K = \frac{NdC}{4\pi a \cos\alpha} \tag{4.19}$$

where a is the shield radius which is small compared to the shortest wavelength of interest. The radius of the shield 'a' should be replaced by 'a+d' for small diameter cables to improve accuracy [4.4].

Figure 4.5 shows us that a group of individual wire strands make up a single carrier. The carriers are woven about other carriers and the weave angle is the angle that the carrier makes in the axial direction.

The major assumption built into the braided-wire cable transfer impedance is that the rhombic apertures resulting in weaving can be approximated by elliptical holes. The transfer impedance for the braided-wire cable is very accurate at low frequencies (i.e. $d<<\delta$) and accurate at high frequencies (i.e. $\omega M_{12} >>|Z_d|$) to less than a factor of 3 [4.4].

An example of the normalized transfer impedance for various optical coverages is shown in Figure 4.6.

The transfer admittance of the braided-wire shielded cable is dependent upon the external surroundings and is given by [4.4]

$$Y_T = j\omega C_{12} \tag{4.20}$$

where

$$C_{12} \cong \begin{cases} g\,\dfrac{\pi C_1 C_2}{6\varepsilon C}(1-K)^{3/2}\dfrac{1}{E(e)} & (\alpha<45°) \\[2ex] g\,\dfrac{\pi C_1 C_2}{6\varepsilon C}(1-K)^{3/2}\dfrac{\sqrt{1-e^2}}{E(e)} & (\alpha>45°) \end{cases}, \tag{4.21}$$

C_1 is the per unit length mutual capacitance of the inner conductor and shield,

C_2 is the per unit length capacitance of the shield,

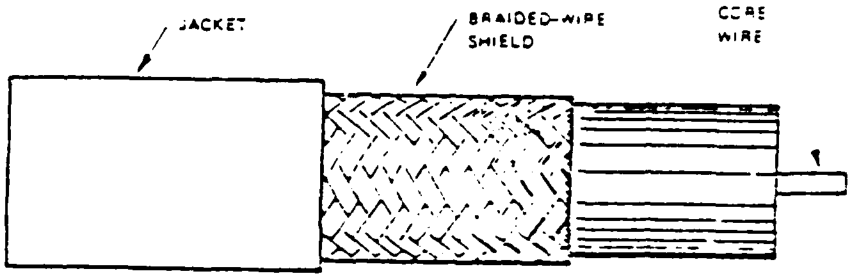
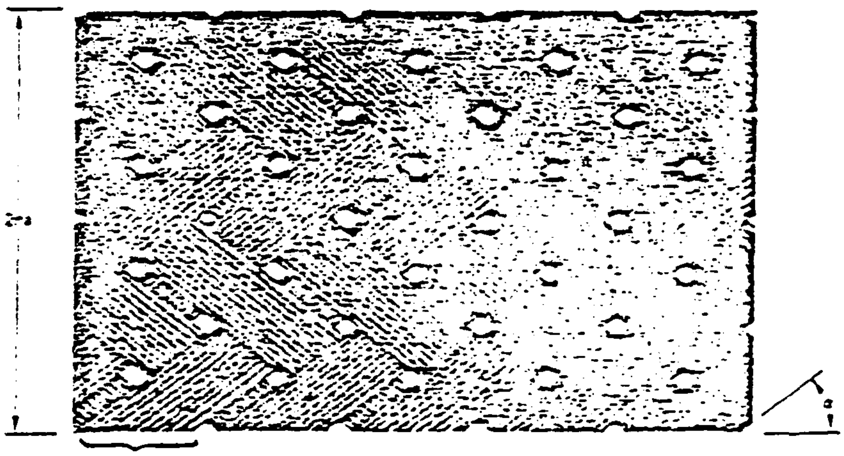


Figure 4.4 Typical Braided Wire [4.4]



Ten strands per carrier shown here

Figure 4.5 Properties of a Typical Braided Snield [1.4]

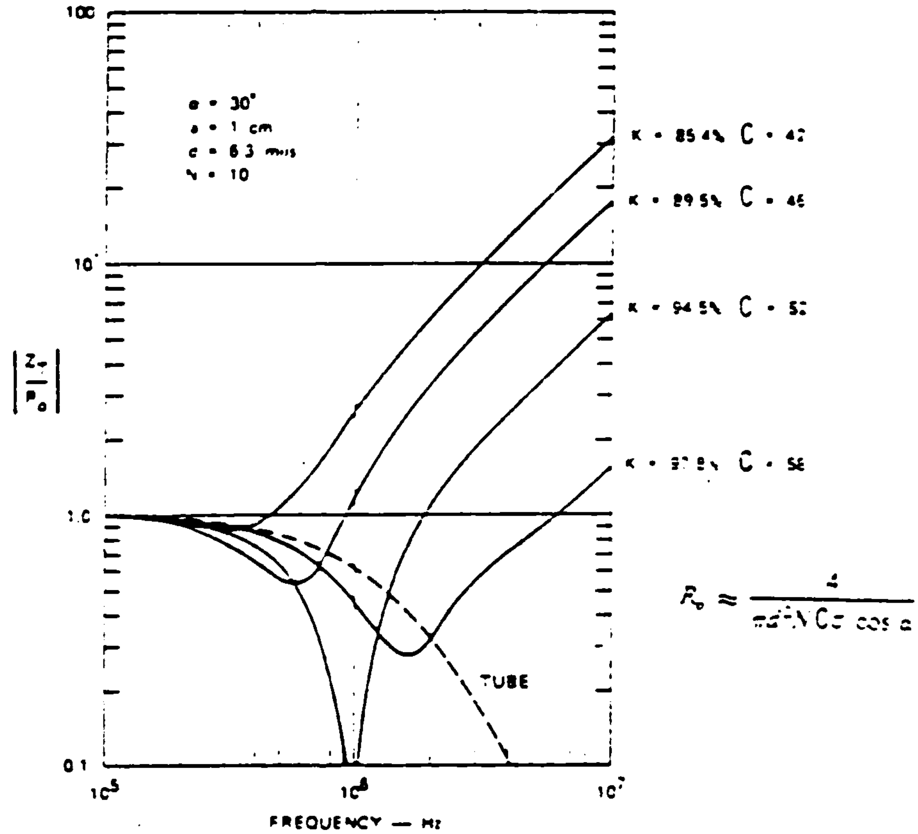


Figure 4.6 Transfer Impedance of a Braided-Wire Shield [4.4]

ε is the insulation permittivity.

The correction factor

$$g = \frac{Z_\varepsilon}{\varepsilon + \varepsilon_2} \tag{4.22}$$

takes into account that the cable sheath dielectric covering ε_2 and inner insulation dielectric can differ. The dielectric sheath is composed of both the outer cable insulation and surrounding media (i.e. air, water, etc.). The remaining parameters in (4.21) are given in (4.17), (4.18), and (4.19).

Table 4.1 summarizes braided-wire shield characteristic parameters for popular coaxial cables. Figure 4.6 compares braided cable transfer impedance with the corresponding solid shield (TUBE).

4.2.3.2 Tape Wound Shields

Another popular method used by manufacturers for shielding cables is the tape-wound shield. This process of shielding can be divided into three distinct categories. The tape-wound shield can have the turns not overlapped and no contact between the turns, or the tape can be overlapped, or the tape can have a gap between the turns.

For a tape-wound shield in which the turns are not overlapped and have no contact between turns, the transfer impedance is [4.4]

$$Z_T = Z_{TUBE} + Z_s \tag{4.23}$$

where

$$Z_{TUBE} = \frac{R_o(1+j)T/S}{\sinh[(1+j)T/\delta]} \tag{4.24}$$

$$Z_s = R_o \left[[(1+j)T/\delta] \coth [(1+j)T/\delta] + j \left(\frac{T}{\delta_o}\right)^2 \frac{a}{T} \right] \tan^2 \alpha \, . \tag{4.25}$$

The transfer impedance is composed of a diffusion term (4.24) and a term which relates to the axial magnetic field leakage of the tape seam (4.25). The remaining parameters are the DC resistance per unit length R_o, the shield thickness T, the skin depth in the shield at the frequency of interst δ, the shield radius a, the wrap angle with respect to the axial direction, and the skin depth for the shield with the permeability being that of free space δ_o. Figure 4.7 shows a cable having a tape-wound shield. Figure 4.8 shows the change in transfer impedance as a function of spiral angle. This figure shows that at low frequencies (i.e. T<<δ) the larger spiral angles result in a larger transfer impedance. At high frequencies (i.e. T>>δ), the smaller wrap angle has the lowest transfer impedance. Note that as the wrap angle approaches zero that the cable transfer impedance approaches the solid shield solution.

Table 4.1 Coaxial Cable Shield Parameters [4.4]

Cable Type (RG-)		Strand Diameter d (inches)	Outer Diameter (inches)	Carriers C	Ends N	Picks P (per inch)	Weave Angle (degrees)	F	Coverage K (%)	Weight per Foot (lbs)	Stranding Factor	DC Resistance R_0	Leakage Inductance	Leakage Capacitance
6		0.0063	0.185	16	9	5.90	25.8	0.740	95.61	0.019	1.54	4.4	3.42	2.4 × [illegible]
6	A1	0.0063	0.185	24	5	8.40	24.0	0.740	95.50	0.019	1.54	6.6	0.79	1.9
6	C	0.0063	0.214	16	6	9.79	31.7	0.806	96.23	0.022	1.98	7.5	3.36	1.9
6	A2	0.0063	0.214	24	6	12.90	27.6	0.806	96.10	0.022	1.90	7.5	0.25	1.2
11		0.0071	0.282	24	8	6.50	27.5	0.799	95.96	0.033	1.59	4.0	0.75	1.6
22	[illegible]	0.0063	0.291	24	8	9.10	35.9	0.763	95.27	0.029	1.95	5.5	0.36	1.9
22	C	0.0063	0.316	24	8	12.00	45.9	0.667	87.50	0.033	2.45	4.4	0.16	0.8
22		0.0063	0.394	24	9	10.50	48.7	0.799	95.95	0.039	2.82	5.9	0.75	1.2
25		0.0063	0.294	16	12	4.00	31.4	0.796	95.44	0.029	1.74	4.8	0.41	2.8
25	A	0.0063	0.296	24	9	4.00	28.8	0.776	94.96	0.029	1.60	4.4	0.36	2.2
25	C	0.0063	0.255	16	15	4.30	25.8	0.887	98.79	0.036	1.80	4.4	0.75	1.6
25	A2	0.0063	0.255	24	11	5.00	25.7	0.796	95.96	0.025	1.54	2.7	0.75	1
35		0.0071	0.478	24	10	6.00	40.8	0.848	97.74	0.056	2.71	4.2	0.12	8.5
58		0.0050	0.120	12	9	7.90	27.7	0.748	93.57	0.009	[illegible]	14.2	3	4.4
58	A	0.0050	0.125	16	[illegible]	10.30	27.7	0.775	94.92	0.018	1.65	[illegible]	2.4	1.2
59		0.0063	0.150	16	[illegible]	8.70	27.8	0.740	94.14	0.015	1.53	6.6	3.44	1.2
59	A	0.0063	0.150	24	5	12.30	27.6	0.871	97.25	0.016	1.53	6.1	3.14	2.6
62		0.0063	0.151	16	7	9.70	27.8	0.776	94.46	0.015	1.65	8.1	0.12	1.4
62	A	0.0063	0.151	24	5	12.30	27.8	0.871	97.15	0.016	1.56	8.1	3.15	8
63		0.0071	0.295	16	12	4.30	27.8	0.792	95.56	0.022	1.61	4.0	3.42	2.7
63	A	0.0071	0.295	24	8	6.50	27.8	0.793	95.71	0.032	1.61	4.6	0.27	1.6
65		0.0071	0.295	24	8	6.50	27.8	0.793	95.71	0.032	1.61	4.0	0.27	1.8
108		0.0050	0.184	16	6	10.00	36.4	0.548	79.38	0.004	2.83	17.8	4.6	25.7
114	[illegible]	0.0062	0.295	24	8	7.00	29.4	0.718	92.07	0.020	1.82	5.1	0.73	4.6
118	[illegible]	0.0071	0.337	24	10	5.40	26.4	0.867	98.10	0.041	1.45	3.1	0.82	8.5
118	C	0.0063	0.367	24	8	10.00	40.5	0.737	93.04	0.033	2.06	6.5	0.85	7.8
122		0.0050	0.095	16	4	12.00	28.9	0.801	96.67	0.008	1.52	16.2	0.27	2.4
122	A	0.0050	0.099	24	4	12.70	19.7	0.928	99.40	0.010	1.21	12.0	3.81	3.38
130		0.0100	0.487	24	8	8.30	39.9	0.786	95.41	0.079	2.18	2.2	0.22	[illegible]
142		0.0050	0.121	16	[illegible]	11.50	38.5	0.791	96.61	0.010	[illegible]	14.1	3.41	2.7
142	C	0.0050	0.141	16	7	14.50	40.7	0.770	95.90	0.011	2.22	16.0	0.55	2.8
144		0.0062	0.290	24	8	9.70	35.1	0.787	96.41	0.029	1.95	5.5	0.22	[illegible]
154		0.0062	0.290	24	8	11.70	41.6	0.851	97.77	0.037	2.18	5.8	2.11	2.55
156	C	0.0070	0.332	24	9	9.20	39.9	0.882	98.13	0.034	2.11	4.1	3.24	[illegible]
158	S	0.0063	0.412	24	8	14.30	57.2	0.838	97.38	0.347	4.18	4.2	[illegible]	3.4
157		0.0062	0.445	24	9	12.00	58.8	0.856	97.57	0.344	4.16	1.6	[illegible]	3.37
157	C	0.0070	0.500	24	10	7.30	44.5	0.729	92.67	0.344	2.88	4	[illegible]	[illegible]
157	S	0.0063	0.500	24	9	12.50	64.5	0.848	97.70	0.348	6.24	5.2	0.15	3.34
174		0.0040	0.063	16	4	15.30	24.4	0.630	86.33	0.007	1.91	25.5	2.2	15.8
179		0.0040	0.066	16	5	12.90	19.2	0.729	92.65	0.004	1.54	29.1	0.40	6.6
181	[illegible]	0.0063	0.215	24	7	8.00	27.7	0.836	97.30	0.023	1.53	5.7	3.14	3.5
181	C	0.0100	0.490	24	8	7.90	43.1	0.829	96.74	0.090	2.29	2.4	0.70	3.06
188	[illegible]	0.0100	0.635	48	7	6.30	27.2	0.918	99.33	0.114	1.38	[illegible]	0.308	3.34
188	C	0.0100	0.680	48	8	7.00	32.7	0.779	95.37	0.184	1.81	1.4	0.11	3
192	[illegible]	0.0100	1.725	48	11	5.87	53.3	0.906	99.22	0.255	3.47	[illegible]	3.14	3.45
192	C	0.0095	1.790	48	11	5.95	54.5	0.764	94.42	0.157	3.98	[illegible]	0.25	3.81
192	S	0.0100	1.890	48	[illegible]	6.83	56.4	0.796	94.84	0.299	4.11	[illegible]	2.11	2.53
192		0.0100	1.725	48	11	4.15	43.5	0.664	85.44	0.229	2.56	0.06	3.54	[illegible]
192	C	0.0095	1.790	48	[illegible]	5.50	57.2	0.775	97.58	0.775	2.88	[illegible]	3.75	4
192	S	0.0100	1.050	48	9	7.10	62.4	0.781	96.79	0.294	6.87	[illegible]	2.27	3.4

A = Alternate
A1 = First alternate
A2 = Second alternate
[illegible]
[illegible]
S = Shield ... from braid

* Braid ... Strand diameter ... [illegible]

Table 4.1 Coaxial Cable Shield Parameters (concluded) [4.4]

Cable Type (RG)	Strand Diameter d (inches)	Outside Diameter (inch)	Carriers C	Ends N	Picks P (per inch)	Weave Angle (degrees)	F	Coverage K (%)	Weight per Foot (lb)	Stranding Factor	DC Resistance [illegible]	Leakage Inductance [illegible]	Leakage Capacitance [illegible]
196	0.0100	1.725	48	11	4.15	43.5	0.664	88.58	0.220	2.90	0.99	0.64	[illegible]
196 C	0.0095	1.780	48	11	5.50	52.2	0.728	82.58	0.225	2.99	[illegible]	[illegible]	0.38
210	0.0063	0.151	16	7	8.70	27.8	0.776	94.98	0.015	1.65	8.1	0.52	3.4
210 A	0.0063	0.151	24	5	12.30	27.8	0.831	[illegible]	0.019	1.54	8.1	0.15	0.96
211	0.0080	0.625	36	10	5.40	32.1	0.644	97.56	0.097	1.65	[illegible]	0.80	0.48
211 A	0.0080	0.625	48	8	5.90	25.2	0.643	97.53	0.087	1.45	1.5	0.88	0.48
212	0.0063	0.190	16	6	5.40	25.8	0.790	95.61	0.016	1.54	6.6	0.47	2.6
212 A1	0.0063	0.190	24	6	9.00	24.9	0.790	95.50	0.019	1.54	6.6	0.29	1.6
212 C	0.0063	0.214	16	9	8.70	37.7	0.404	96.73	0.022	1.90	7.5	0.36	1.8
212 AC	0.0063	0.214	24	6	12.00	37.6	0.505	96.18	0.022	1.90	7.5	0.25	1.2
213	0.0071	0.292	24	8	8.50	27.5	0.799	[illegible]	0.031	1.60	4.8	0.25	1.6
214	0.0063	0.292	24	6	10.60	32.9	0.706	95.44	0.025	2.50	9.9	0.37	1.2
214 C	0.0063	0.317	24	7	15.40	53.0	0.880	97.75	0.034	[illegible]	9.5	[illegible]	0.45
217	0.0071	0.380	24	10	5.40	29.1	0.700	99.49	0.042	1.66	2.2	0.30	1.5
217 C	0.0071	0.405	24	8	10.60	45.3	0.794	95.75	0.046	2.06	5.4	0.22	[illegible]
218	0.0100	0.640	24	14	3.10	30.0	0.490	99.29	0.118	1.53	1.2	0.27	0.44
218 A1	0.0100	0.690	36	9	4.00	29.4	0.611	96.41	[illegible]	1.54	1.2	0.14	0.32
218 A2	0.0100	0.690	48	7	5.00	27.5	0.649	97.72	0.115	1.50	1.1	0.25	0.21
220	0.0100	0.925	36	12	3.50	30.8	0.448	97.44	0.151	1.55	0.91	0.26	0.53
220 A	0.0100	0.925	48	9	4.20	27.5	0.520	96.75	0.148	1.55	0.80	0.34	0.55
222	0.0063	0.189	16	9	5.90	25.8	0.790	95.41	0.015	1.54	6.6	0.47	2.9
222 A1	0.0063	0.189	24	6	8.80	24.9	0.790	96.58	0.015	1.54	6.6	0.29	1.9
222 C	0.0063	0.214	16	9	8.70	37.7	0.404	96.73	0.022	1.98	7.5	0.36	[illegible]
222 AC	0.0063	0.214	24	6	13.00	37.6	0.505	96.19	0.022	1.98	7.5	0.25	1.2
223	0.0050	0.120	12	9	9.00	31.5	0.775	94.95	0.010	[illegible]	14.9	0.72	4.4
223 A1	0.0050	0.120	16	7	11.50	30.4	0.795	95.80	0.018	1.46	15.5	0.42	2.2
223 C	0.0050	0.140	12	9	10.80	38.1	0.729	92.83	0.010	2.22	14.9	1.2	1.8
223 AC	0.0050	0.140	16	7	15.00	41.5	0.792	95.11	0.011	2.29	18.2	0.45	2.2
225	0.0063	0.290	24	6	10.80	52.7	0.708	95.52	0.029	3.49	9.8	0.25	1.2
225 C	0.0063	0.315	24	7	15.40	52.9	0.957	97.90	0.032	2.22	8.5	0.12	0.44
226	0.0063	0.375	24	10	10.50	46.8	0.807	96.14	0.042	2.35	5.2	0.82	0.12
226 C	0.0063	0.400	24	9	10.50	48.6	0.704	91.33	0.035	2.24	5.5	0.92	2.1
301	0.0050	0.190	16	10	8.00	27.1	0.752	93.84	0.014	1.95	10.0	0.72	4.4
302	0.0050	0.151	16	7	11.50	36.8	0.684	90.84	0.010	2.22	15.8	1.5	4.4
303	0.0050	0.121	16	7	11.50	30.6	0.781	95.61	0.010	1.71	14.1	0.42	2.1
304	0.0063	0.190	24	5	14.50	37.6	0.749	93.71	0.712	2.12	5.8	0.52	2.8
304 C	0.0063	0.715	24	6	11.50	34.4	0.756	94.57	0.021	1.51	1.2	0.40	2.2
318	0.0040	0.083	16	5	4.50	7.2	0.722	92.32	0.004	1.41	29.5	0.58	[illegible]
326	0.0035	0.550	24	27	8.46	43.3	0.890	98.80	0.042	2.12	5.7	0.35	0.22
326 C*	0.0035	0.560	24	27	8.46	44.1	0.877	99.49	0.043	2.71	6.8	0.36	0.30
328	0.0100	1.085	48	9	5.50	38.5	0.795	95.80	0.167	2.05	1.8	0.14	0.15
328 C	0.0070	1.125	48	12	6.70	45.0	0.796	95.85	0.111	2.51	[illegible]	0.15	0.64
328 S	0.0100	1.225	48	9	5.60	47.4	0.748	93.62	0.127	2.45	[illegible]	0.28	1.2
329	0.0100	0.290	24	7	5.90	32.3	0.777	94.90	0.040	1.92	2.4	0.38	2.2
329 C	0.0070	0.430	24	9	8.70	45.9	0.794	95.74	0.043	2.78	4.1	0.21	1.2
[illegible]	0.0063	0.391	24	[illegible]	16.30	53.8	0.891	98.62	0.034	3.21	8.1	0.25	2.1

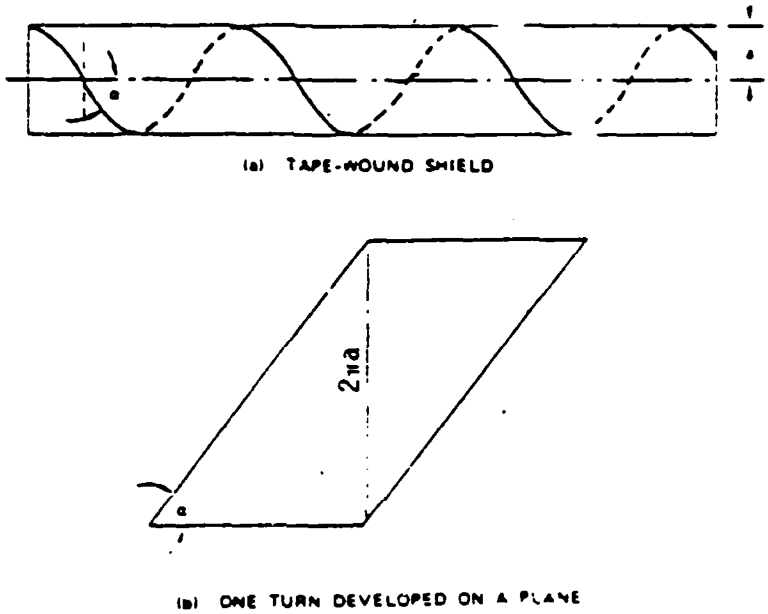


Figure 4.7 Illustration of Parameters for a Single-Layer Tape-Wound Shield [4.4]

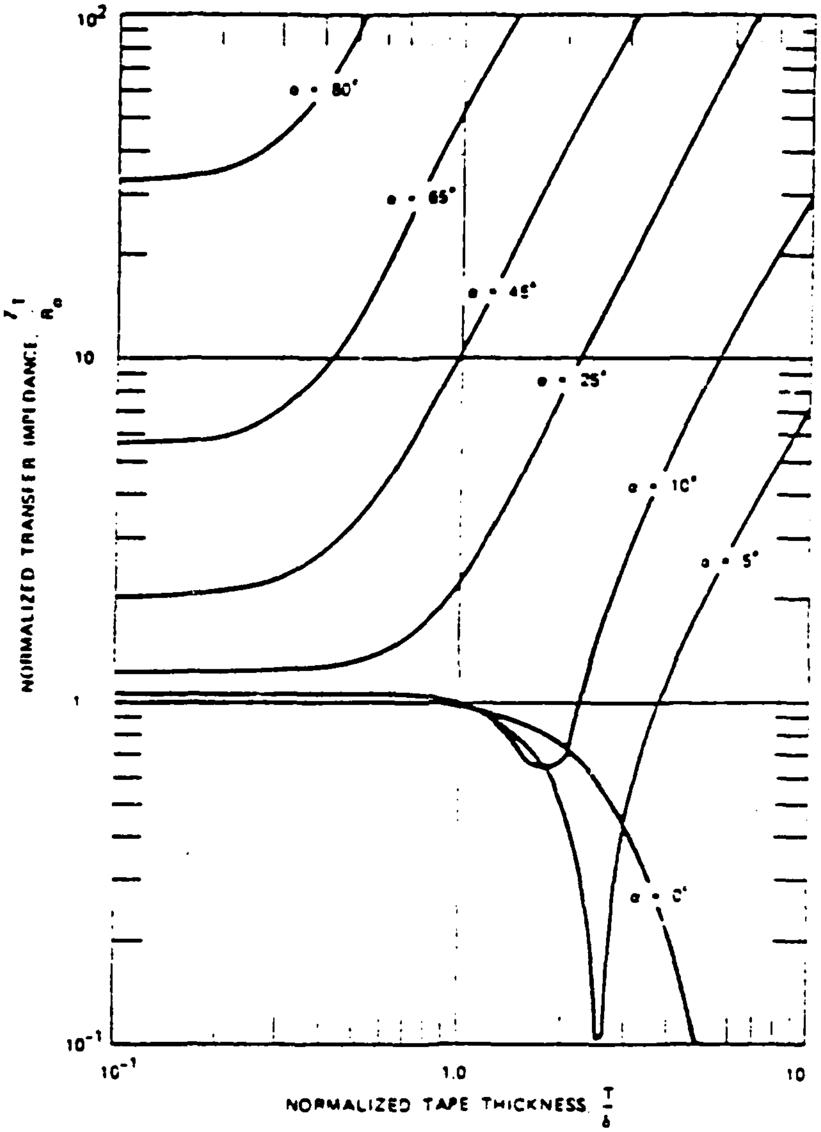


Figure 4.8 Magnitude of the Transfer Impedance Computed for a Tape-Wound Shield [4.4]

For the other types of tape-wound shields, the transfer impedance can be calculated using (4.23), (4.24), and (4.25) providing the wrap angle is modified accordingly. For tape-wound shields where there is a gap between turns, the wrap angle is

$$\alpha = \cos^{-1}((W+W_o)/2\pi a) \tag{4.26}$$

where W is the width of the tape and W_o is the width of the gap. For tape-wound shields where there is overlap between turns, the wrap angle is

$$\alpha = \cos^{-1}((W-W_o)/2\pi a) \tag{4.27}$$

where W is the width of the tap and W_o is the amount of overlap.

For the case where there is a gap between turns, the cable shield does not provide for 100% optical coverage of the inner conductors. Consequently there is a transfer admittance associated with the tape-wound shield with a gap between turns. The transfer admittance is given by (4.20) and the capacitance per unit length is [4.4]

$$C_{12} = \frac{C_1 C_2 W_o^2}{64 \pi \varepsilon a^2 \cos\alpha} \tag{4.28}$$

where C_1 is the per unit length mutual capacitance between the inner conductors and the shield, C_2 is the capacitance per unit length for the shield, and ε is the dielectric constant of the insulator.

4.2.4 Transfer Impedance For Cables With Multiple Shields

The equivalent transfer impedance for multiply shielded cables can be obtained by multiple applications of the two layer transfer impedance formula given in (4.5). For example, suppose we have the triply shielded cable with a solid tubular outer shield, and two inner braided-wire shields. For simplicity, suppose that the characteristic impedance of all three shields are the same, Z_o. The equivalent transfer impedance is

$$Z_T = \frac{Z_{T1} Z_{T2}}{2Z_o + j\omega L_{13}} \tag{4.29}$$

where

$$Z_{T2} = \frac{Z_{T3} Z_{T4}}{2Z_o + j\omega L_{34}} \tag{4.30}$$

where Z_{T1} is the transfer impedance of the inner braid, Z_{T3} is the outer braid transfer impedance, Z_{T4} is the tubular shield transfer impedance, L_{13} is the

mutual inductance between the braided shields, and L_{34} is the mutual inductance between the tubular shield and the outer braided shield.

The characteristic impedance is in general determined by the cable geometry. For example, the characteristic impedance for a coaxial cable is

$$Z_0 = \frac{\sqrt{\mu/\varepsilon}}{2\pi} \log \frac{b}{a} \tag{4.31}$$

where a is the outer radius of the inner conductor, b is the inner radius of the outer conductor, μ is the permeability of the insualtion, and ε is the the permittivity of the insulation.

4.2.5 Shielded and Unshielded Twisted Pair Cables

In single conductor transmission lines, the return path for the circuit is either through the ground system or through the shield of a shielded cable. The ground loop formed by the transmission line can couple considerable energy to the circuit elements. To minimize the induction loop area and consequently voltage sources, twisted pairs of cables are often used. A detailed discussion of the coupling mechanism is in Section 9.2.1 of Grounding and Bonding.

A time varying uniform magnetic field impinging radially upon the twisted pair cable provides for approximate elimination of the voltage sources (see Figure 4.9a). This is because the net induction loop area in the direction of the magnetic field is less than one twist of the cable pair.

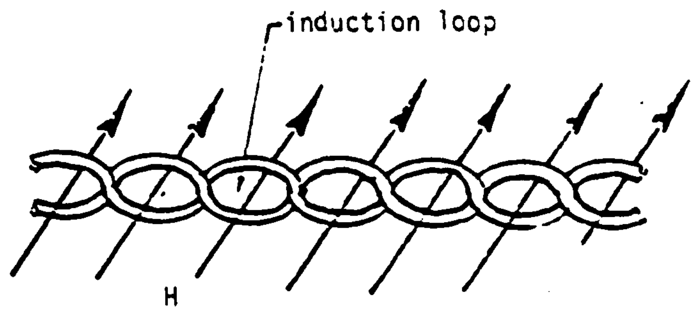
For a time varying uniform magnetic field impinging axially on the twisted pair cable, the effective induction loop area is a circular loop the radius of the insulation on one of the twisted pair cables times the number of twists in the cable (see Figure 4.9b). This composes an air wound solenoid. Thus it is possible, although not probable, to couple large amounts of energy into a system.

When the magnetic fields are not uniform there is even greater coupling to the twisted pair cable. This coupling is generally small due to the small loop areas formed by the cables.

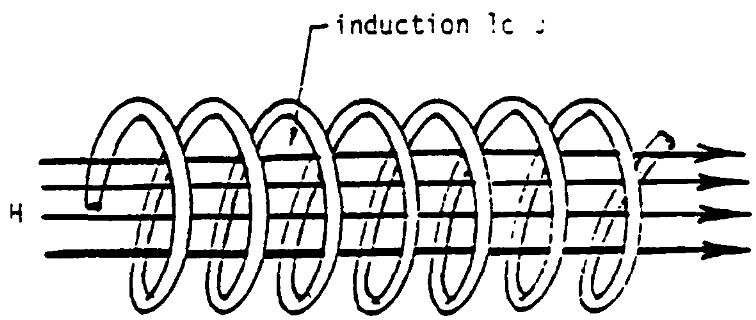
When a twisted pair is shielded, the current sources driving the cable are greatly reduced. This is because the shield reduces the electrostatic coupling into the cables (i.e. small transfer admittance). This is part of cable shielding and is discussed in the previous sections. Low magnetic and electrostatic field cable coupling is thus possible for shielded twisted pair cables. Thus, the use of shielded twisted pairs can virtually eliminate spurrious signals from appearing on signal lines.

4.2.6 Measured Surface Transfer Impedance of Navy Shielded Cables

This subsection describes the results of a testing effort to measure the surface transfer impedance of a number (15) of shielded cables currently in use by the U.S. Navy [4.5]. The objectives of this test effort was to determine the shielding provided by these cables.



a) Radial Magnetic Field



b) Axial Magnetic Field

Figure 4.9 Induction Loop Areas For Twisted Pair Cables

The tests were carried out using the triaxial test figures and the swept frequency continuous wave (CW) test procedures described in Section 10.2.

A general description of the fifteen (15) types of shielded cables tested and their physical/electrical characteristics are given in Table 4.2. As can be seen in the table, the shield designs of all cables except the 2SJ-11 are of braid-wire construction. The 2SJ-11 cable shield consists of a spiral-wrapped copper tape. All of these cables are used in shielded circuit applications aboard U.S. Navy ships. These applications include weapons control, radar, NTDS, sonar, interior communications, lighting, and power circuits. Of the cables listed in Table 4.2, only the 2SWU-1 and DSWS-4 are watertight cables. These cables are used where a watertight deck or bulkhead is to be penetrated. The cable geometry parameters are provided in Table 4.3 for reference purposes.

A summary of the measurement results is presented in Table 4.4. Continuous plots of the magnitude of the transfer impedance as a function of frequency are given in Figures 4.10 through 4.24.

4.2.7 Supplemental Measured Surface Transfer Impedance of Shielded Cables and Discussion

From the measured transfer impedance and shielding effectiveness of other shielded cables, some general observations concerning the shielding effectiveness of shielded cables can be made. That is, the shielding effectiveness is affected by corrosion, choice of shielding material, grounding of the armor shield, braid angle, wire size and use of multiple shields to name a few. This subsection addresses some of these effects and their relation to the shielding effectiveness of shielded cables.

Reference 4.1 gives some computed results for a double solid shielded cable 640 meters long with a core of 8 pairs of 16-gauge copper wires and 18 pairs of 19-gauge copper wires. The cable shields were shorted at the ends, and the core to inner shield termination was open circuited. The other characteristics are shown in Table 4.5.

Figure 4.25 shows the transfer impedance magnitude as computed from (4.3). Figures 4.26 and 4.27 illustrate the current response to a unit impulse of current in the outer shield and the voltage response to the same impulse.

Transfer impedance measurements of five different cable types are listed below [4.1]:

1. RG 62B/U, single shield (Figure 4.28)
2. RG 13A/U, double shield (Figure 4.29)
3. RG 58A/U, triax (Figure 4.30)
4. Electronic Specialty Co. Evaluation Test Cable 0.170-inch diameter solid shield (Figure 4.31)
5. RG 12/U Armored:
   a. with armor floating (Figure 4.32)
   b. with armor bonded to the cable outer conductor at ends (Figure 4.33). (NOTE: the bond was made using a

Table 4.2 General Description/Characteristics of Navy Cables Tested [4.5]

Type & Size Designation	No. of Cndrs in Cable	Conductor Size: Nom. Diam. Inches	Conductor Size: Nom. Area MCM	Cable O.D. Max Inches	Rated Voltage Max(RMS)	Max. Amperes per Conductor: D.C.	Max. Amperes per Conductor: 400Hz	Shield Type	Federal Stock Number 6145-
2SJ-7	2	0.171	22.800	0.605	600	56	56	Tin coated copper braided shield.	110-6297
3SJ-14	3	0.072	3.831	0.325	600	14	14		838-0005
4SJ-20	4	0.041	1.216	0.280	600	6	--		110-6306
MCOS-2	2	0.049	1.608	0.460	600	5	--	Uncoated copper braided shield.	913-7297
*MCOS-5	5	0.028	0.525	0.305	300	3/1	--		917-2342
DSS-2	2	0.048	1.779	0.390	600	6	--	Tin coated copper braided shield.	914-9973
DSS-4	2	0.076	4.497	0.500	600	13	--		913-2401
FSS-4	4	0.076	4.497	0.625	600	13	--		965-7843
7SS-2	7	0.048	1.779	0.625	600	--	--		905-6797
MS-37	37	0.057	2.426	0.800	300	--	--		079-1287
2SWU-1	2	0.046	1.620	0.255	---	--	--		901-0091
**1S75MU-8	8	0.031	0.700	1.080	---	--	--		811-4611
2AU-40	80	0.031	0.700	1.370	600	--	--		905-7255
DSWS-4	2	0.076	4.497	0.800	---	--	--		776-8513
2SJ-11	2	0.108	9.016	0.445	600	31	16	Spiral wrapped copper tape.	110-6303

* This cable has one shielded pair and three single unshielded conductors.

** This cable contains 8 shielded coaxial lines without any common overall shield.

Table 4.3 Measured Shield Construction/Coverage Characteristi-s of Cables Tested [4.5]

Cable Type	Picks per Inch, P	No. of Strands per Braid, N	Diameter of Strands, d, Mils	Shield Radius a, Inches	No. of Carriers	Braid Angle, α, Degrees (calculated)	Fill F (cal.)	Optical Coverage, % K = 100 $(2F-F^2)$(cal.)
2SJ-7	6.7	11	10.0	0.21	24	36	1.25	94
3SJ-14	10.0	6	10.0	0.11	24	30	1.23	95
4SJ-20	6.7	9	10.0	0.09	16	25	1.43	81
MCOS-2	10.7	7	5.0	0.10	24	30	0.76	94
MCOS-5	15.6	5	5.0	0.07	24	31	0.76	94
DSS-2	12.6	6	6.3	0.11	16	49	0.62	86
DSS-4	13.2	6	6.3	0.18	24	51	0.64	86
FSS-4	14.2	6	6.3	0.19	24	56	0.65	87
TSS-2	14.2	6	6.3	0.19	24	55	0.66	88
MS-37	7.6	10	6.3	0.30	24	50	0.55	80
2SWU-1	9.6	7	5.0	0.09	16	35	0.59	83
1679MU-8	18.3	4	10.0	0.08	24	39	1.17	97
2AU-40	8.3	10	6.3	0.52	24	66	0.57	82
LSWS-4	9.9	8	6.3	0.16	16	51	0.64	87

*2SJ-11	width, w inches 0.75	overlap, inches 0.21	shield radius a, inches 0.16	Braid angle, α, degrees 57	Turns, N per inch 1.5

* Spiral wrapped copper tape.

Table 4.4 Summary of Test Results [4.5]

Cable Type	Magnitude of Measured Surface Transfer Impedance at			
	0.1 MHz	1 MHz	10 MHz	100 MHz
2SJ-7	5.2 mΩ/m	2.8 mΩ/m	17 mΩ/m	200 mΩ/m
3SS-14	7.5	8.4	24	450
4SJ-20	12.5	8.4	42	560
HCOS-2	12.5	10.8	13	170
MCOS-5	15	24	110	Large*
DSS-2	18	30.5	190	Large*
DSS-4	11.4	16	90	Large*
TSS-4	13.5	26	165	Large*
7SS-2	13.5	27.5	170	850
MS-37	6.8	16.8	120	Large*
2SWU-1	18.5	20.5	115	Large*
**1S75MU-8	0.22	0.14	Below noise level	9
DSWS-4	12.3	26	185	Large*
2AU-40	11.5	43	300	Large*
2SJ-11	75	132	270	Large*

** This cable has 8 individually shielded coaxial lines without any outer common shield.

* "Large" implies the magnitude of the surface transfer impedance is larger than 1000 mΩ/m.

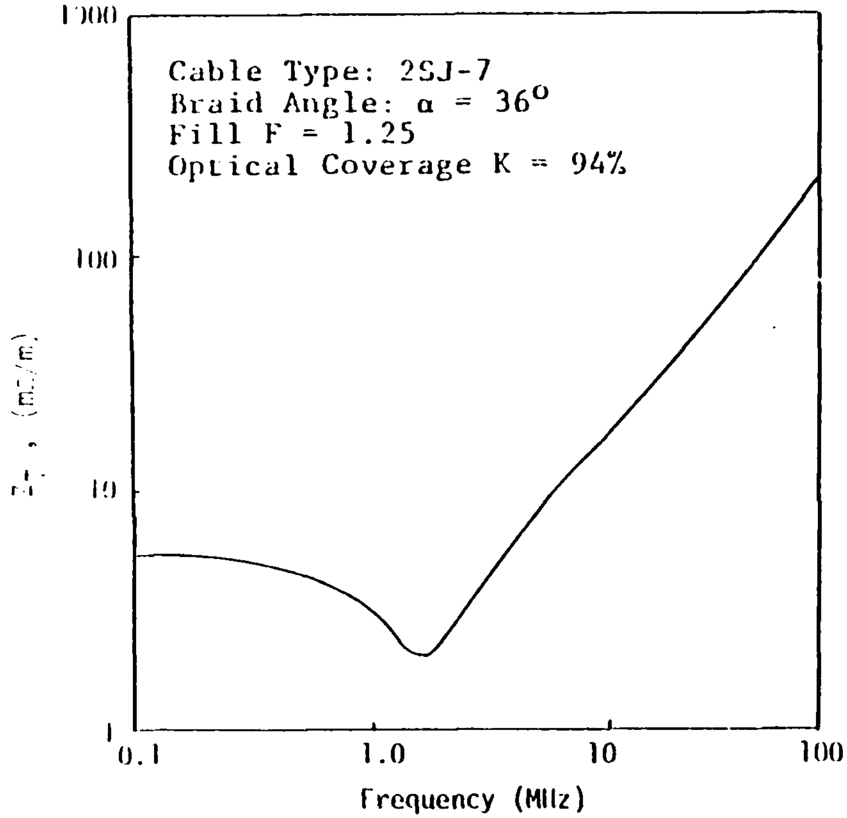
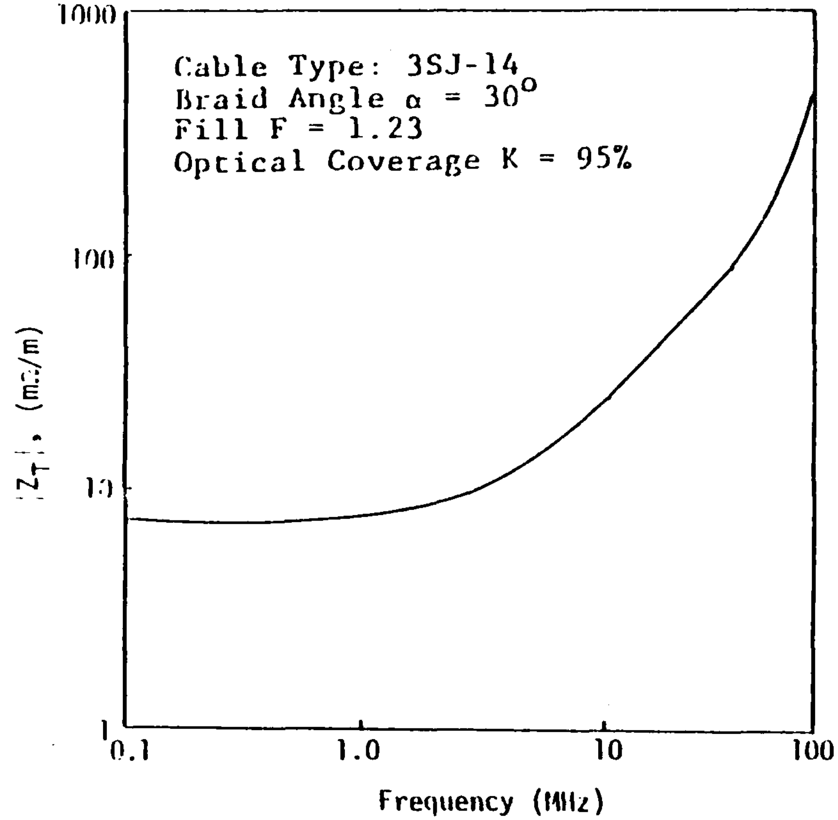


Figure 4.10 Measured Amplitude of Surface Transfer Impedance for 2SJ-7 Type Cable [4.5]



4.11 Measured Amplitude of Surface Transfer Impedance for 3SJ-14 Cable [4.5]

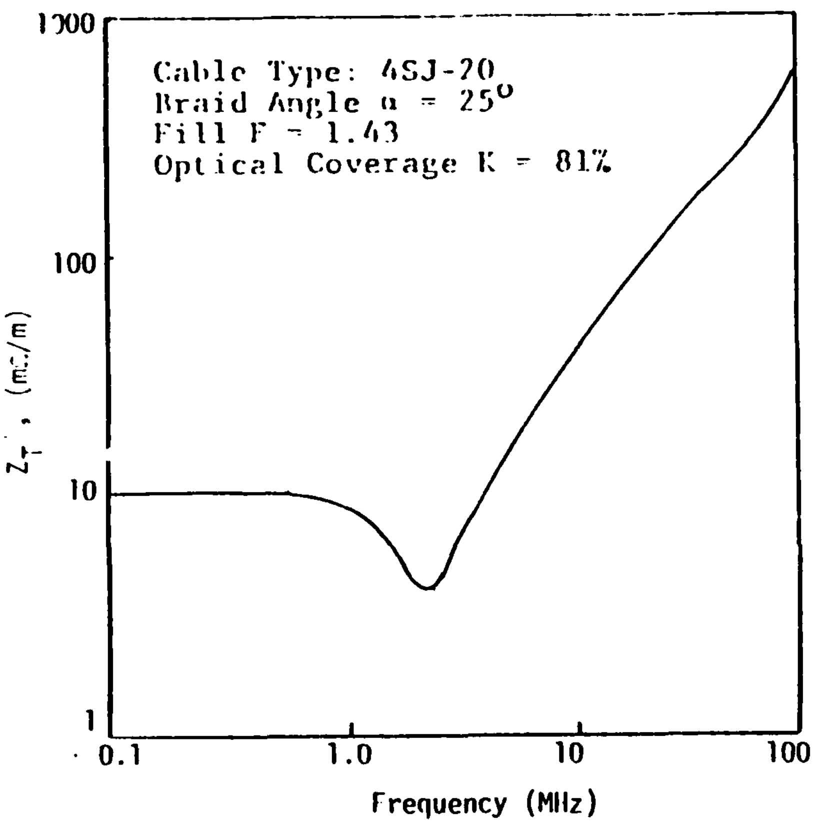


Figure 4.12 Measured Amplitude of Surface Transfer Impedance for 4SJ-20 Cable [4.5]

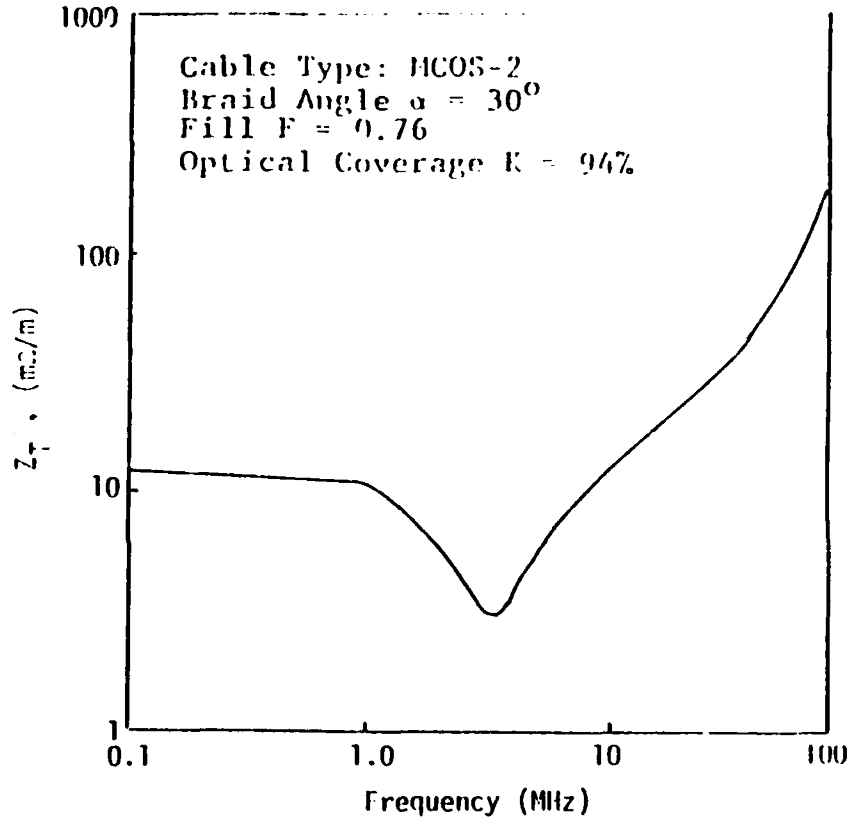


Figure 4.13 Measured Amplitude of Surface Transfer Impedance for MCOS-2 Cable [4.5]

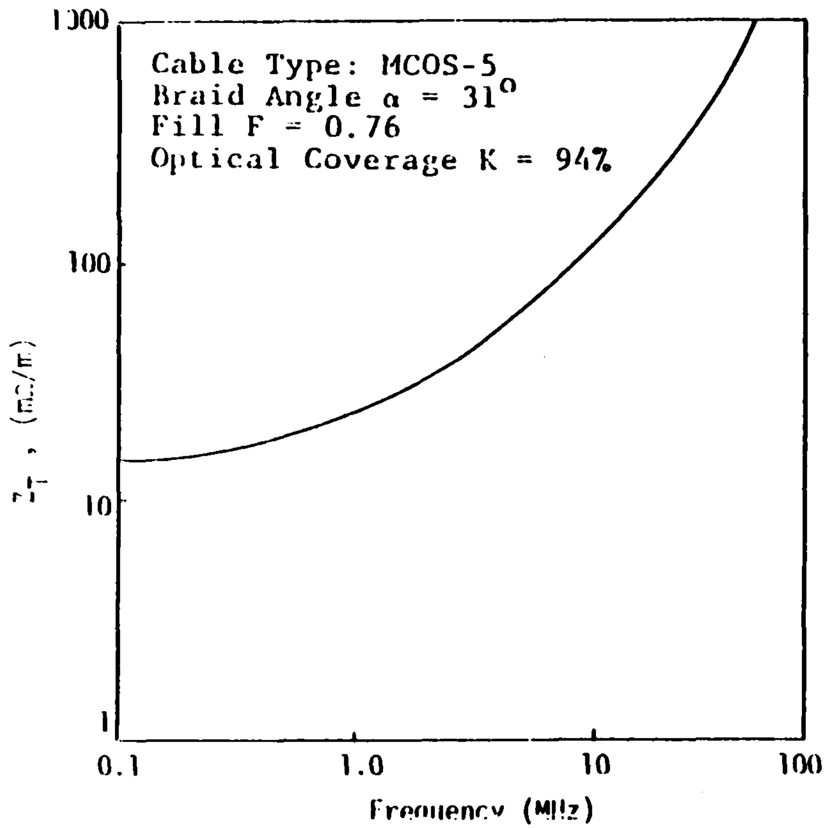


Figure 4.14 Measured Amplitude of Surface Transfer Impedance for MCOS-5 Cable [4.5]

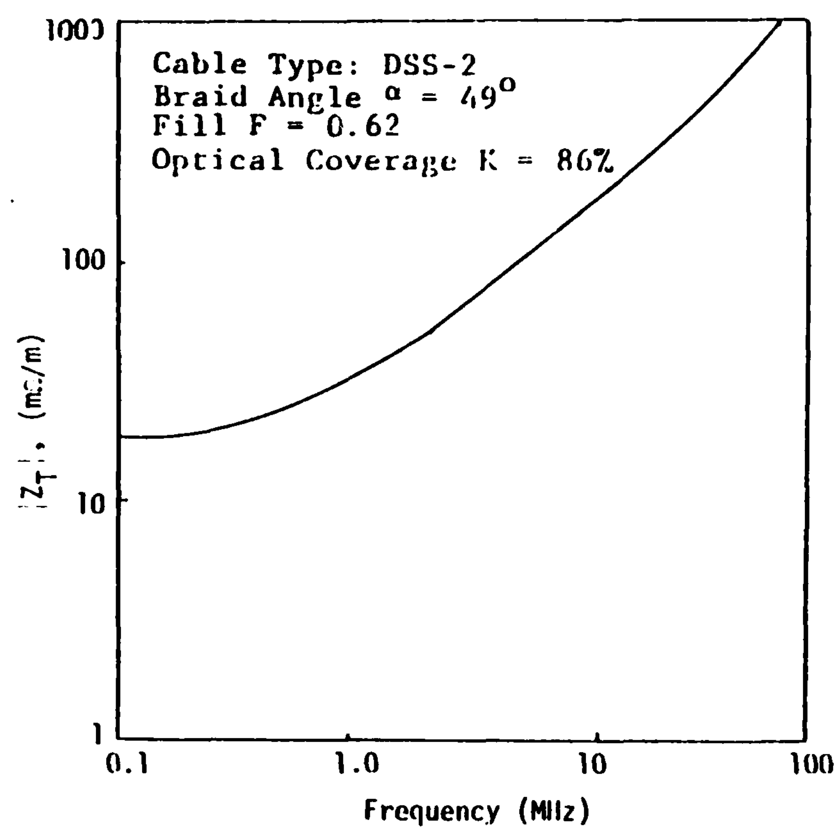


Figure 4.15 Measured Amplitude of Surface Transfer Impedance for DSS-2 Cable [4.5]

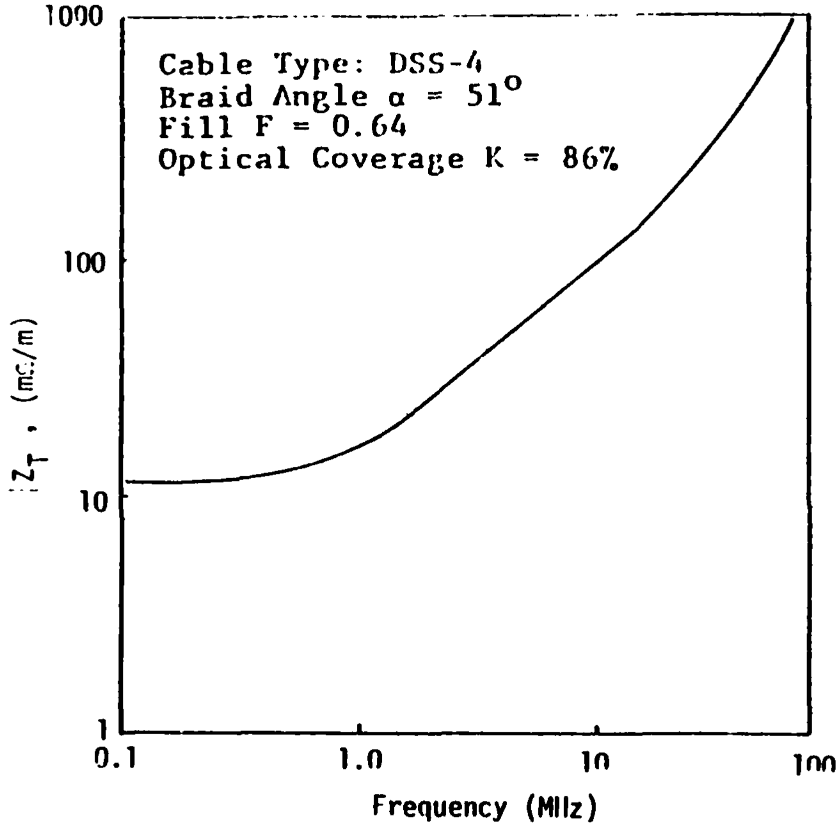


Figure 4.16 Measured Amplitude of Surface Transfer Impedance for DSS-4 Cable [4.5]

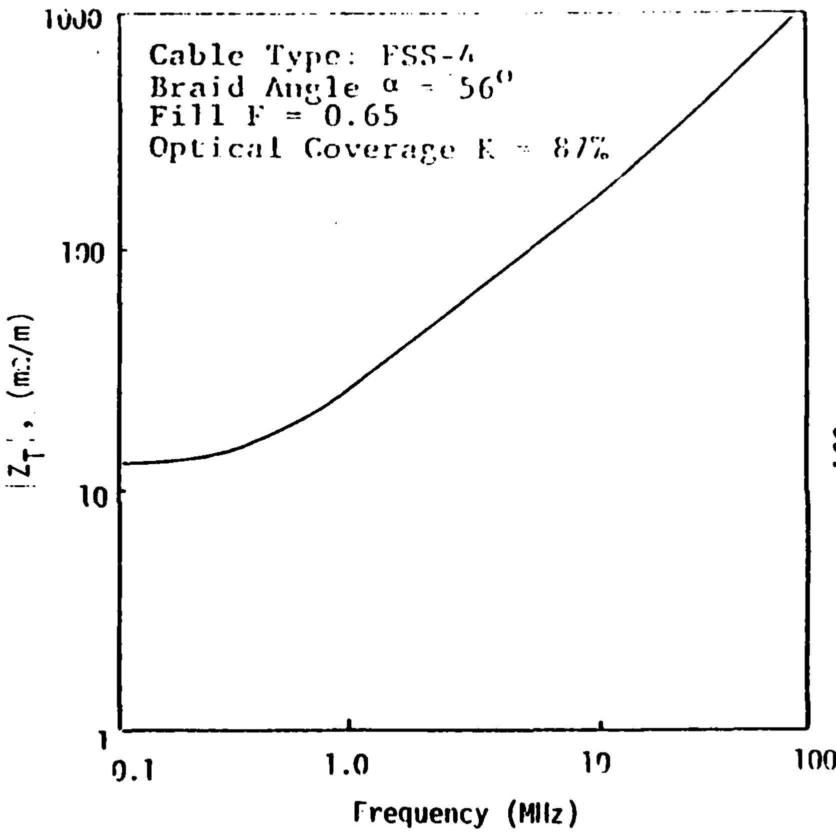


Figure 4.17 Measured Amplitude of Surface Transfer Impedance for FSS-4 Cable [4.5]

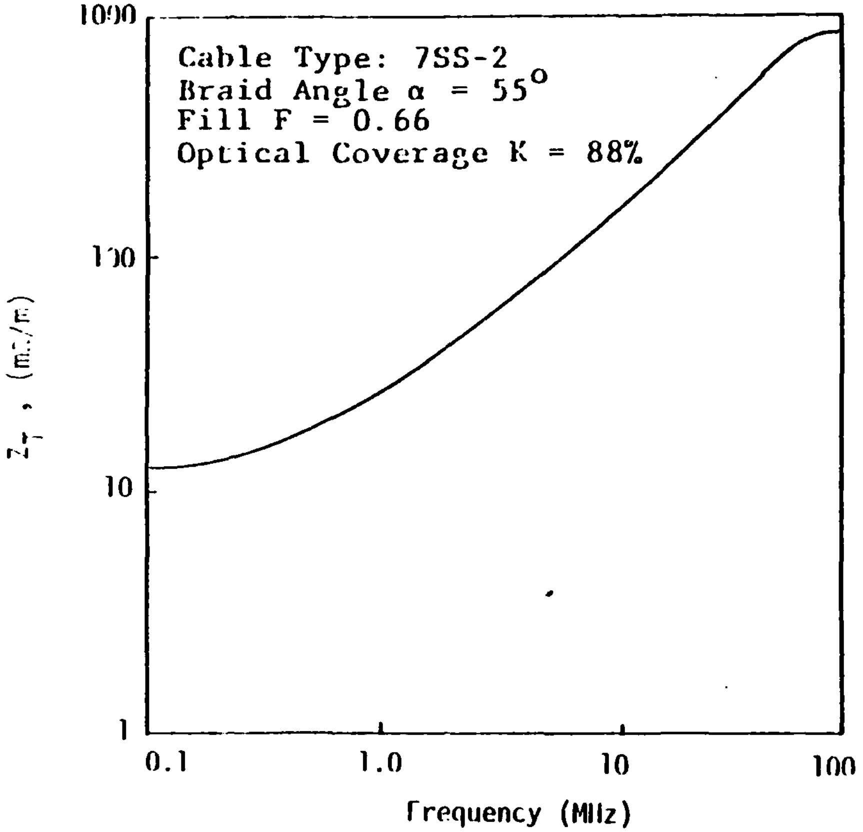


Figure 4.18 Measured Amplitude of Surface Transfer Impedance for 7SS-2 Cable [4.5]

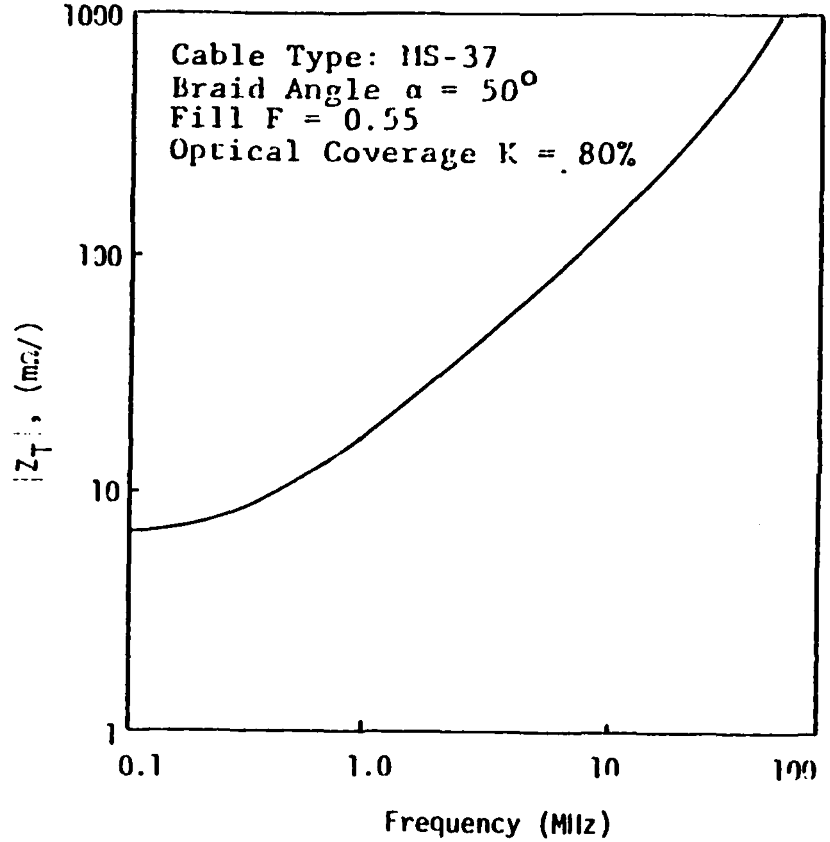


Figure 4.19 Measured Amplitude of Surface Transfer Impedance for MS-37 Cable [4.5]

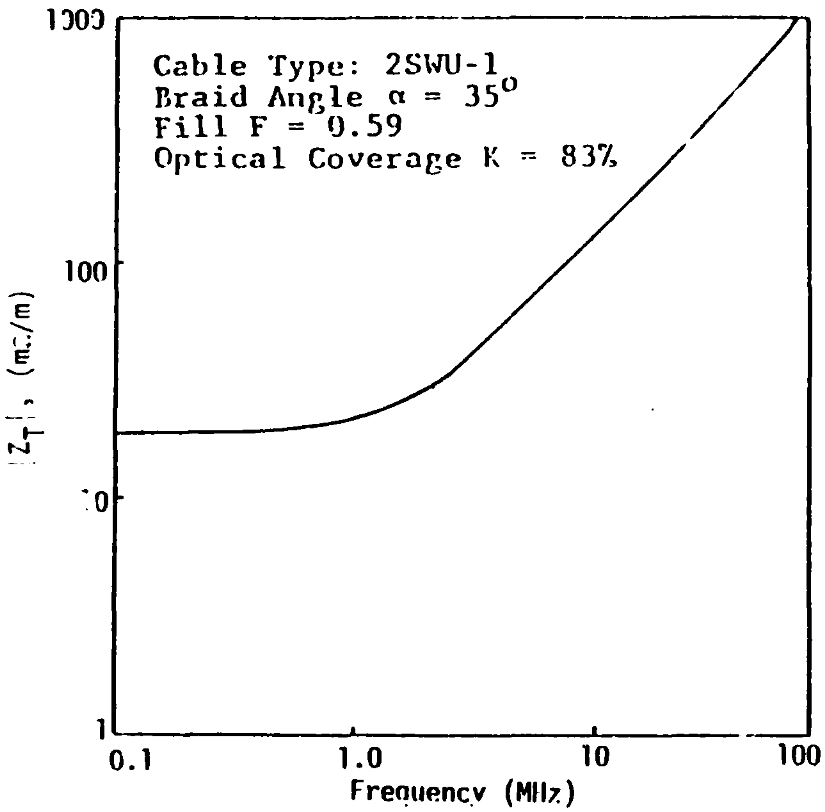


Figure 4.20 Measured Amplitude of Surface Transfer Transfer Impedance for 2SWU-1 Cable [4.5]

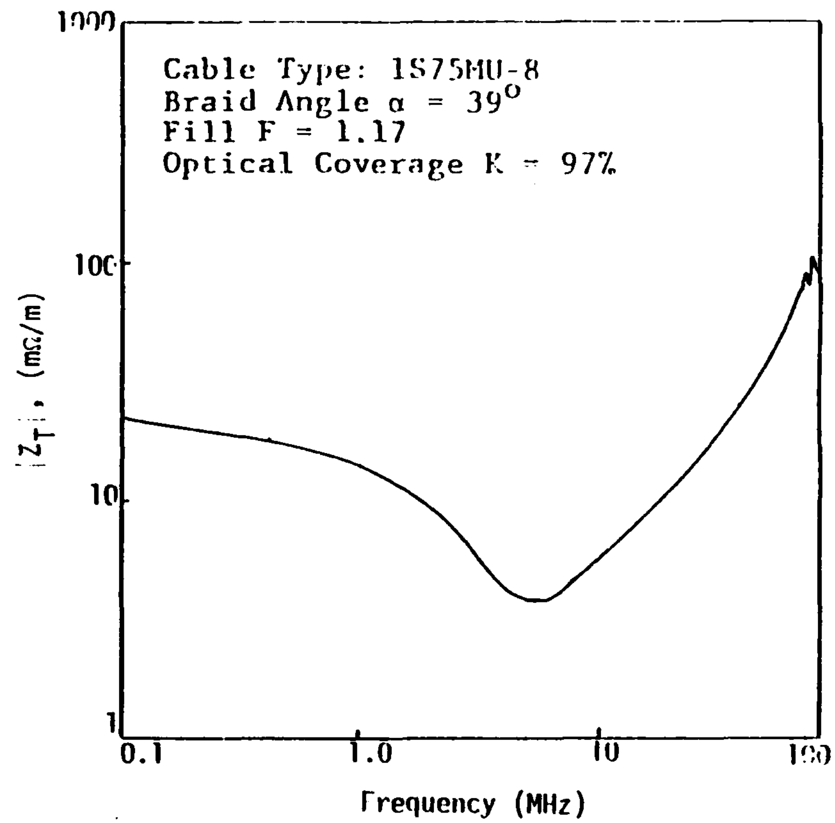


Figure 4.21 Measured Amplitude of Surface Transfer Impedance for 1S75MU-8 Cable [4.5]

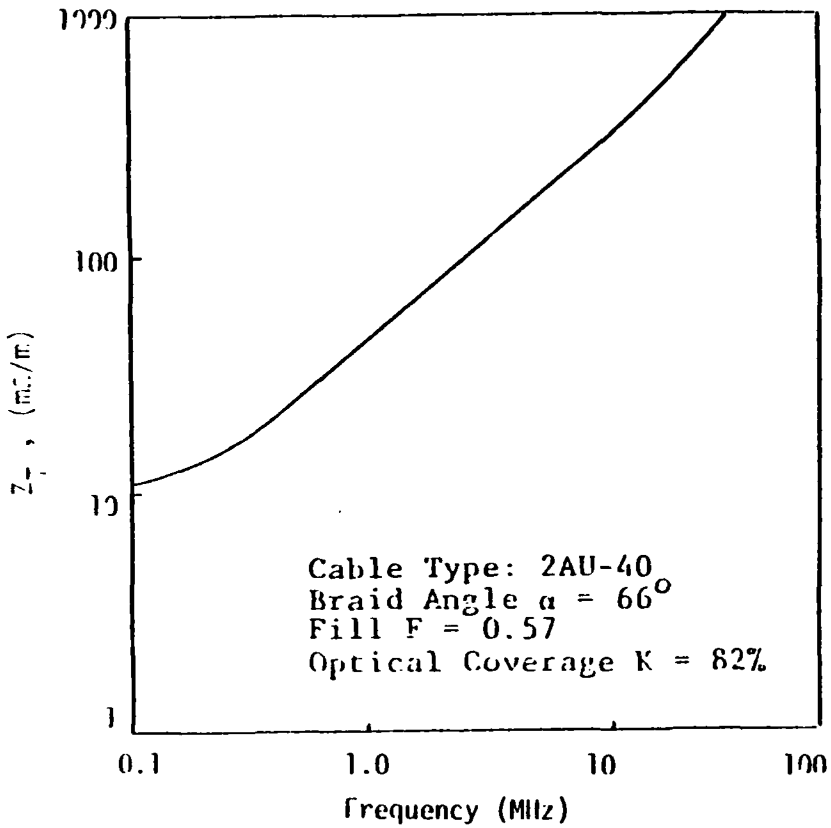


Figure 4.22 Measured Amplitude of Surface Transfer Impedance for 2AU-40 Cable [4.5]

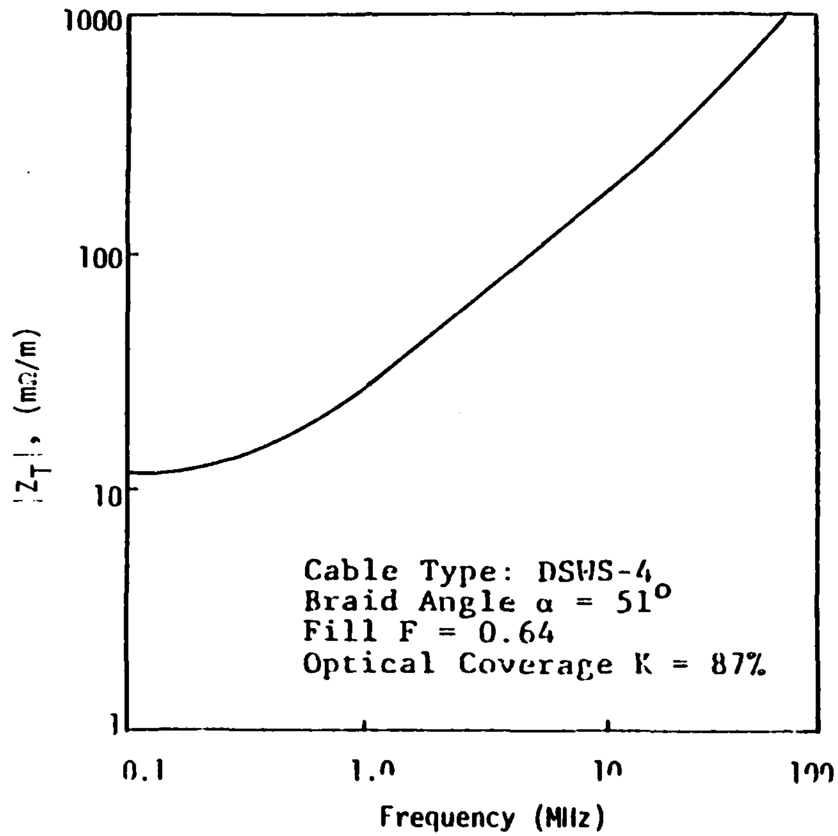


Figure 4.23 Measured Amplitude of Surface Transfer Impedance for DSWS-4 Cable [4.5]

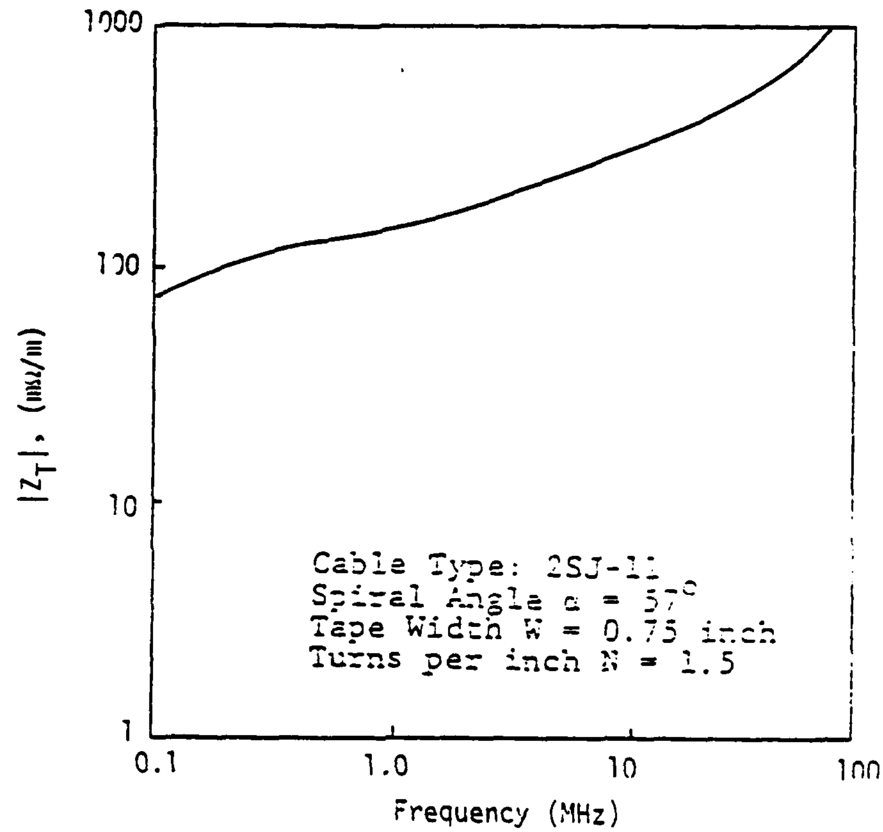


Figure 4.24 Measured Amplitude of Surface Transfer Impedance for 2SJ-11 Cable [4.5]

Table 4.5 Characteristics of Example Cable [4.1]

Characteristic	Outer Sheath	Gap	Inner Sheath	Gap	Core
Material	Copper	Air, Polyethylene	Mild steel	Polyethylene	Copper
Radius (cm)	2.2	-	1.5	-	1.0
Thickness (mils)	20	-	10	-	
Conductivity[a] (mho/m)	4.7×10^7	0	7.5×10^6	0	5.8×10^7
Relative Permeability	1.0	1.0	620	1.0	1.0
Dielectric Constant	10	1.4	10	2	10

NOTE: [a]The reduced conductivity of the outer sheath was used to accommodate the fact that the outer sheath was corrugated.

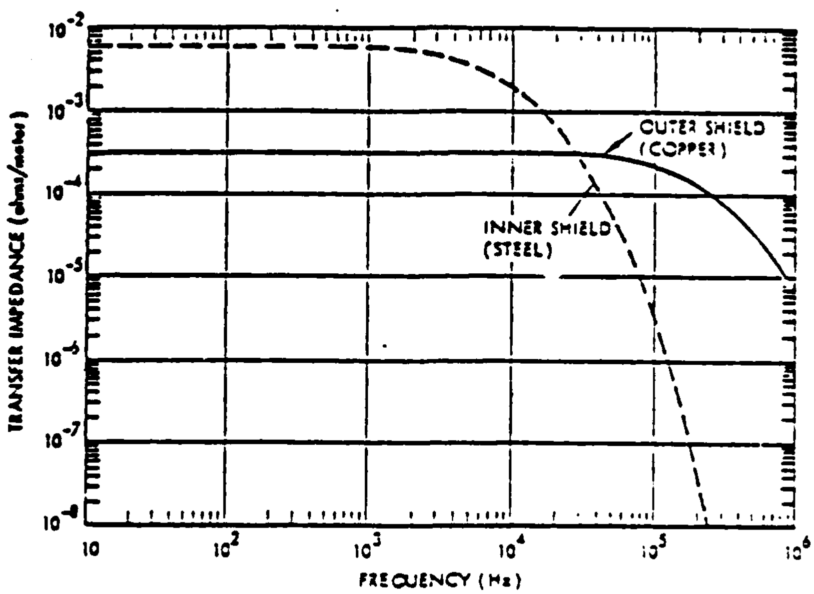


Figure 4.25 Magnitude of Transfer Impedance for 20-mil Copper Shield and 10-mil Mild Steel Shield [4.1]

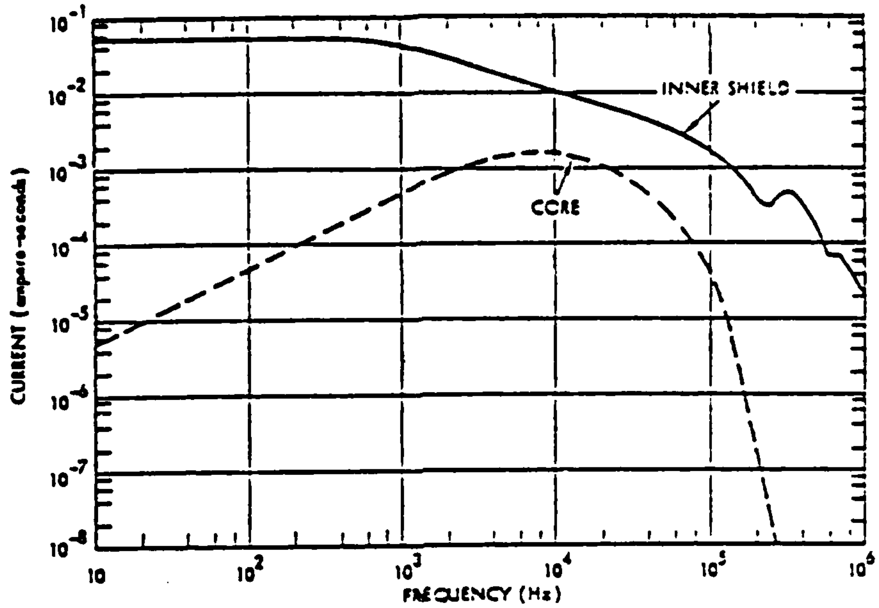


Figure 4.26 Current Responses to Unit Impulse [4.1]

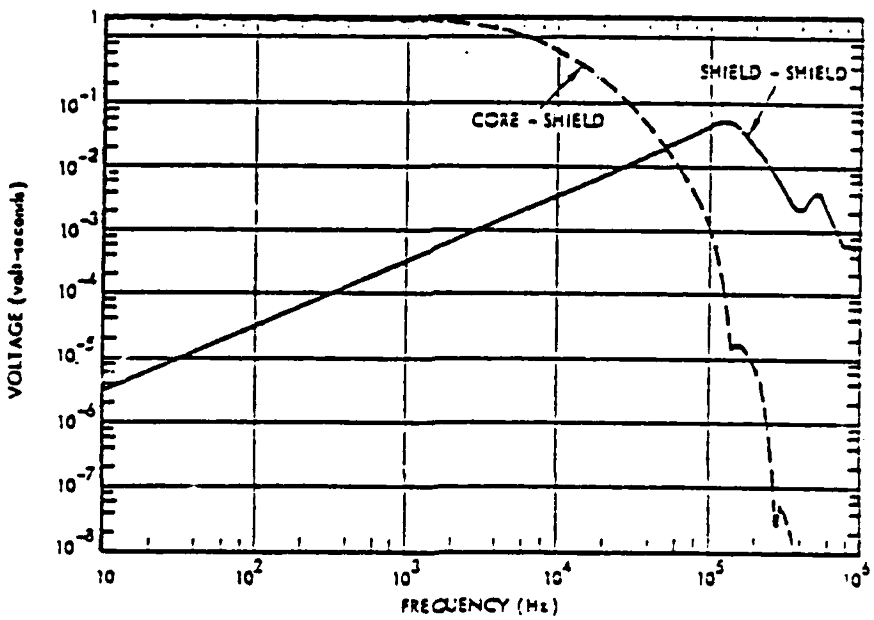


Figure 4.27 Voltage Responses to Unit Impulse [4.1]

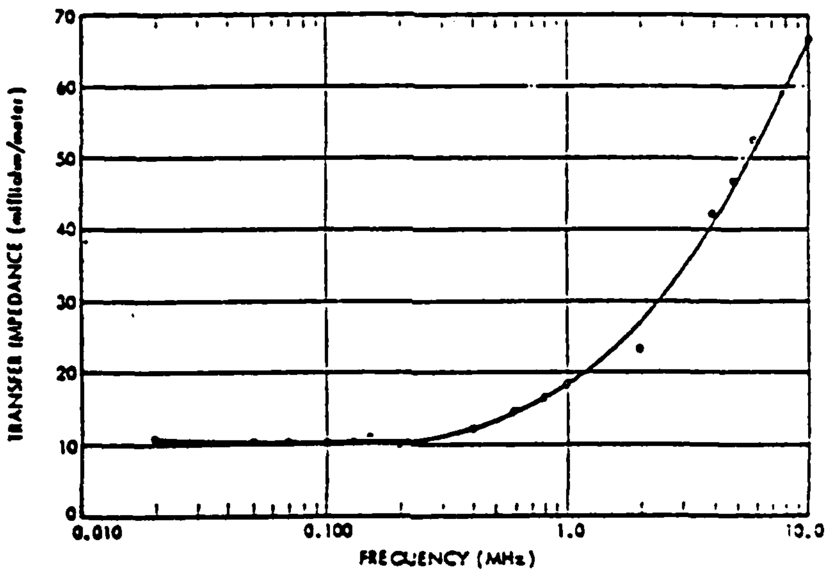


Figure 4.28 Transfer Impedance versus Frequency RG 62B/U [4.1]

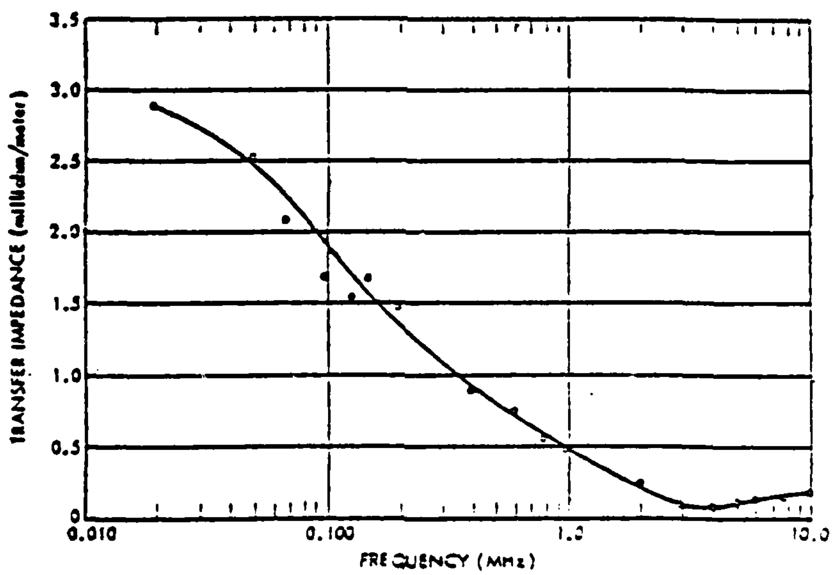


Figure 4.29 Transfer Impedance versus Frequency RG 13 A/U [4.1]

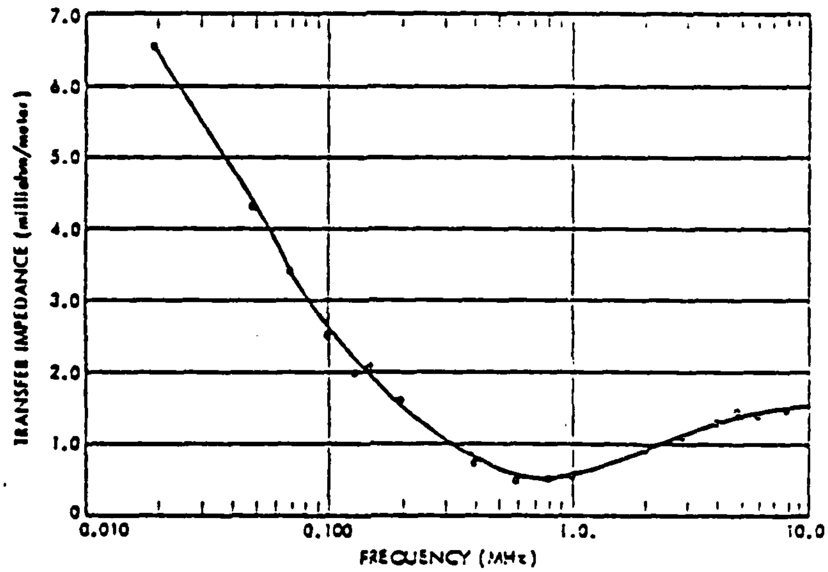


Figure 4.30 Transfer Impedance versus Frequency RG 58A/U Triax [4.1]

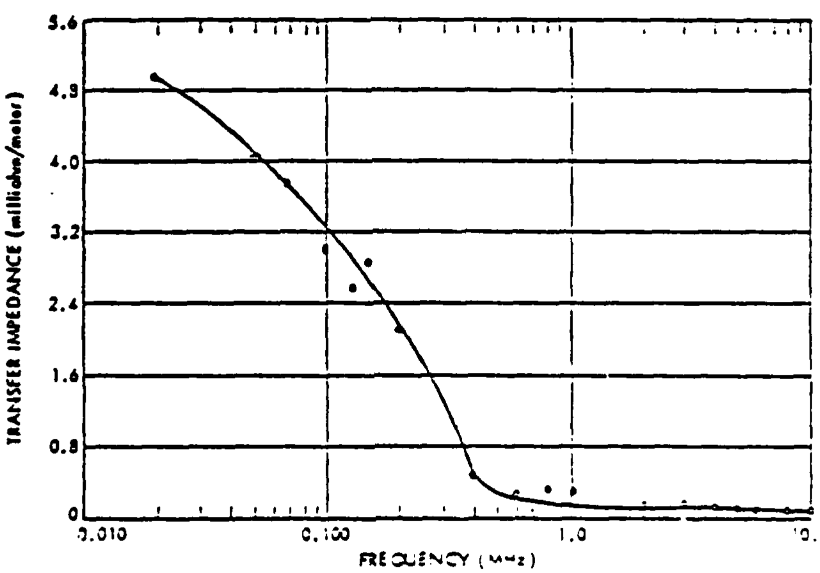


Figure 4.31 Transfer Impedance versus Frequency Solid Shield Cable [4.1]

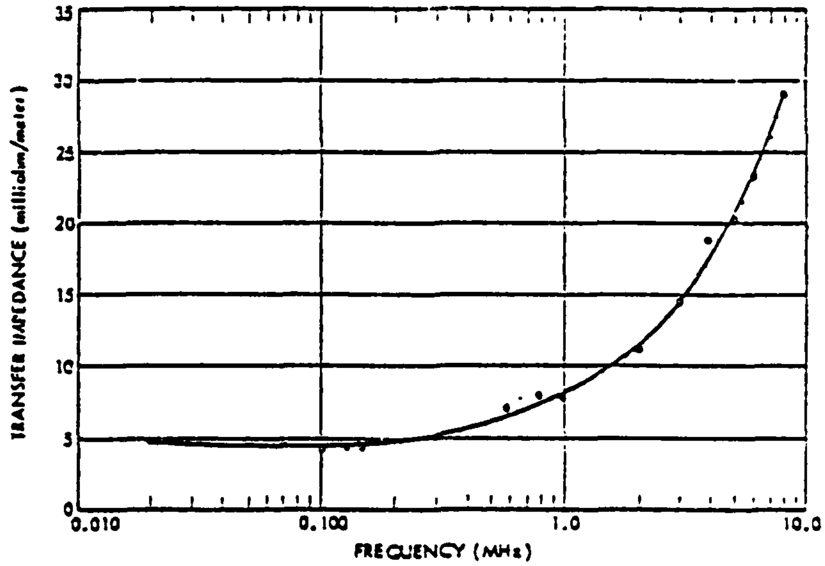


Figure 4.32 Transfer Impedance versus Frequency RG 12/U Armored (Armor Floating) [4.1]

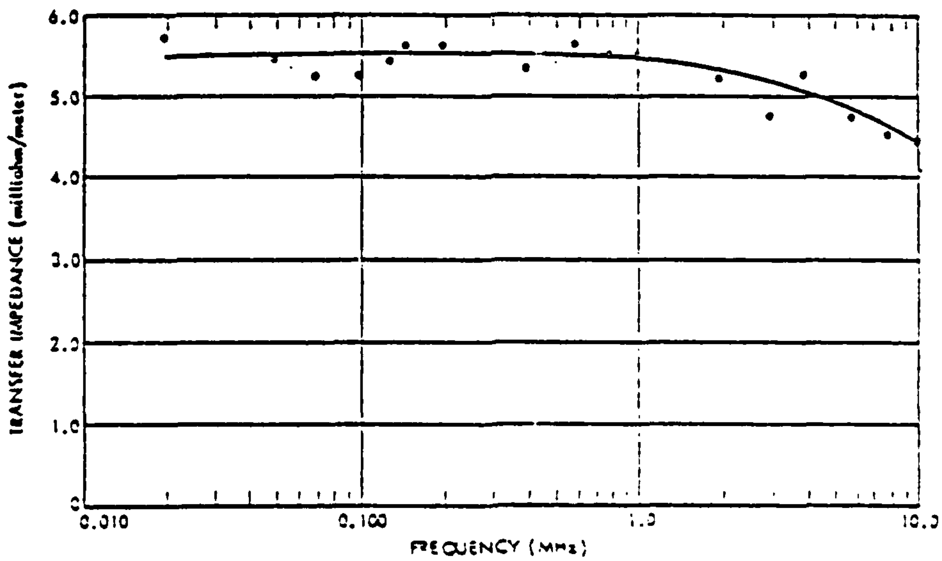


Figure 4.33 Transfer Impedance versus Frequency RG 12/U Armored (Armor Banded to Cable Shield at Ends [4.1]

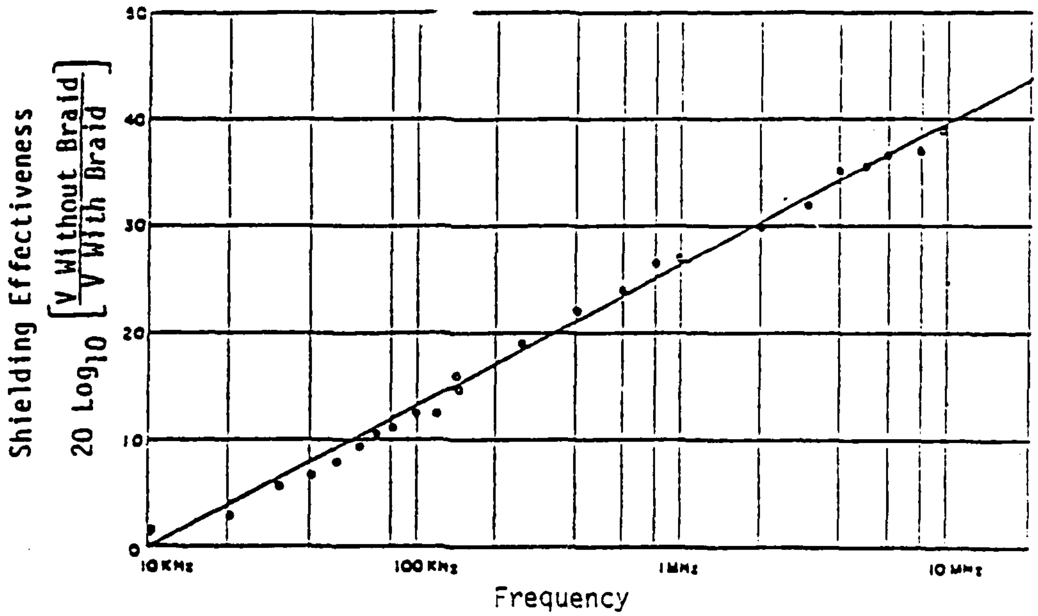


Figure 4.34 Shielding Effectiveness of Cylindrical Copper Braid from RG/18 with Loose Ends [4.6]

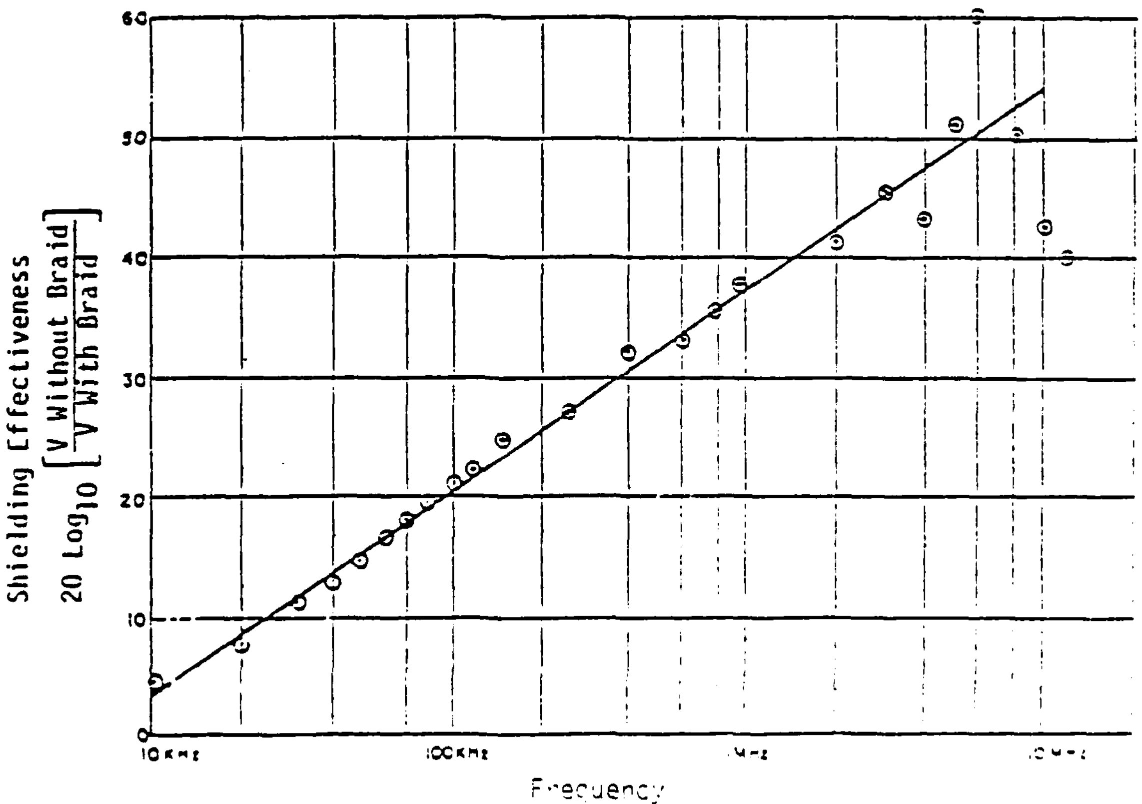


Figure 4.35 Shielding Effectiveness of Cylindrical Copper Braid from RG-18 with Circumferentially Soldered Ends [4.6]

low resistivity plastic cement made by Emerson and Cummings, ECCO BOND SOLDER 56C).

In measurements performed on the cable shields of RG/18 [4.6], the two shields (an outer aluminum braid, and an inner flexible copper braid) of 1 meter length of RG/18 were removed and the shielding effectiveness of each shield was measured separately. The measuring technique consisted of wrapping the shield around a glass tube which contained an internal magnetic loop pickup. This pickup was inserted between the plates of a parallel plate transmission line which was their energy source. The shielding effectiveness was defined as

$$20 \log_{10} \frac{\text{Loop Voltage Without Braid}}{\text{Loop Voltage With Braid}} \qquad (4.32)$$

Figure 4.34 shows the results obtained for copper braid with loose ends which approximated a long cable length. Figure 4.35 presents the results for the same shield with the ends circumferentially soldered to represent a short cable length. The results for a corroded aluminum outer braid are presented in Figure 4.36 which indicates that corrosion seriously degrades shielding effectiveness.

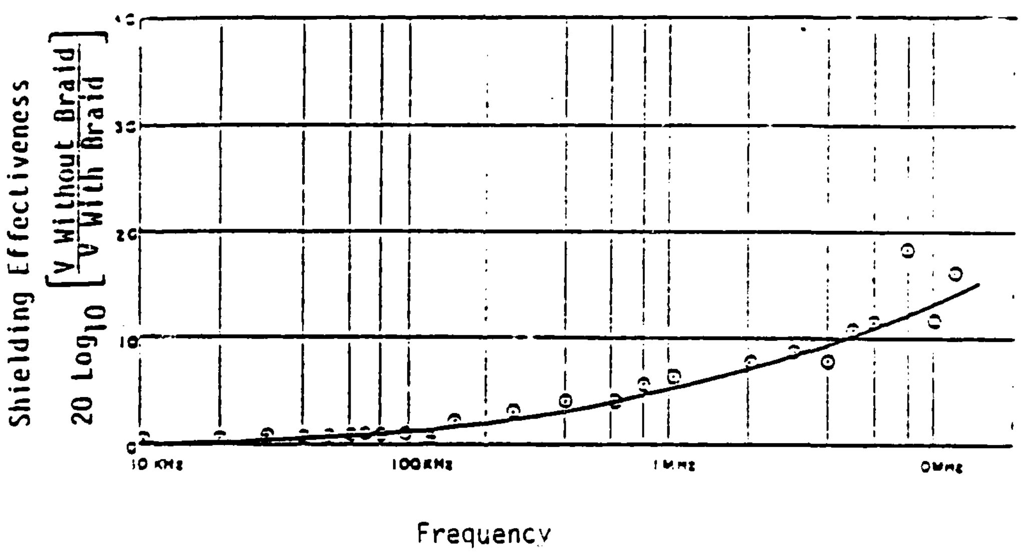


Figure 4.36 Shielding Effectiveness of Cylindrical Aluminum Braid with Loose Ends (with corrosion) [4.6]

In Reference 4.1, shielding effectiveness data for various solid shielded cables are related to RG-9 A/U which is a double braided silver plated cable commonly used by microwave test equipment manufacturers. RG-9 will probably respond as shown in Figure 4.6 for braided cables. These data (Figures 3.37 through 3.41) indicate that additional shields provide a substantial increase in shielding.

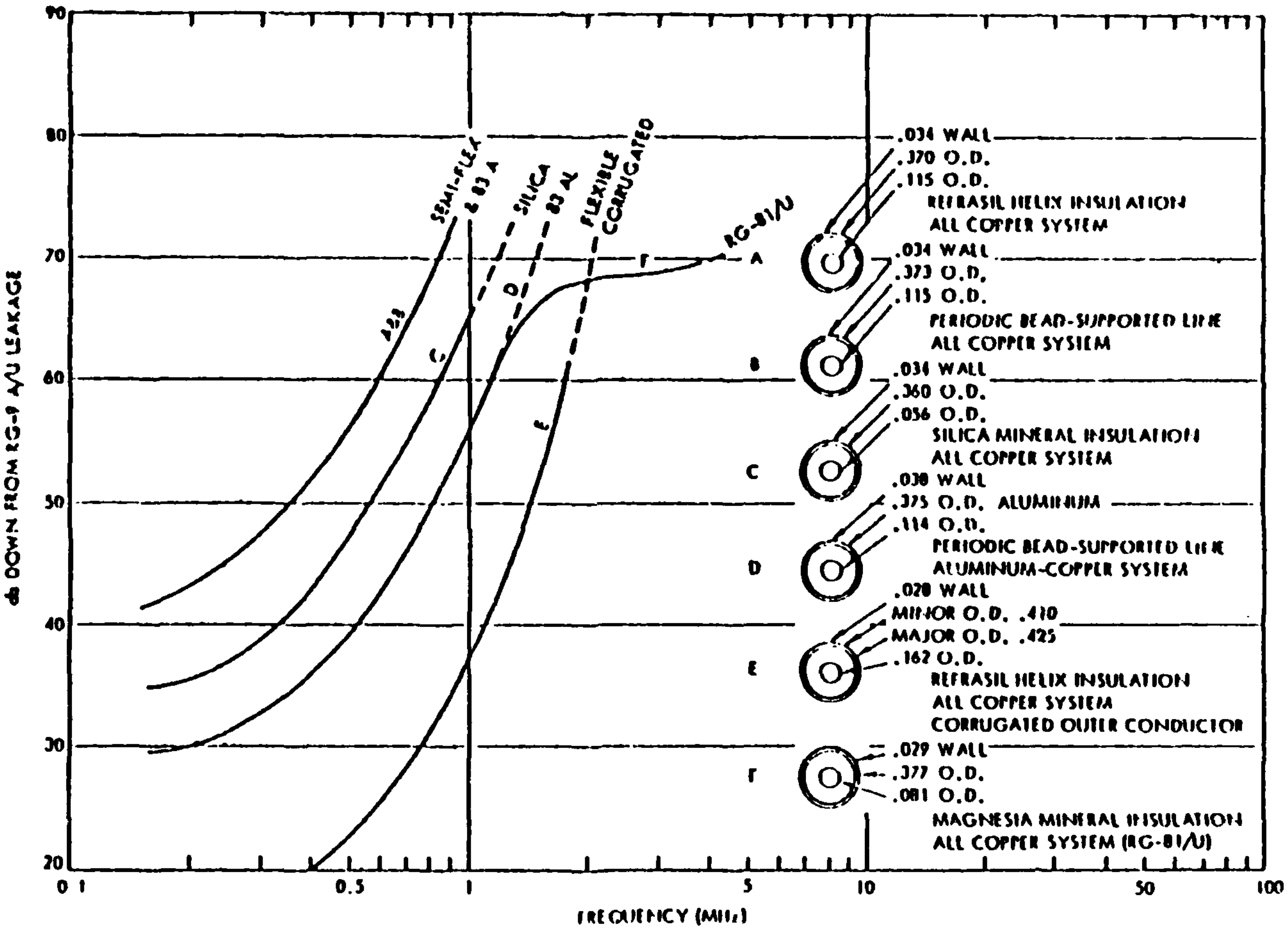


Figure 4.37 Relative Shielding Effectiveness of Solid Copper and Aluminum Sheaths for Various 3/8-inch O.D. 50-Ohm Coaxial Cables [4.1]

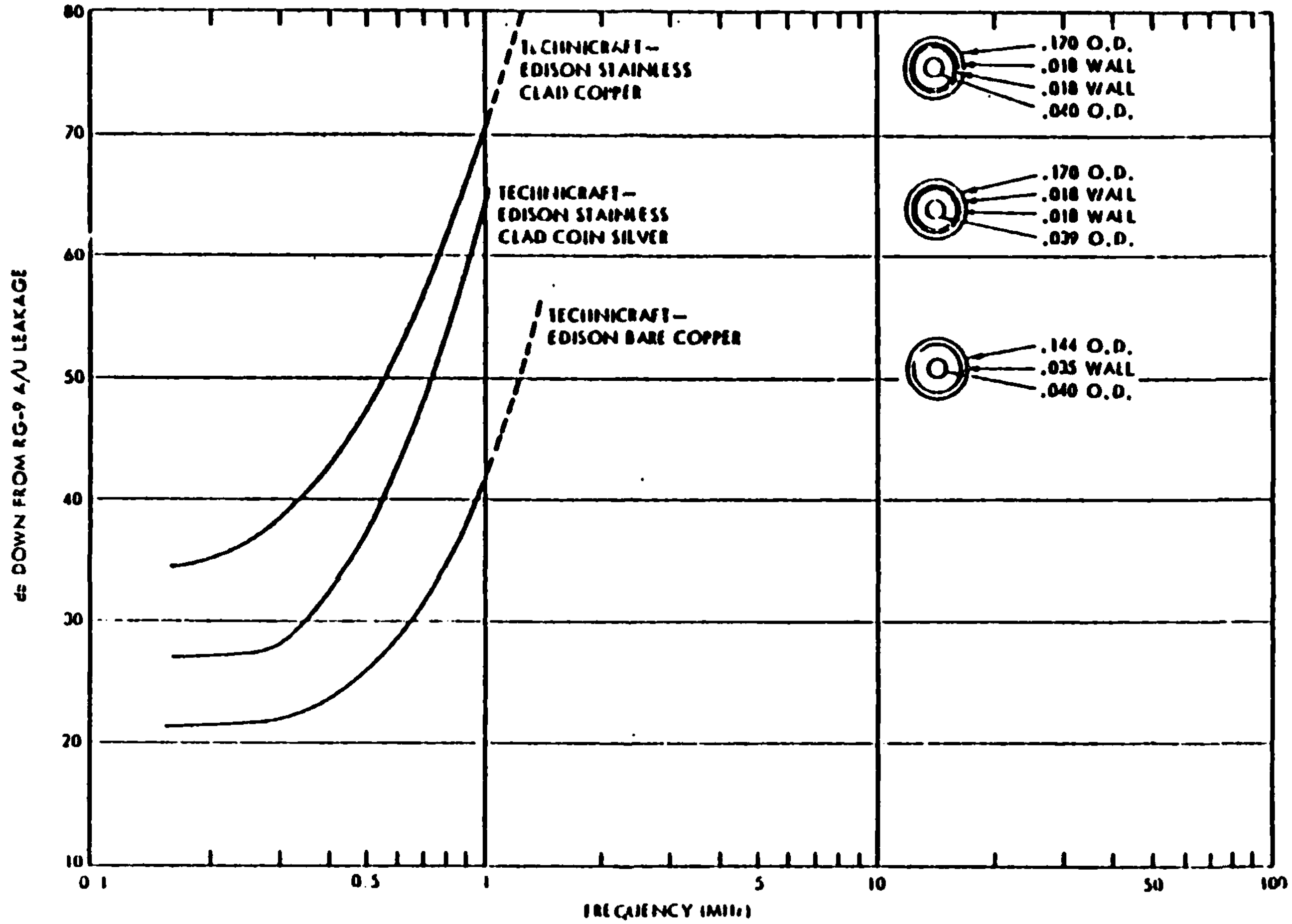


Figure 4.39 Relative Shielding Effectiveness of Stainless-Clad Copper and Stainless-Clad Coil Silver, 50-Ohm Mineral-Insulated Silica Cables [4.1]

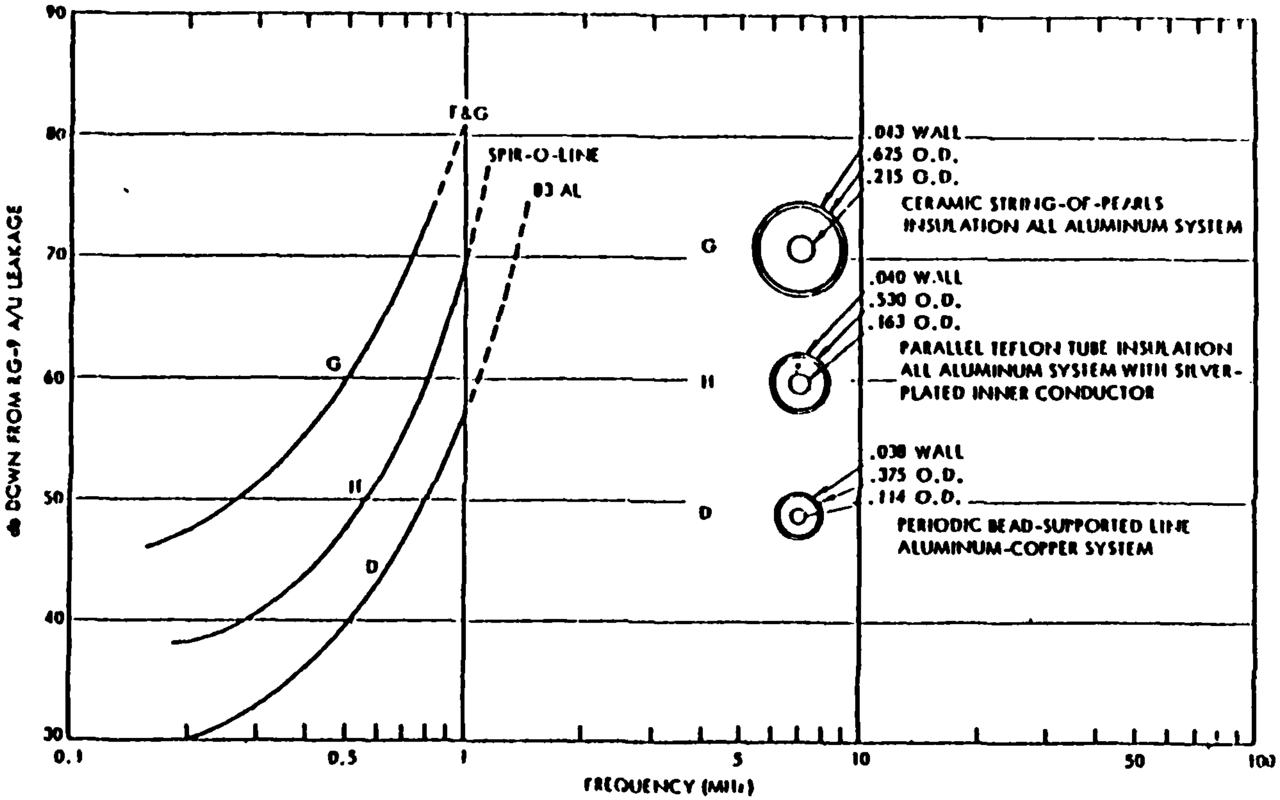


Figure 4.39 Relative Shielding Effectiveness of 50-Ohm, Solid-Aluminum, Sheathed Coaxial Cables of Different Diameters [4.1]

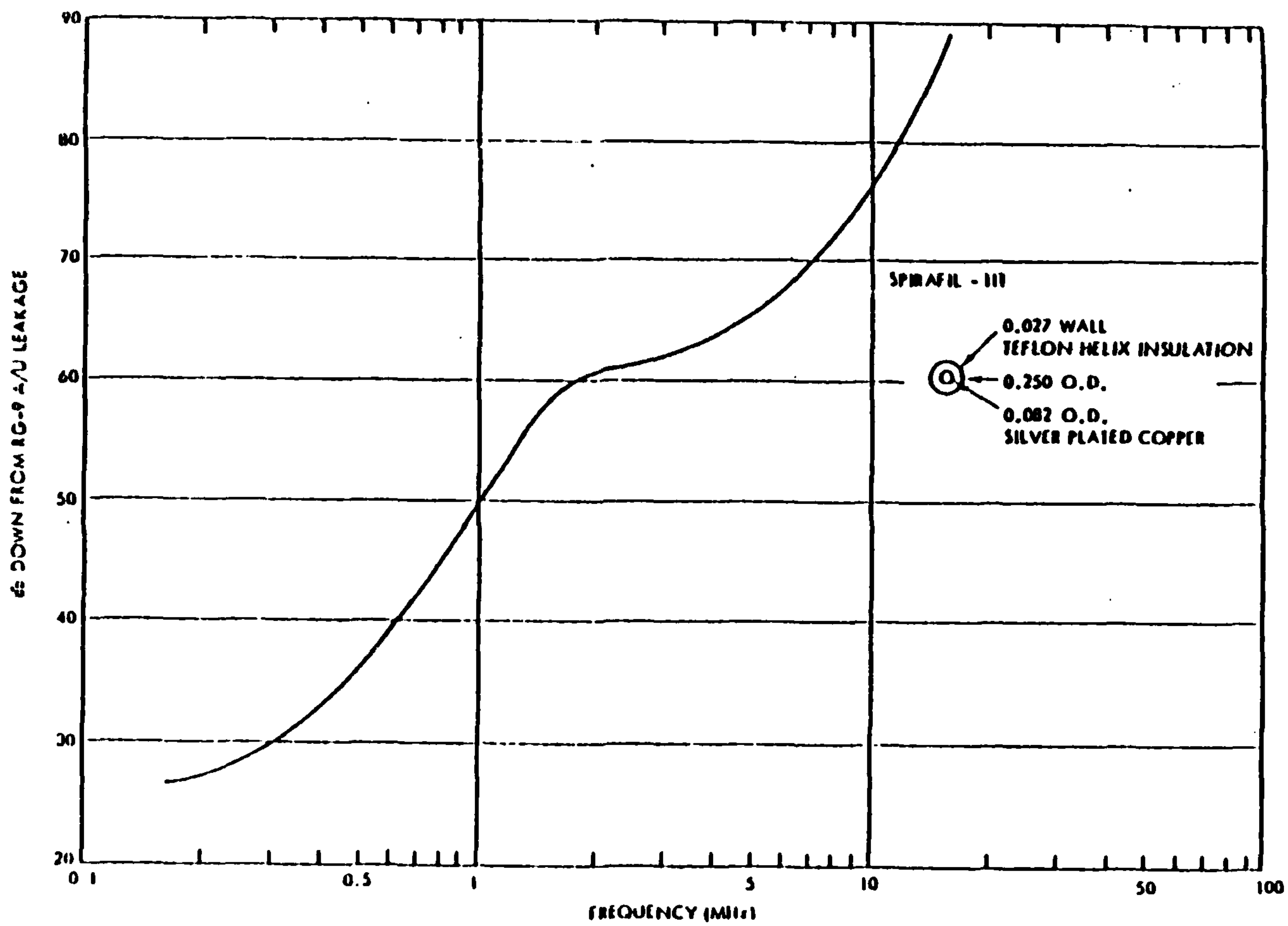


Figure 4.40 Relative Shielding Effectiveness of Nickel-Plated Copper Sheath [4.1]

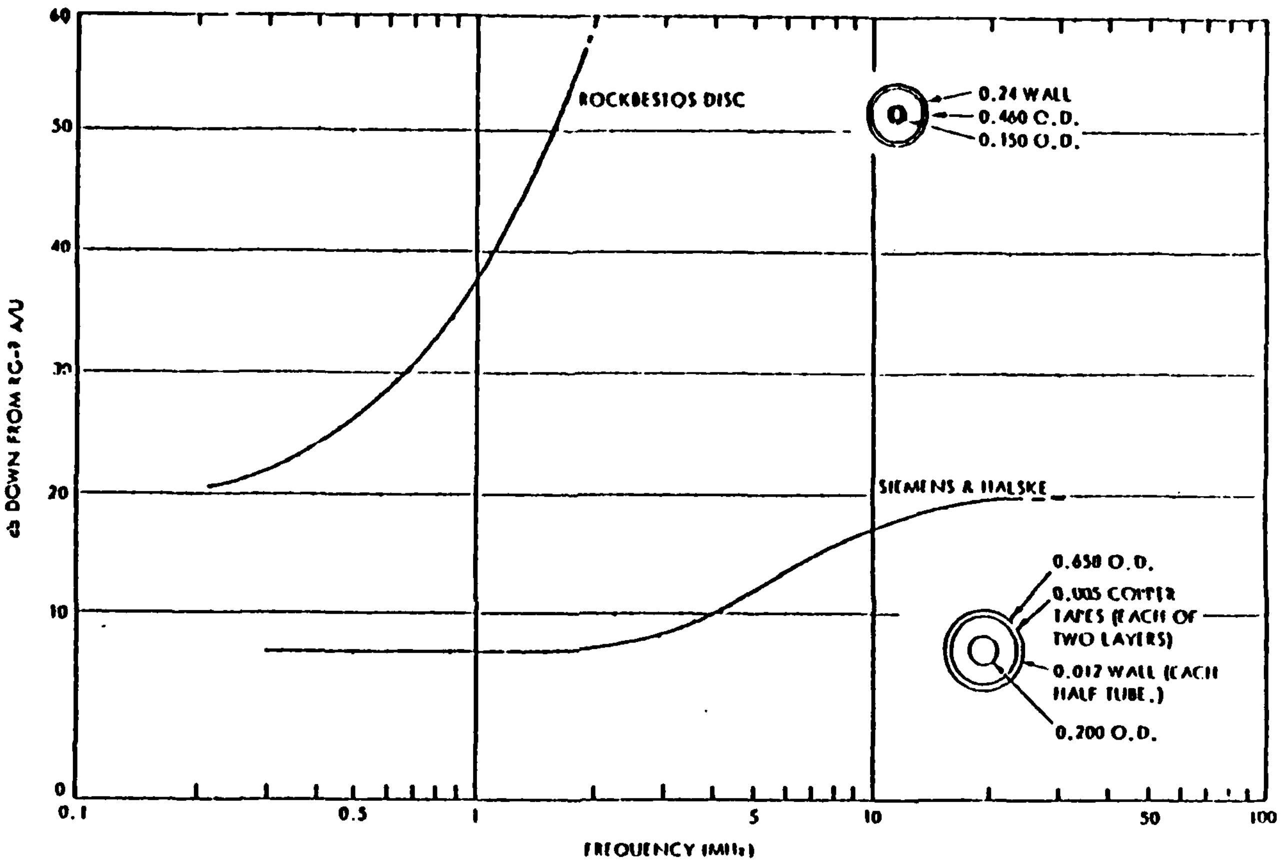


Figure 4.41 Relative Shielding Effectiveness of Disc-Shaped Coaxial Lines Employing (a) Solid Copper Sheath and (b) Two Corrugated Half-Tubes of Copper Sheathing Enclosed in Two Reverse Layers of Copper Tapes [4.1]

Ferromagnetic materials can provide added shielding because of their high relative permeabilities, but the effect of high permeability is limited by saturation levels. Therefore, the material thickness must be great enough to prevent complete saturation. The depth of saturation penetration for high permeability materials and sinusoidal excitation is given as [4.2]

$$p = \frac{1}{\pi}\sqrt{\frac{A}{\sigma B_s f a}} \tag{4.33}$$

where p is the depth of saturation penetration (m), A is the peak current amplitude (A), σ is the conductivity (mhos/m), B_s is the saturation flux (W/m^2), f is the frequency (Hz), and a is the outer shield radius (m). Table 4.6 shows values of σ and B_s for typical materials.

Table 4.6 High-Permeability Material Properties [4.2]

Material	Saturation Flux (W/m^2)	Conductivity (10^6 mhos/m)
Annealed Steel	2.1	10.0
Hipernom	0.75	1.6
Hipernik	1.6	2.0
Hiperco	2.42	4.0
45 Permalloy*	1.6	2.2
78 Permalloy	1.07	6.3
4-79 Permalloy	0.87	1.8
Supermalloy	0.8	1.7

*Similar properties for Nicaloi, 4750 alloy, Carpenter 49, Armco 48.

For example, a current peak of 1000 A at a frequency of 10 mHz in 0.01-m radius Hipernom ($\sigma = 1.6 \times 10^6$ mhos/m and $B_s = 0.75\ W/m^2$) results in a depth of saturation penetration of 2.9×10^{-5} m or about 1 mil.

A similar approximation can be used for pulses

$$p = \sqrt{\frac{Q}{\pi \sigma B_s a}} \tag{4.34}$$

where Q is the current-time integral of the pulse (A-sec).

Increases in attenuation at low excitation levels result from energy stored in the magnetic field in the material. When the material is completely saturated, some attenuation remains because it is still a good conductor of finite thickness.

Table 4.7 contains a summary of cable shielding material [4.7].

4.2.8 Example of Using the Transfer Impedance Concept in Choosing the Cable

Consider the case of an exterior cable connecting critical equipment on an unhardened destroyer class ship. This means that the current on the cable shield can be 60 times the current on the inner conductor (pin current). From (4.4), the transfer impedance of the cable must be chosen such that

$$|Z_T| \le \left|\left(Z_0 + Z_\ell + j\omega \frac{Z_c \ell}{c}\right)\right| / 60\ell \tag{4.35}$$

where ℓ is the length of the exterior cable, Z_c is the characteristic impedance of the cable, Z_0 is the impedance of the source, and Z_ℓ is the impedance of the load. If $Z_0 = Z_\ell = Z_c = 50\Omega$ and recalling that ($\ell \ll 2\pi c/\omega$), the transfer impedance must be

$$|Z_T| \le \frac{5\Omega}{3\ell} . \tag{4.36}$$

This says that the longer the cable, the greater the shielding must be.

For a 100 m cable, the transfer impedance must be less than 17mΩ/m. This would correspond to using a high quality single shielded cable or possibly a multiply shielded cable. It should be warned that this analysis assumes that the connectors used play no significant part in coupling exterior cable currents in the inner conductors.

4.3 Cable Connectors

4.3.1 Transfer Impedance and Shielding Effectiveness

Cable connectors interface cables to other cables and cables to equipment. Most rf connectors shield the inner conductors (pins) with a solid shield. Nevertheless, there are three or more locations where electrical contact is weak. That is, the cable shield can make poor electrical contact with the connector shield and the connector plug can make poor electrical contact with the socket. Also, the backshell can make poor connection with plug/receptacle. In any case, spurious currents and/or voltages are induced on the inner conductor(s) due to leakage at these discontinuities. Note these source terms differ from those discussed in (4.1) and (4.2) in that they are point (highly localized) source terms.

The source terms that drive the inner conductors can be determined from the transfer impedance. The point voltage sources are determined from the lumped parameter transfer impedance Z_T times the connector current I_c, i.e.

$$V_s(\omega) = Z_T(\omega)\, I_c(\omega) . \tag{4.37}$$

Table 4.7 Comparison of Shielding Materials [4.7]

	Probable Shielding Effectiveness	Probable Durability In Vibration	Probable Corrosion Resistance	Relative Weight	Probable Contact Resistance	Tensile Strength	Relative Cost	Other Comments
Solid Shields	>110 dB	-	-	-	-	-	-	
Ferromagnetic								
Permalloy, Hipernom	Excellent	Questionable	Excellent	Thin/Light	High	High	High	
Steel	Excellent	Questionable	Poor	Thin/Light	Moderate	High	Low	
Non-Magnetic								
Aluminum	Excellent	Fair	Poor	Light	High	Low	Low	
Copper	Excellent	Good	Fair	Heavy	Low	Low	Moderate	
Brass	Excellent	Good	Fair	Heavy	Moderate	Moderate	Moderate	
Braid Shields (Single Layer)	20-50 dB	-	-	-	-	-	-	See Notes 1 and 2.
Tinned Copper	Excellent	Excellent	Excellent	Moderate	Low	Low	Low	
Nickel Plated Copper	Excellent	Excellent		Moderate	Low	Low	Low	
Monel	Good	Questionable	Excellent	Moderate	Low	High	Moderate	
Nickel	Good	Good	Excellent	Moderate	Low	High	Moderate	
Aluminum	Excellent	Poor	Poor	Light	High	Low	Low	
Stainless Steel	Good	Questionable	Excellent	Moderate	High	High	Moderate	
Multilayer Braid Shields								
Double-Braid	70-100 dB	-	-	Heavy	-	-	Moderate	See Notes 1 and 2.
Triple-Braid	90-120 dB	-	-	Very Heavy	-	-	High	See Notes 1 and 2.

NOTE: 1. Optimum braid weave angles are in the range of 30-45 degrees.
2. Braid optical coverage should be 85 percent or better.

There are no significant current source terms if the connector provices 100% optical coverage. However, there are instances when less than 100% optical coverage can arise because of poor installation of the connector.

Some typical values for the lumped parameter transfer impedance are shown in Table 4.8 where R_0 and M_{12} are related to the transfer impedance by

$$Z_T = R_0 + j\omega M_{12} \tag{4.38}$$

The shielding effectiveness for connectors (like cables) is defined in many varying ways. For this reason care should be taken when using shielding effectiveness tables and graphs. Hence, a single general relationship between shielding effectiveness and transfer impedance is not within the scope of this handbook. However, shielding effectiveness measurements made using the same test fixture, loads, etc. are commonly used in the industry to compare connectors. Although shielding effectiveness information is not amenable for determining transient voltage levels developed on cables, the concept is useful in comparing connector types to one another. This will be discussed later in subsection 4.3.3 where connector types are compared using the shielding effectiveness concept.

4.3.2 Measured Transfer Impedance of Navy Cable Connectors

This subsection describes results of a testing effort to measure the transfer impedance of a number (13) of cable connectors in use by the U.S. Navy [4.11]. The objective was to determine the EMP protection provided by various connector configurations and materials.

The tests were performed using the triaxial test fixtures and swept continuous wave (CW) test procedures described in Section 10.2 for measuring the surface transfer impedance of cable shields.

The connectors which were tested are made up from three separate parts - a shell, a plug and a socket. The Military Specification (MS) part numbers for the shell-plug-socket combinations which were tested are given in Table 4.9. All parts are in the MS3400 series which are used for shipboard jacketed cable applications only. Also included in the table are the cable types which were used with the connectors and the code number which is used to identify the connector on the test result curves.

For EMP protection, a connector must provide a low impedance path for current flow from the cable shield to the external side of the bulkhead and must maintain shielding integrity so that energy induced on the cable shield will be dumped outside the compartment which the cable is entering. Factors which determine the connector impedance and shielding integrity are 1) shape and size, 2) method by which the cable shield is attached to the connector shell, 3) material and finish, 4) contact maintained through threaded or other connections, and 5) the method by which the socket is attached to the bulkhead.

The shape and size of the connector will contribute to resistance (surface area) and inductance. Calculation of the impedance as a function of shape is extremely difficult and has not been attempted.

Table 4.8 Resistance and Mutual Inductance of Cable Connectors [4.4]

Connector	Identification	R_c (ohms)	M_{12} (H)
Multipin Aerospace connectors (Threaded)	Burndy NAS-15863	0.0033	$5.[illegible] \times 10^{-11}$
	Deutch 38068-10-5PN	0.15	2.5×10^{-11}
	Deutch 38068-18-31SN	0.005	1.6×10^{-10}
	Deutch 38060-22-55SN	0.023	1.1×10^{-10}
	Deutch 38068-14-7SN	0.046	5.0×10^{-11}
	Deutch 38060-14-7SN	0.10	8.2×10^{-11}
	Deutch 38050-14-7SN	0.023	6.7×10^{-11}
	Deutch 38068-12-12SN	0.0033	3.0×10^{-11}
	Deutch 38066-12-12SN	0.012	1.3×10^{-11}
	Deutch 38066-12-12SN	0.012	1.3×10^{-11}
	Deutch 38060-12-12SN	<0.001	2.5×10^{-12}
	Deutch 38068-12-12SN	0.014	3.5×10^{-11}
	AMP	0.0067	1.6×10^{-11}
	AMP	0.0057	1.5×10^{-11}
	AMP	0.0033	1.9×10^{-11}
Type N	UG 218/U-UG58A/U	*	*
Type BNC (Bayonet)	UG 88C/U-UG1094/U	0.002	$4\text{-}8 \times 10^{-11}$
Anodized	MS 24266R-22S-55	5×10^{4}	$\omega M < R_c$ @ 20 MHz
Open shell	MS 3126-22-55	0.5-1	$\omega M < R_c$ @ 20 MHz
Split shell	MS 3100-16S-1P MS 3106A-	0.001	$\approx 20 \times 10^{-11}$

*Too small to measure in presence of 4 inches of copper tube used to mount connector

Table 4.9 Code Identification for Shell-Plug-Socket Combinations [4.11]

Code Designation	Cable Type	Number of Wires	Wire Gauge	Shell Type	Plug Type	Socket Type
1	MS-37	37	16	MS-3437A-134A	MS-3406D-40-56P	MS-3402D-40-56S
2A	DSS-4	2	12	MS-3437B-31A	MS-3406D-20-4P	MS-3402D-20-4S
2B	DSS-4	2	12	MS-3437B-31A	MS-3406D-20-4P	MS-3404D-20-4S
3A	DSS-4	2	12	MS-3437A-31A	MS-3406D-20-4P	MS-3402D-20-4S
3B	DSS-4	2	12	MS-3437A-31A	MS-3406D-20-4P	MS-3404D-20-4S
4	FSS-4	4	12	MS-3437B-39A	MS-3406D-22-23P	MS-3402D-22-23S
5	FSS-4	4	12	MS-3437A-39A	MS-3406D-22-23P	MS-3402D-22-23S
6	2SJ-7	2	8	MS-3437A-39A	MS-3406D-22-22P	MS-3402D-22-22S
7A	DSS-4	2	12	MS-3437A-31S	MS-3406DS-20-4P	MS-3402DS-20-4S
7B	DSS-4	2	12	MS-3437A-31S	MS-3406DS-20-4P	MS-3404DS-20-4S
8A	DSS-4	2	12	MS-3437A-31D	MS-3406DT-20-4P	MS-3402DT-20-4S
8B	DSS-4	2	12	MS-3437A-31D	MS-3406DT-20-4P	MS-3404DT-20-4S
9	2SWU-1	2	16	MS-3437B-11A	MS-3406D-10SL-3P	MS-3402D-10SL-3S

Discontinuities in the current flow path result in increased resistance and breaking of shield integrity. One such discontinuity occurs at the connection between the cable shield and the shell. Pressure connection between cable shield and shell unavoidably results in some contact resistance. When such a pressure connection is not provided in the shell design, the cable shield must be connected back to the cable clamp via a wire. The inductance associated with this wire contributes greatly to overall connector impedance and radiation of energy to the cable core conductors. These shield termination methods are illustrated in Figure 4.42. The "Extended Shield Conductor" shown in the figure was used to provide an additional shield termination in the tests.

A second discontinuity in the current flow path occurs at the threaded connections. The degree of contact obtained in threaded connections is a strong factor in determining the resistance and energy leakage of the connector and is dependent on mechanical design (shoulder, thread and seat), torque used when tightening the connection, and finish on the material.

A third discontinuity which contributes to resistance and energy leakage is mounting of the socket to the bulkhead. For flange mounting, a socket surface to bulkhead surface discontinuity exists. For jam nut mounting, the socket thread to jam nut and jam nut surface to bulkhead surface interfaces both contribute to overall discontinuity.

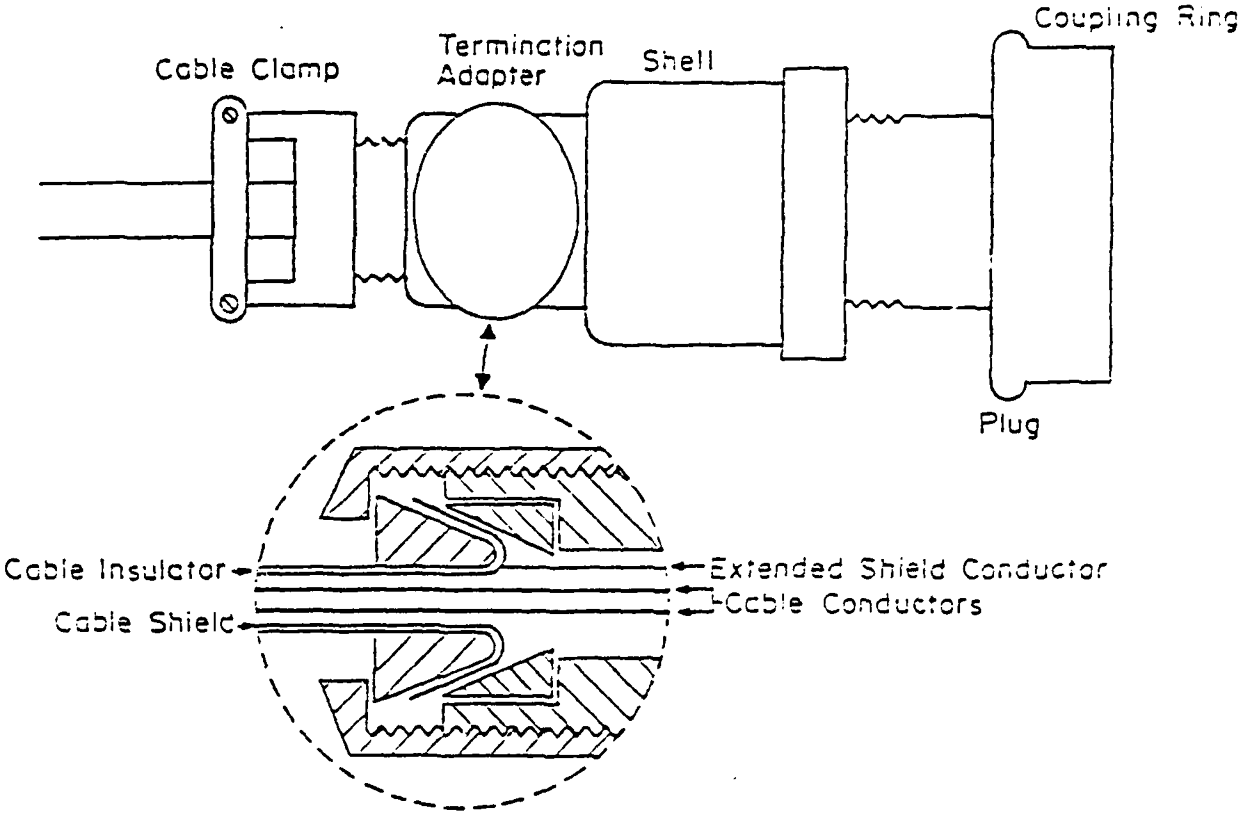
Table 4.10 lists some of the properties of the connectors which were tested that effect their electrical characteristics. These properties include the material and finish of the parts, provision for electrical termination of the cable shield on the shell, and the mechanical mounting of the socket. All illustrated in the table, the connectors which were tested encompass a number of combinations of materials, finish, shield termination and socket mounting methods.

The transfer impedance magnitude for all connectors with the exception of #5 are presented in Figures 4.43 and 4.44. It was found that the socket mounting method does not have a significant effect on the measured value of Z_T. The results obtained for connector #5 are discussed separately for the other connectors.

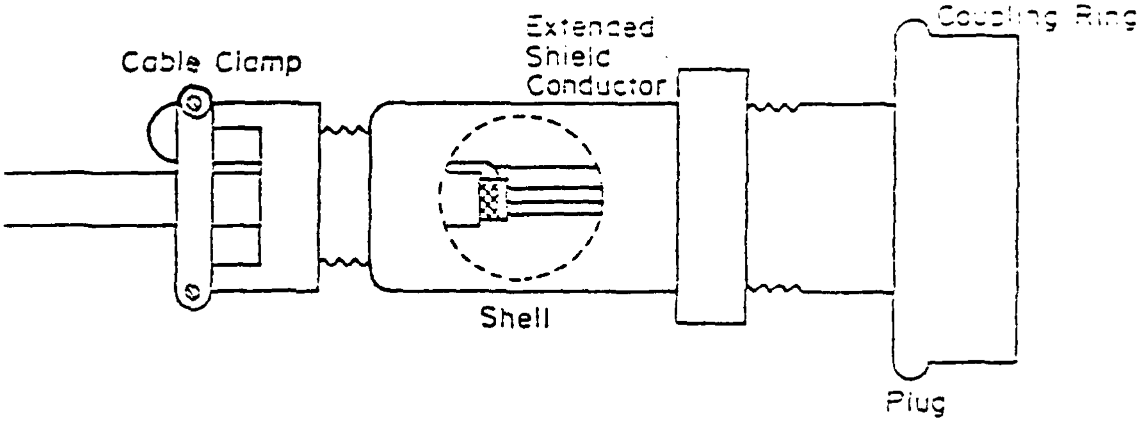
In the tests on the connectors, two shield connection methods were used (see Figure 4.42). When the extended shield conductor is floating, the cable shield is connected externally (to the connector shell). When the extended shield conductor is connected, the cable shield is grounded externally and internally.

The curves of Figure 4.43 for which the cable shield is connected externally show the marked superiority of connectors for which the cable shield is terminated on the connector shell. Connectors #2A, #2B, #4 and #9 all require a conductor connected between shield and cable clamp for cable shield termination. The inductance that this lead adds to the impedance of the surface current path and the radiation from this lead (effectively a loop) results in a substantial increase in the value of Z_T.

When the extended cable shield is connected to provide an external and internal connection for the cable shield, a reduction in Z_T results. This is because of the reduction of current flow on the connector because another current path has



Shield Terminated On Shell (Type A Shell)



Shield Connected To Cable Clamp (Type B Shell)

Figure 4.42 Shield Connecting Methods [4.11]

Table 4.10 Shell- Plug- Socket Description [4.11]

Code Designation	Material	Finish	Cable Shield Terminated on Shell	Socket Mount
1	Aluminum	Cadmium plate over nickel	Yes	Flange
2A	Aluminum	Cadmium plate over nickel	No	Flange
2B	Aluminum	Cadmium plate over nickel	No	Jam Nut
3A	Aluminum	Cadmium plate over nickel	Yes	Flange
3B	Aluminum	Cadmium plate over nickel	Yes	Jam Nut
4	Aluminum	Cadmium plate over nickel	No	Flange
5	Aluminum	Cadmium plate over nickel	Yes	Flange
6	Aluminum	Cadmium plate over nickel	Yes	Flange
7A	Stainless Steel	Chromate Plate*	Yes	Flange
7B	Stainless Steel	Chromate Plate*	Yes	Jam Nut
8A	Ferrous Alloy	Cadmium Plate	Yes	Flange
8B	Ferrous Alloy	Cadmium Plate	Yes	Jam Nut
9	Aluminum	Cadmium plate over nickel	No	Flange

* Shell is not plated.

See Tables 4.9 and 4.10 for Code Number Identification

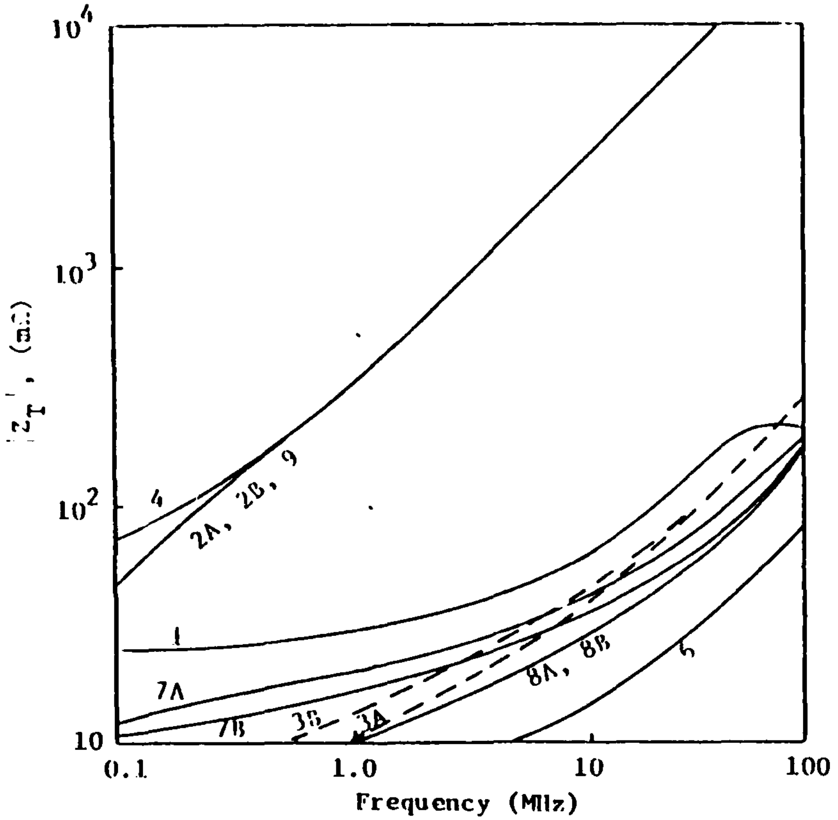


Figure 4.43 Connector Transfer Impedance Amplitude with Cable Shield Connected Externally [4.11]

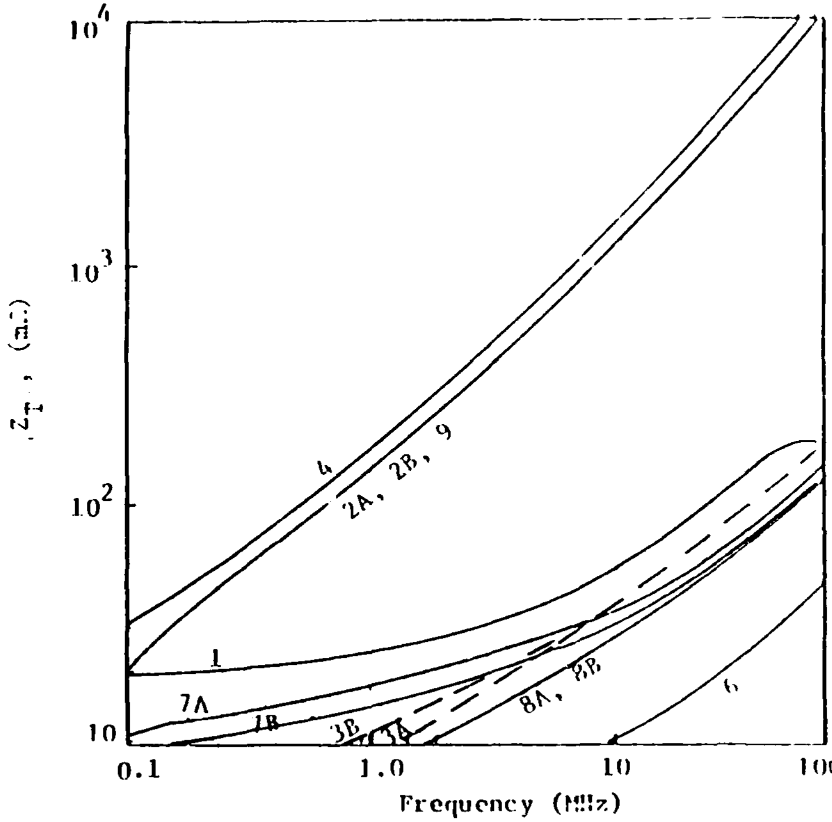


Figure 4.44 Connector Transfer Impedance Amplitude with Cable Shield Connected Externally and Internally [4.11]

been provided. However, this additional current path allows energy flow directly from the cable shield to the internal side of the bulkhead (the compartment). Paths which bring energy from external to internal areas must be avoided to obtain specified levels of EMP protection.

The effects of repeated connecting of the connectors and whether or not the connector shell is grounded are shown in Figures 4.45 and 4.46, respectively. From these results, the unnecessary reconnection of connectors is not recommended.

4.3.3 Supplemental Measured Transfer Impedances of Cable Connectors

In subsection 4.3.2, some of the problems associated with attaching the cable shield to the connector and grounding the connector were discussed. Added in this subsection are the problems associated with the connector plug - connector socket interface. Both problems can be alleviated by achieving low impedance electrical contacts.

Reference 4.16 presents shielding effectiveness as a function of coupling torque for the NAS 1599 multipin threaded connector in a vibration environment. The shielding effectiveness is defined as

$$S.E. = 20 \log_{10} \frac{I_1}{I_2} , \qquad (4.39)$$

where I_1 is the current in the connector shell, and I_2 is the current induced on the center conductor. The results are shown in Figures 4.47 through 4.52. Figures 4.47 through 4.49 show shielding effectiveness as a function of torque for the size 10 and 12 connectors and also for the size 10 connectors with rf fingers. About 20 dB may be gained in some cases by the use of higher torque than can be obtained by hand. Rf fingers can add up to 20 dB more shielding. The frequency of the measurements was in the range of .5 to 50 MHz.

The connectors were tested under the vibration environment given in Figure 4.50. The results are given in Figures 4.51 and 4.52 for the size 10 and 12 connectors. respectively. Vibration degrades the shielding effectiveness of the size 10 connector as much as 15 dB at low torque levels, while there is no degradation at torque levels above 80 in-lb. Shielding effectiveness of the size 12 connector is degraded 60 dB at hand-tight levels and between 5-10 dB at torque levels above 100 in-lb. These experiments show that hand-tightening NAS 1599 connectors is not sufficient and that additional torque is needed.

4.3.4 Example of Using the Transfer Impedance Concept in Choosing the Cable Connector

Let's again consider the case of an exterior cable connecting critical equipment on an unhardened destroyer class ship. Let's assume that the cable connector connects two cables. The loads on either side of the connector are the characteristic impedances, Z_c. Thus the low frequency transfer impedance of the connector can be expressed by the expression similar to (4.35)

See Tables 4.9 and 4.10 for Code Number Identification

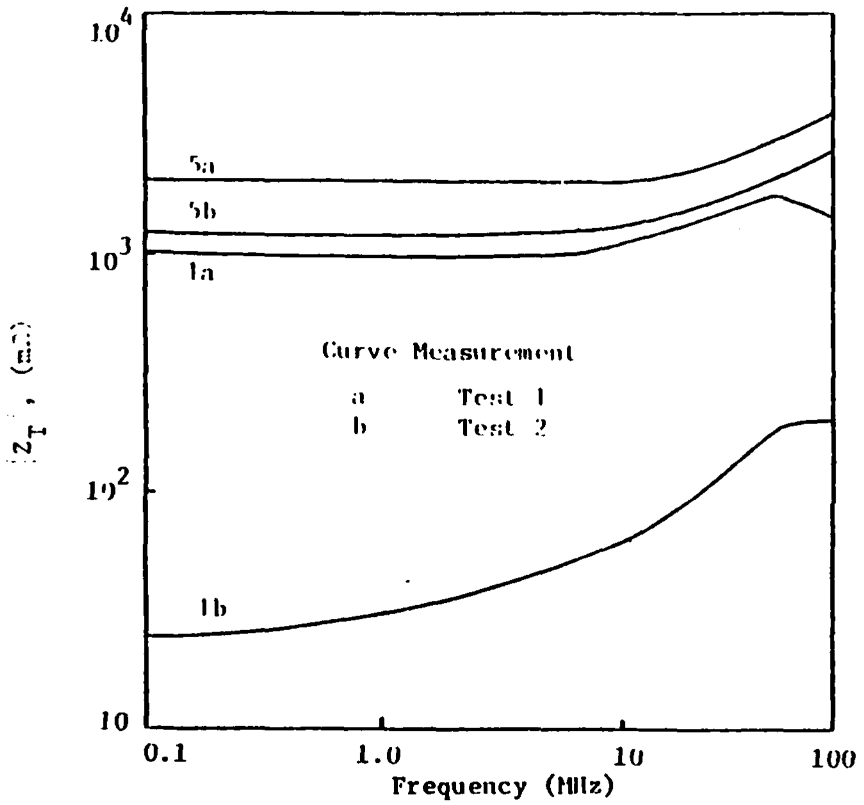


Figure 4.45 Variation of Transfer Impedance Amplitude when Connectors are Disconnected and Reconnected Between Tests [4.11]

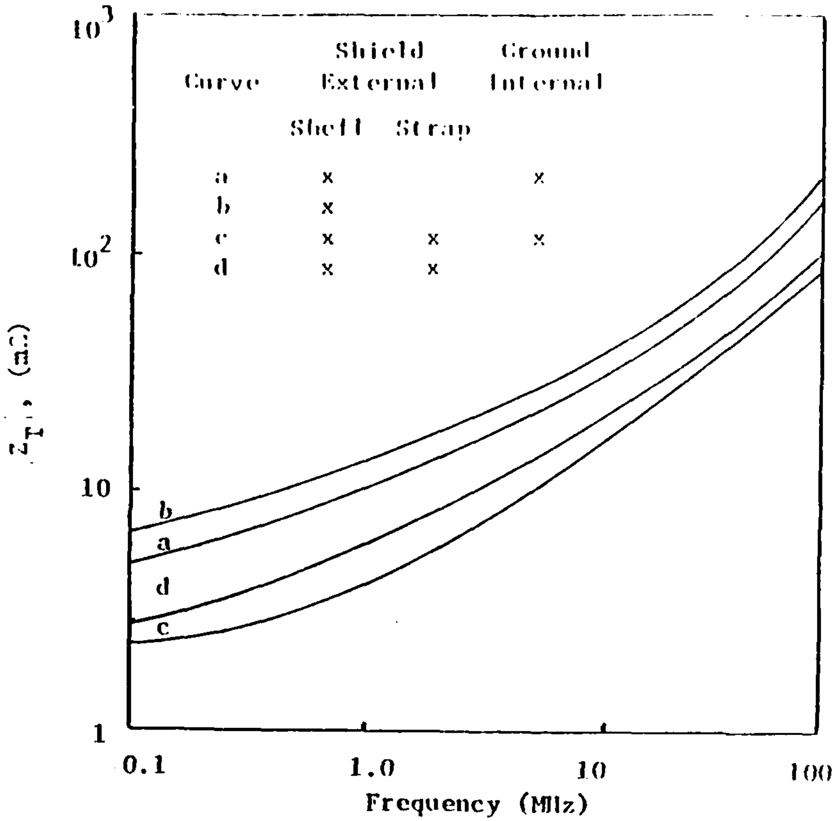


Figure 4.46 Transfer Impedance Amplitude of Connector 3A for Different Shield Grounding Methods [4.11]

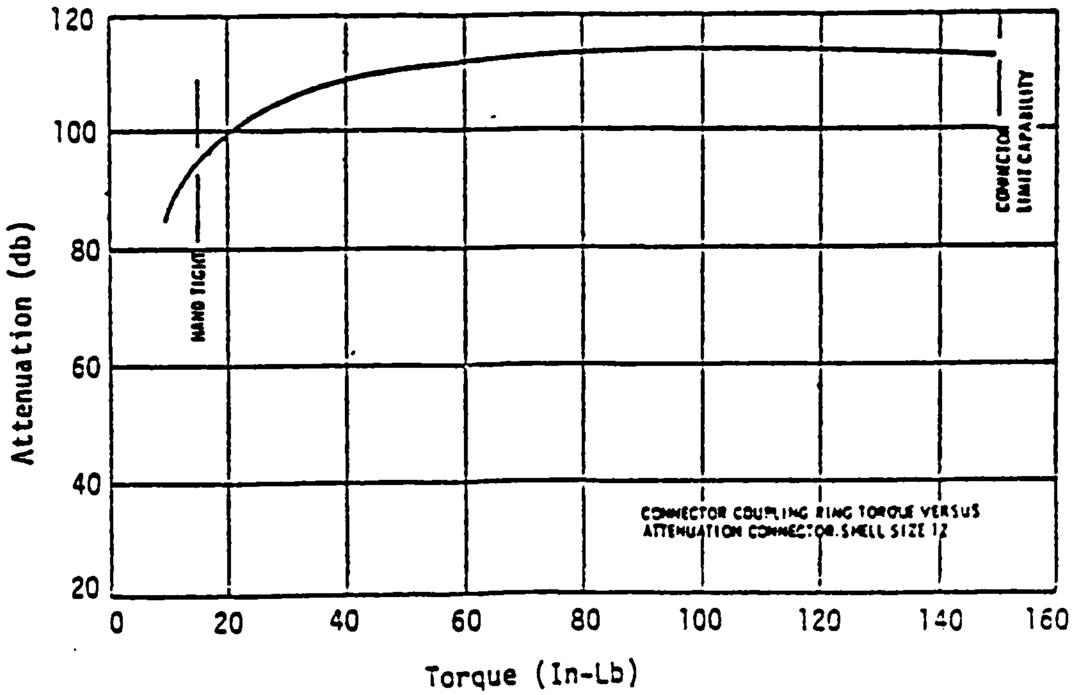


Figure 4.47 Static Test [4.16]

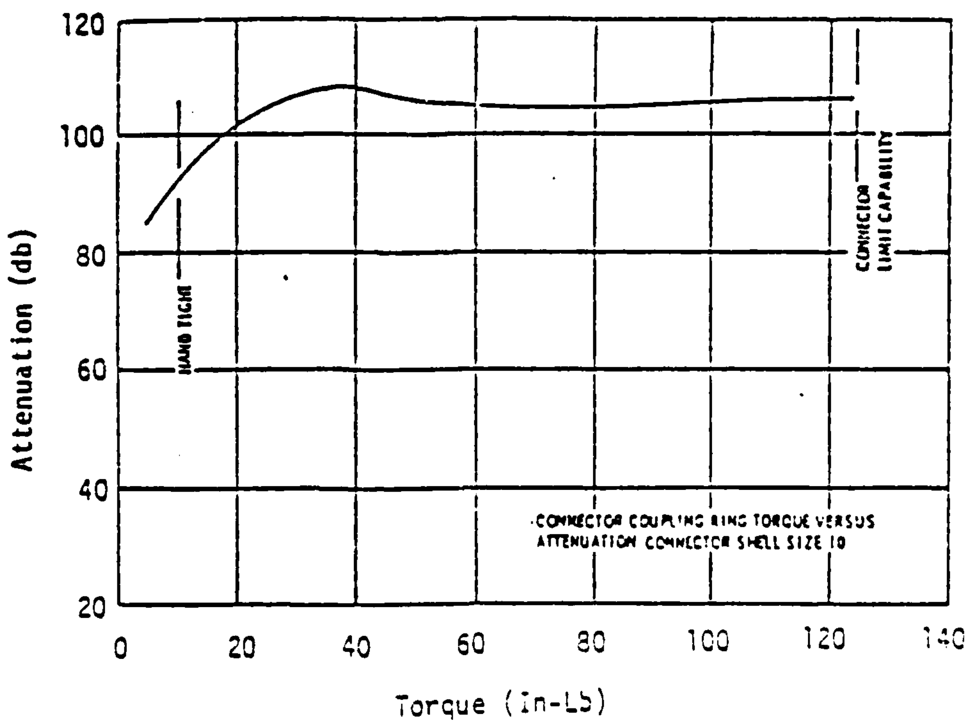


Figure 4.48 Static Test [4.16]

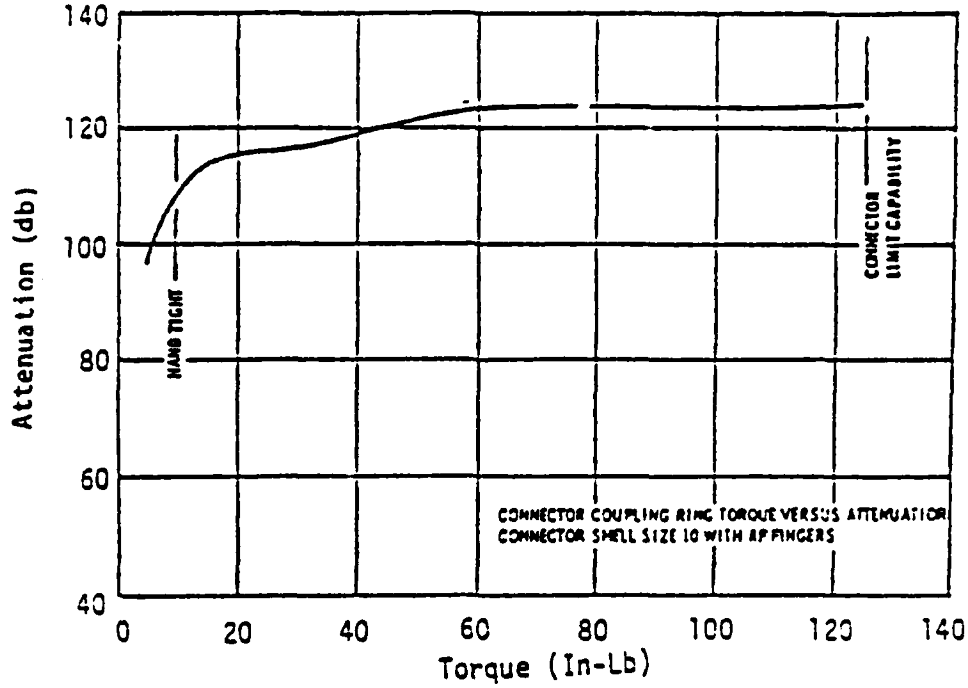


Figure 4.49 Static Test [4.16]

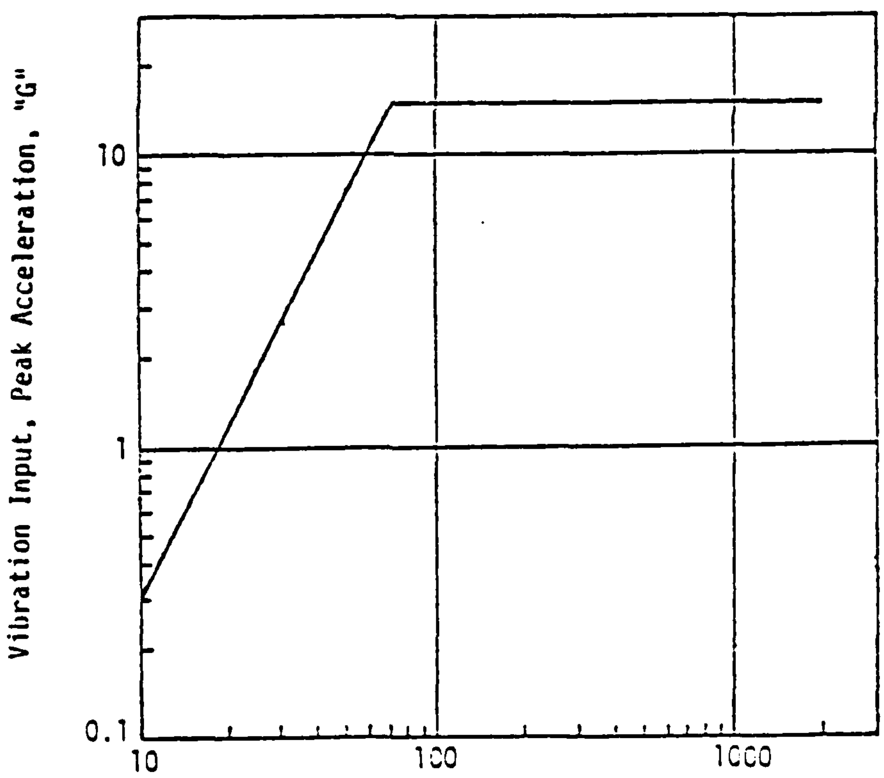


Figure 4.50 Test Vibration Input [4.16]

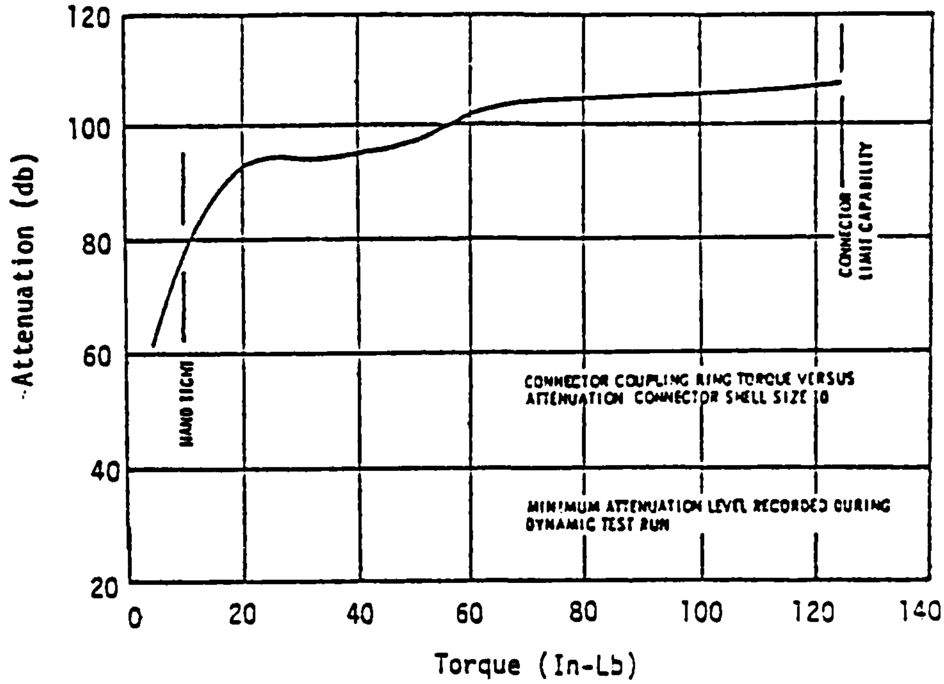


Figure 4.51 Dynamic Test (X Axis) [4.16]

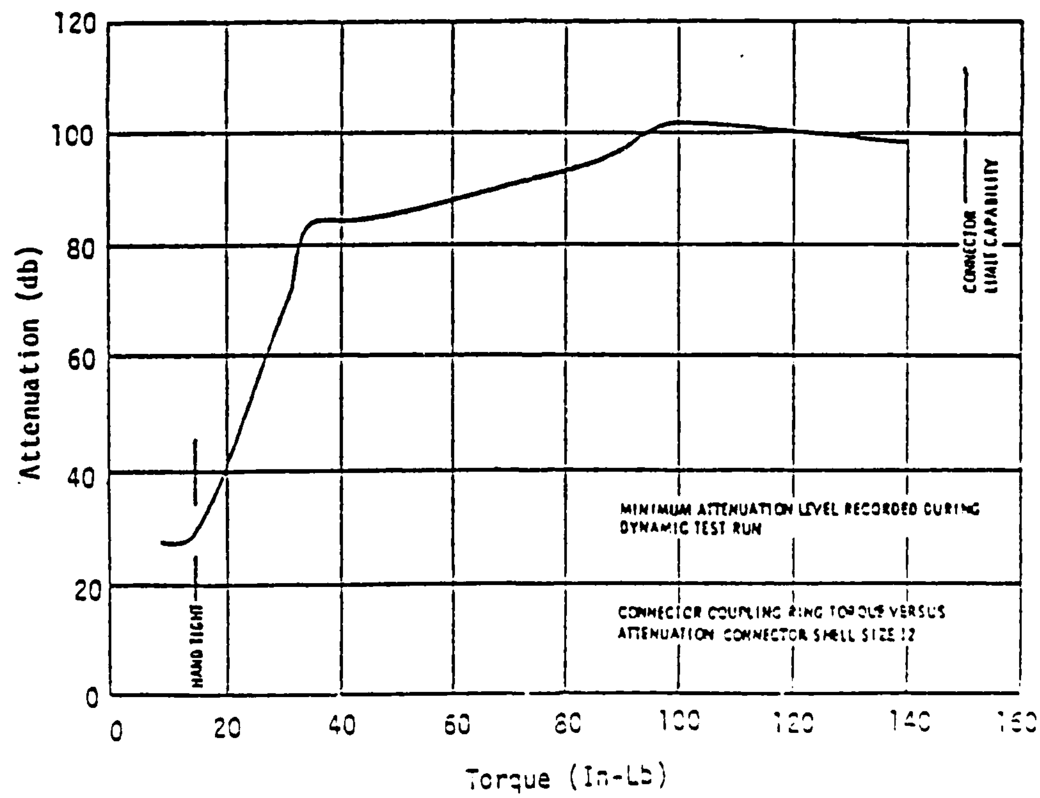


Figure 4.52 Dynamic Test (X Axis) [4.16]

$$Z_T \leq Z_c \ / \ 30 \qquad (4.40)$$

where ($I_s = 60\ I_p$, where I_s is the shield current and I_p is the pin current). Thus the transfer impedance for a 50 Ω cable must be less than 1.7 Ω. This condition can easily be met by most connectors with the possible exception of anodized connectors (see Table 4.8). Thus the use of connectors presents less leakage than a meter of braided cable, unless poor installation practices (such as using pigtails or connecting the cable shield inside the connector shell) are used.

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CHAPTER 5

INTERFACE SUSCEPTIBILITY ANALYSIS

5.0 Executive Summary

The material in Chapter 5 discusses computer and simple hand analysis techniques for determining circuit damage thresholds at the equipment interface pins. The methods are used for determining whether or not the transients specified in Section 2.4 will cause component damage and consequent equipment failure.

5.1 Background

Most circuits are designed for steady state operation. In order to protect equipment from EMP induced transients, the designer must address the problems associated with the introduction of these pulses on the equipment interface pins. Specifically, the circuits must endure the interface pin transients specified in Section 2.4.3.

Much of this chapter addresses the procedure for determining component damage thresholds from the manufacturer's specifications on an individual component [5.1-5.15]. Once the transient damage threshold of the components is established it can be determined whether circuit hardening is required by performing an interface susceptibility analysis [5.15-5.18].

The interface susceptibility analysis determines for a specified threat the minimum levels of voltage and current on an interface pin that are sufficient to permanently damage one or more components. The analysis can be performed with only a calculator or more complex computer circuit codes [5.19-5.21], with corresponding accuracy.

The circuit will be required to be hardened if the equipment fails when stressed by the transient pulse. Individual components fail when the transient pulse causes permanent damage of the component. There are two basic mechanisms causing components to fail. The first damage mechanism is dielectric breakdown. Dielectric breakdown can occur when voltage levels are exceeded for a given thickness of dielectric material. Dielectric breakdown accounts for arcing between coils on inductors and transformers, puncture of dielectrics between the plates of a capacitor, and puncture of the oxides in MOS devices. The second damage mechanism is thermal heating of the component. Thermal heating of the component can cause leads to melt on delicate components, junctions in semiconductors to diffuse, and changes in the microstructure of metal oxide varistors.

Manufacturers generally specify the DC voltage ratings of components containing dielectrics that may break down. Transient voltage ratings are typically greater than the DC voltage rating on dielectrics for short duration pulses. This is because dielectric breakdown is dependent on voltage rate of rise (cf. Section 6.3.2 on dielectric breakdown devices). In addition, dielectric voltage ratings depend upon the thickness of the dielectric material. For example, MOS devices can break down for overvoltages across the thin oxide junctions. Consequently, some MOS manufacturers build in a voltage limiting device to protect this junction. Inductors and transformers have thin dielectric coatings on the wires. When fast rate of rise voltage transients occur across

Clarify! leads reader to think it is hardening

an inductor (or transformer) an overvoltage can occur between the dielectric coating. However, DC voltage ratings are generally specified by the manufacturer and often can be used as worst-case estimates of dielectric breakdown levels. Consequently, dielectric breakdown as a failure mechanism is not dwelt upon heavily in this chapter.

Thermal heating of components is the primary concern in this chapter. This is because transient damage thresholds caused by heating are not specified by the component manufacturers.

The components most susceptible to thermal damage are semiconductors (Figure 5.1). The method for predicting failure thresholds of discrete semiconductor devices was developed by Wunsch [5.14] and Tasca [5.13]. They found that the power required for thermal damage of the simple semiconductor junction obeyed the relation

$$P = Kt_p^{-1/2} \tag{5.1}$$

check numbers

for rectangular pulses of durations t_p between 100 nanoseconds and 10 nanoseconds (which is the time regime of interest for EMP). The constant of proportionality in (5.1) became known as the Wunsch damage constant and is a characteristic of a specific device.

Later, it was shown [5.22] that the simple thermal model of Wunsch and Tasca was lacking for certain classes of devices. In fact, discrepancies over two orders of magnitude between the damage constants obtained from experimental and analytical models were possible. This resulted in the investigation [5.23] of new models to adequately (within a factor of 10) predict the damage constants of semiconductor devices that did not strictly adhere to the simple thermal model of Wunsch and Tasca. This resulted in damage models for not only diodes, but also transistors and integrated circuits.

The accuracy of using the models and data is limited. Experimentally determined Wunsch damage constants should be derated. Changes in component technology over the years have resulted in smaller devices which perform the same function as components having the same device number using older technologies. There are also differences in manufacturing design for the same component. Consequently Wunsch damage constants determined experimentally for a unique part can vary from manufacturer-to-manufacturer and year-to-year. For this reason, Wunsch damage constants measured for a particular part should be derated by a factor of five when applied to other devices with the same part number.

Also, analytically determined Wunsch damage constants should be derated by a factor of 50 or greater. Derating should be done largely because of uncertainties in extending the analytic models to devices that have never been tested. In addition, there is a large spread in the measured data when devices are grouped according to device family. Device family pertains to the grouping of devices according to technology (i.e. TTL, DTL, MOS, etc.). Figures 5.2 and 5.3 illustrate the variation in measured failure levels, and shows the need for derating devices when grouped in this way.

Section 5.2 briefly describes the dominant component failure modes, and then provides detailed models for the most vulnerable component types. Methods are shown for determining damage constants from experimental data, manufacturers' specification sheets and by estimating.

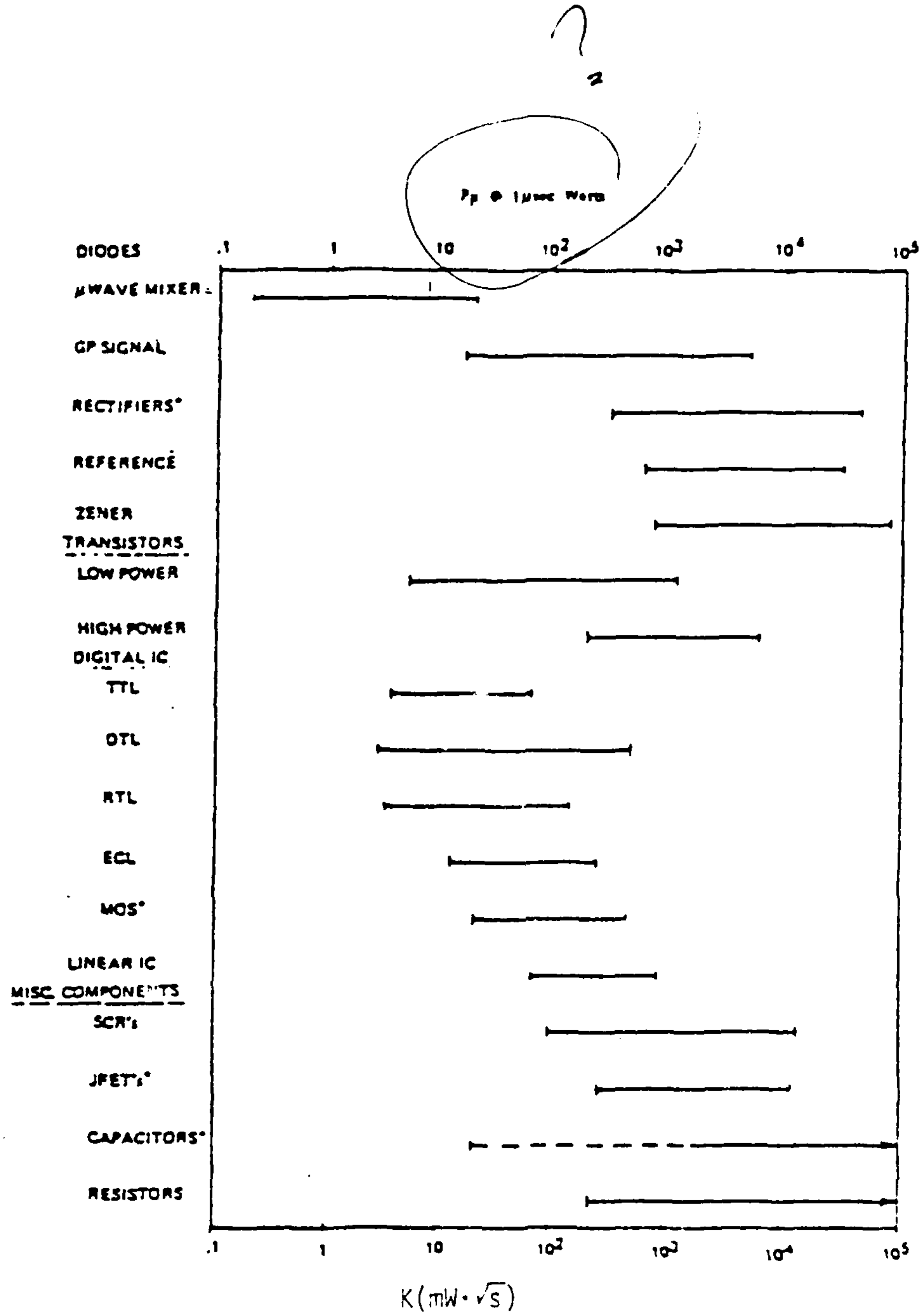


Figure 5.1 Relative Damage Susceptibility of Electronic Components [5.18]

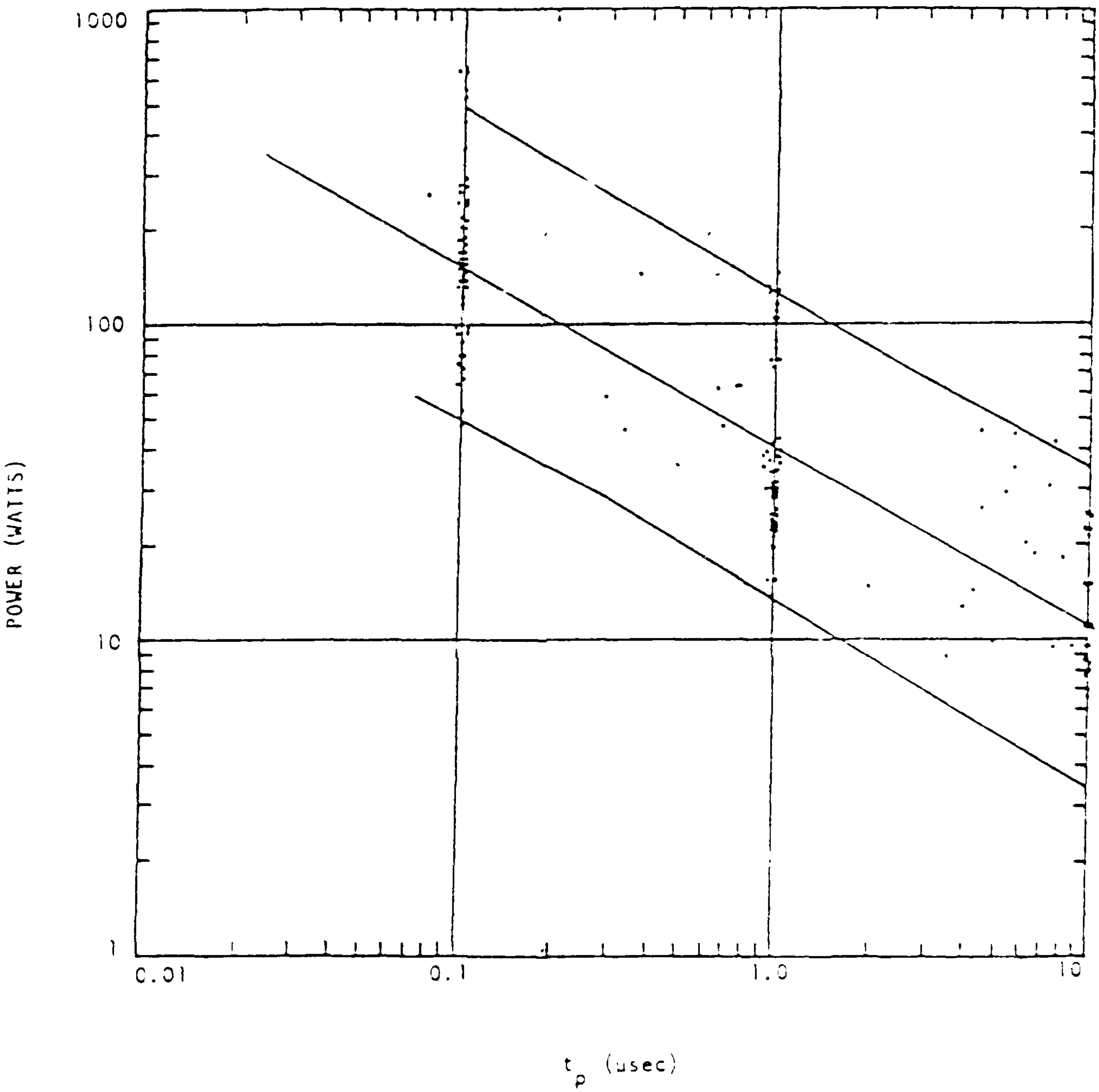
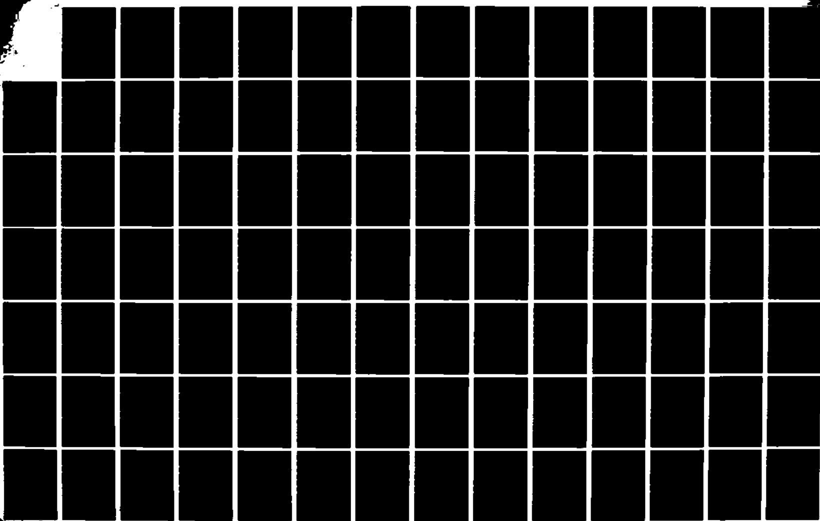
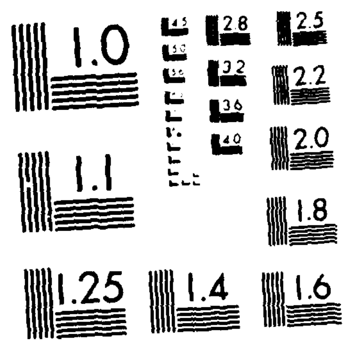


Figure 5 - DTL-INPUT Category [5.2]

HARDENING OF NAVAL EQUIPMENT(U) ELECTRO MAGNETIC
APPLICATIONS INC DENVER CO S R ROGERS ET AL. 15 JUL 81
SSIFIED N60921-80-C-0190 F/G 15/5 NL





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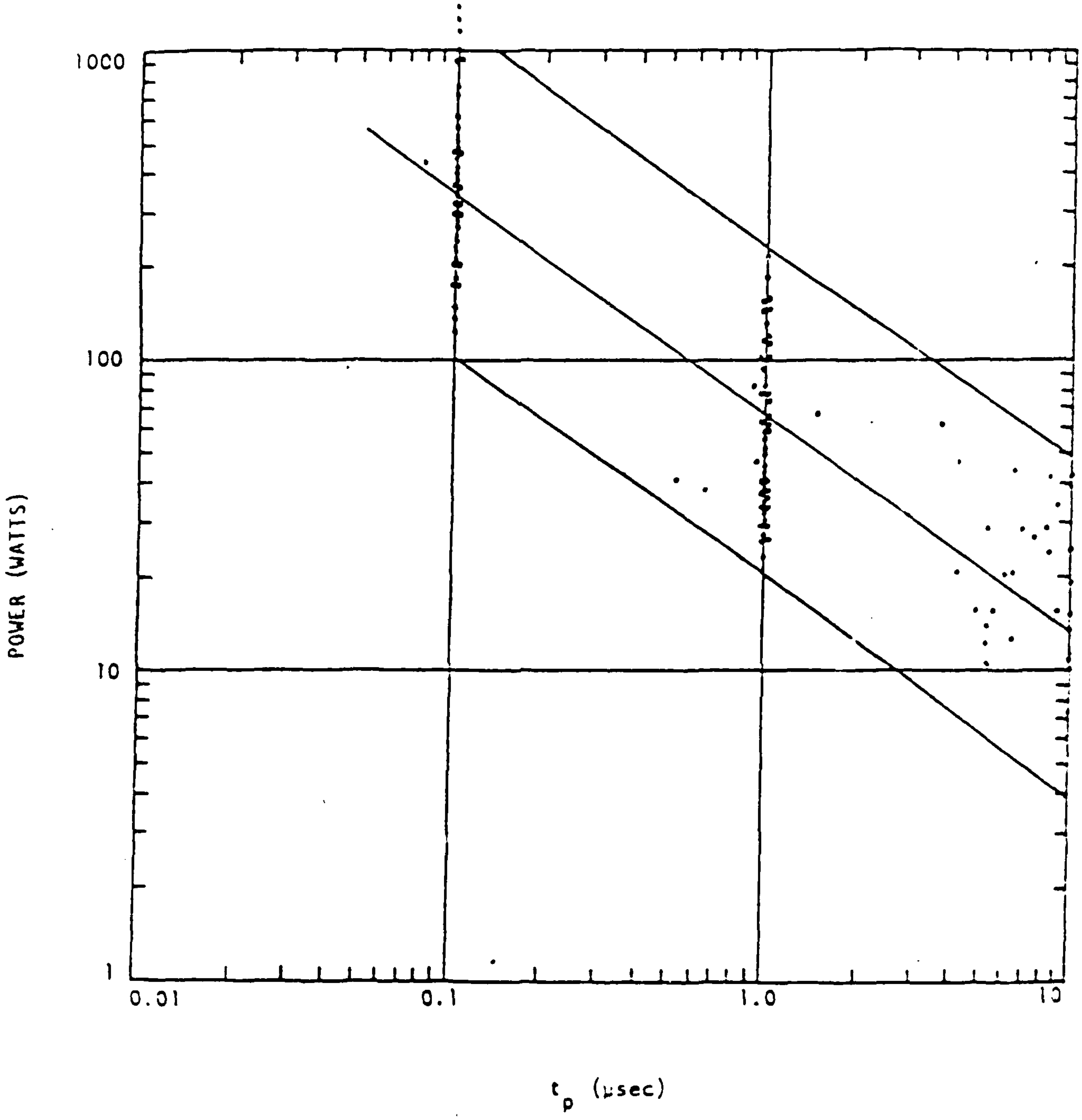


Figure 5.3 DTL-OUTPUT Category [5.23]

Once the component damage thresholds are established, the circuit can be analyzed using simple or computer analysis techniques to see if any components are damaged when subjected to the transients specified in Section 2.4.3. Simple techniques requiring only a calculator (hand analysis) as well as computer analysis techniques are discussed in Section 5.3.

In addition Section 5.3 describes methods of organization and documentation. The method of determining hardness margins is also presented.

This chapter concludes with an example section which demonstrates circuit analysis methods. Several examples are cited in Section 5.4 that demonstrate the analsis techniques in Section 5.3.

Should the circuit be shown to be soft (susceptible to damage), the techniques in Chapters 6 and 8 should be considered to provide interface hardening.

5.1.1. Outline for Performing the Interface Susceptibility Analysis

The first step in either preliminary or detail analysis is the determination of failure criteria. Electronic components will be discussed in five general categories: semiconductors, resistors, capacitors, inductive devices and miscellaneous components such as switches and lamps. The hierarchy of data sources is discussed. A discussion of failure models used is included. The failure models are readily calculated on a handheld calculator.

5.1.2 Derating of Damage Power Levels

The procedures and models described in this document calculate failure power (P_F) as the nominal or average value, with the exception of integrated circuits.

For semiconductors derate: 1/50 for analytical data; 1/5 for SUPERSAP2* experimental data and assumed standard models for transistors and diodes; and 1/100 for assumed standard models for integrated circuits and amplifier modules.

5.1.3 Choosing Component Failure Models

The data sources for potentially susceptible components may be prioritized as follows:

PRIORITY I	- SUPERSAP2* experimental data
PRIORITY II	- Analytical models defined in Section 5.2
PRIORITY III	- Assumed Standard Models.

The highest priority data source available should be used.

5.1.4 Conversion of Damped Sine Pulse to Rectangular Pulse

The transient pulse used for testing equipment specified in Section 2.4.3 is a damped sinusoid pulse. In order to use the Wunsch damage models, it is necessary to convert the damped sinusoid pulse to an equivalent rectangular

*SUPERSAP2 is a publicly available failure model data base. Its use is described in detail in Section 5.2.5.

pulse. Conversion to rectangular pulses has the following built in assumption [5.16]:

1. Significant heating of the semiconductor device occurs only when the device is in reverse breakdown, and

2. Device parameters, such as breakdown voltage, do not change significantly during the damped sine excitation.

The relation between the damped sine pulse with a decay factor Q and the square pulse of duration t_p is given by [5.16]

$$t_p = \frac{1}{Bf} \tag{5.2}$$

where f is the frequency of the sine pulse and B is a constant which is a function of Q. The relationship between B and Q is shown in Figure 5.4. Note that for a Q of 16 ± 4 the upper limit is chosen for conversion which results in a B of 1.8. That is, in this handbook, the coversion of the damped sine pulse of Section 2.4.3 to a rectangular pulse is

$$t_p = \frac{1}{1.8f} \tag{5.3}$$

where t_p is the rectangular pulse duration and f is the frequency of the sine pulse.

5.2 Device Damage Mechanisms

This section describes circuit component failure modes and how to model them for the most vulnerable component types: semiconductors, resistors, capacitors, inductive devices, and miscellaneous components. For each of these component types, methods of obtaining failure data from SUPERSAP2, manufacturers' specification sheets, and estimates are described. Further information on device damage mechanisms and modeling are available in References 5.1 through 5.15.

5.2.1 Semiconductor Failure

Semiconductor devices include diodes, transistors, integrated circuits, silicon controlled rectifiers, and thyristors. These devices consist of one or more interconnected p-n junctions with various junction areas and doping levels. Overall device failure is caused by permanent damage to one of the p-n junctions.

The main source of permanent damage in p-n junctions is a heating effect called thermal second breakdown [5.13]. Whenever voltages or currents are impressed upon semiconductors, the bulk resistance of the p-n junction results in power dissipation in the form of heat. Thermal second breakdown is a local thermal runaway effect at the junction, resulting in microplasmas and hot spots (melting of the junction). This failure mode is a function of junction parameters such as geometry, thickness, doping, resistivity, and other parameters such as biasing and device geometry

The p-n junction parameters can be used to analytically determine the Wunsch damage constants when measured damage constants are unknown. The junction parameters can be calculated from the device operating characteristics given by the manufacturer or D.A.T.A. books which summarize manufacturers device characteristics. Typical characteri cs for semiconductor devices are shown in Figure 5.5 which depicts a low-cost silicon rectifier. These same types of

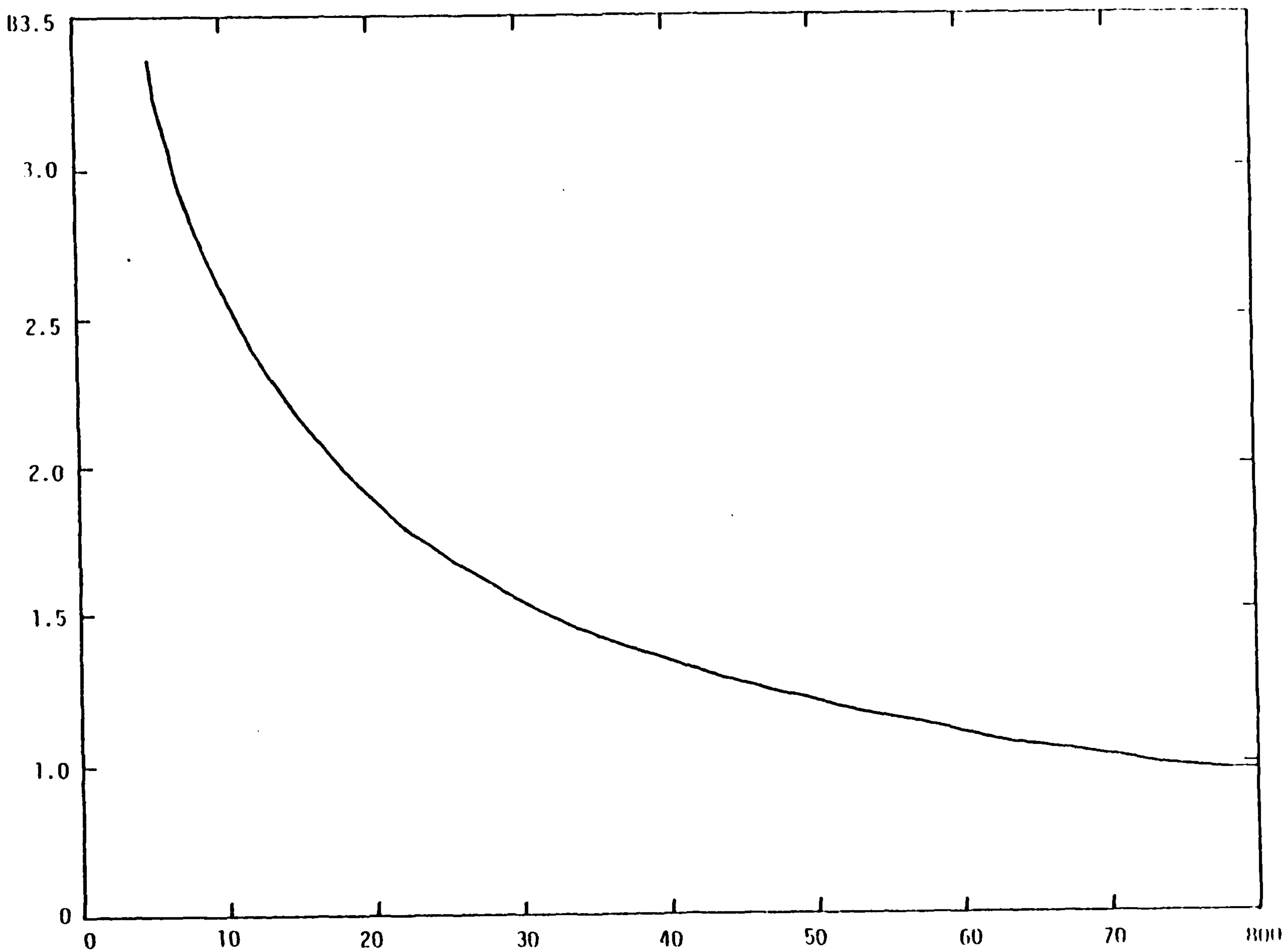
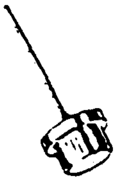


Figure 5.4 Rectangular Pulse Conversion Factor B Versus Sine Wave Decay Factor Q

1N3659 thru 1N3663 (SILICON)



CASE 43
(DO-21)

Low-cost silicon rectifiers in hermetically sealed, press-fit case, designed for operation under severe environmental conditions. Cathode connected to case, but available with reverse polarity by adding suffix "R" to type number.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	1N3659 1N3659R	1N3660 1N3660R	1N3661 1N3661R	1N3662 1N3662R	1N3663 1N3663R	Units
Peak Repetitive Reverse Voltage DC Blocking Voltage	$V_{RM(rep)}$ V_R	50	100	200	300	400	Volts
RMS Reverse Voltage	V_r	35	70	140	210	280	Volts
Average Half-Wave Rectified Forward Current with Resistive Load @ 100°C case @ 150°C case	I_O			30 25			Amp Amp
Peak One Cycle Surge Current (150°C case temp, 60 Hz)	$I_{FM(surge)}$			400			Amp
Operating Junction Temperature	T_J			−65 to +175			°C
Storage Temperature	T_{stg}			−65 to +200			°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	1N3659 1N3659R	1N3660 1N3660R	1N3661 1N3661R	1N3662 1N3662R	1N3663 1N3663R	Unit
Maximum Forward Voltage at 25 Amp DC Forward Current	V_F	1.2	1.2	1.2	1.2	1.2	Volts
Maximum Full Cycle Average Forward Voltage Drop @ Rated PIV and Current	$V_{F(AV)}$	0.7	0.7	0.7	0.7	0.7	Volts
Maximum Full Cycle Average Reverse Current @ Rated PIV and Current (as half-wave rectifier, resistive load, 150°C)	$I_{R(AV)}$	5.0	4.5	4.0	3.5	3.0	mA
Thermal Resistance	θ_{JC}			1.0			°C/W

Figure 5.5 Typical Characteristics Provided by Semiconductor Manufacturers [5.24]

device characteristics are shown in D.A.T.A. books in a different format. Many of the manufacturers specifications are presented in a format that is not readily adaptable to use. That is, there are discrepancies as to what each manufacturer defines as maximum current, breakdown voltage, etc.

When using the analytical models, it is important to use the correct device characteristics in the equations. Tables 5.1 and 5.2 contain the information for interpreting information contained in the D.A.T.A. books to be consistent with the symbols contained in the following subsections. Shown in Tables 5.1 and 5.2 are the sections of the D.A.T.A. book that particular devices can be found and the method for converting the information contained in that section for use in the analytical models. These device characteristics in order of presentation are breakdown voltage, maximum current, junction capacitance, junction to ambient thermal resistance, and junction to case thermal resistance.

Semiconductor failure is related to the power dissipated in the junctions, and this failure power has been determined experimentally to be given by:

$$P_f = A\, t_p^{-B}, \tag{5.4}$$

with A and B device damage constants and t_p the duration of a rectangular pulse between 100 ns and 10 μs in width. For EMP threats, the failure power of most semiconductor devices is given by (5.1), i.e.

$$P_f = K t_p^{-1/2},$$

where K is the Wunsch damage constant. Figure 5.1 shows the range of K for different component types.

The models for determining semiconductor component failure current, voltage, and power are now presented.

5.2.1.1 Diodes

Diode failure is well represented by the Wunsch model for the simple p-n junction undergoing second thermal breakdown, i.e. equation 5.1.

The equivalent circuit failure model for a diode is shown in Figure 5.6. A surge resistance R_s, is defined as:

$$R_S = R_{BLK} - R_{SC}. \tag{5.5}$$

If the surge resistance, damage constant, and breakdown voltage are known, then the failure current and voltage are given by:

$$I_F = \frac{-V_{BD} + \sqrt{V_{BD}^2 + 4R_S P_F}}{2R_S} \tag{5.6}$$

Table 5.1 D.A.T.A. Diode Conversion [5.18]

D.A.T.A. Sec.	FOR: V_{BD}	FOR: I_{MAX}	FOR: JUNCAP		FOR: θ_{JA} (EQ. 1)*		FOR: θ_{JC} (EQ. 2)*	
			FOR: C_{RD}	FOR V_{RD}	Power A (P_A)	T_J	Power C (P_C)	T_J
2 Silicon Reference Diodes	Nom. Ref. Volt (Use ones with no symbols)				Max. Diss. @ 25^0 C (Use when no symbols)	Max. Temp. (Use J only)	Max. Diss. @ 25^0 C, (Use ☑ only)	Max. Temp. (Use J only)
3 Diodes	PIV	Ave. Rec. Fwd. Cur.	Cap.	At Test Volts	Diss. (Abs. Max.) (Use when no symbols)	Same as above		
4 Diodes/ Rectifiers	PIV	Ave. Fwd. I	Cap. at 0 Volts	(Use 1.0 Volts)				
5 Rectifiers	PIV	Max. Ave. Fwd. DC I_o			Diss. Max. Rating at 25^0 C (Use when no symbols)	Max. Temp. (Use J only)	Diss. Max. Rating at 25^0 C (Use when no symbols)	Max. Temp. (Use J only)
8 Microwave Mixer Diodes	None				Abs. Max. Rating Burnout (Use § Only)	Max. Temp.		

Table 5.1 (cont'd) D.A.T.A. Diode Conversion [5.18]

D.A.T.A. Sec.	FOR: V_{BD}	FOR: I_{MAX}	FOR: JUNCAP		FOR: θ_{JA} (EQ. 1)*		FOR: θ_{JC} (EQ. 2)*	
			FOR: C_{RD}	FOR V_{RD}	Power A (P_A)	T_J	Power C (P_C)	T_J
10 Voltage Variable Capacitor & Varactor Diodes	PIV		Cap. C_J	At Test Volts				
11 Tunnel Diodes	None	Abs. Max. Fwd. Cur.	Max. Total Cap. (Use Ø only)	Use 1.0 Volt	Abs. Max. Diss. (Use when no symbols	Max. Temp. (Use J Only)	Abs. Max. Diss. (Use when no symbols)	Max. Temp. (Use J Only)

* Equation 1: $\theta_{JA} = (T_J-25)/P_A$ Equation 2: $\theta_{JC} = (T_J-25)/P_C$

Table 5.2 D.A.T.A. Transistor Parameter Conversions [5.18]

D.A.T.A. Sec.	FOR: V_{BD}	FOR: I_{MAX}	FOR: INJUNCAP/OUTJUNCAP		FOR: θ_{JA} (EQ. 1)		FOR: θ_{JC} (EQ. 2)	
			C_{RE} or C_{RC}	V_{RE} or V_{RC}	P_A	T_J	P_C	T_J
2 GER. PNP Low Power	(EB) Abs. Max. BV_{ebo}	I_C	(C_{OCB}) C_{ob}	(V_{BCBO}) BV_{ebo}	Max. Coll. Diss. @ 25^0 C (Use all)	Max. Temp. (Use J only)	Max. Coll. Diss. @ 25^0 C (Use ø only)	Max. Temp. (Use J only)
	(CB) BV_{cbo}	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above
3 GER. NPN Low Power	(EB) Abs. Max. BV_{ebo}	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above
	(CB) Abs. Max. BV_{cbo}	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above
4 Silicon PNP Low Power	(EB) Abs. Max. BV_{ebo}	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above
	(CB) Abs. Max. BV_{ebo}	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above

Table 5.2 (cont'd) D.A.T.A. Transistor Parameter Conversions [5.18]

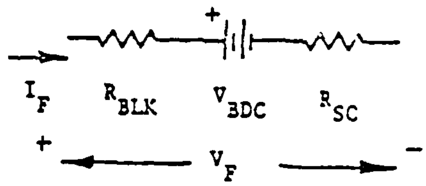
D.A.T.A. Sec.	FOR: V_{BD}	FOR: I_{MAX}	FOR: INJUNCAP/OUTJUNCAP		FOR: θ_{JA} (EQ. 1)		FOR: θ_{JC} (EQ. 2)	
			C_{RE} or C_{RC}	V_{RE} or V_{RC}	P_A	T_J	P_C	T_J
5 Silicon NPN Low Power	(EB) Abs. Max. BV_{ebo}	I_C	(C_{OCB}) C_{ob}	(V_{BCBO}) BV_{cbo}	Max. Coll. Diss. @ 25^o C (Use all)	Max. Temp. (Use J only)	Max. Coll. Diss. @ 25^o C (Use ϕ only)	Max. Temp. (Use J only)
	(CB) Abs. Max. BV_{cbo}	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above	Same as above
6 Silicon FET P-Chan.	(EB) BV_{gss}	I_d	(C_{RE}) Max. C_{is}	(V_{RE}) .5 V	Max. Device Diss. @ 25^o C	Same as above.	Max. Diss. @ 25^o C (Use Λ only)	Same as above
	(CB) BV_{dss}	Same as above	(C_{RC}) Same as above	(V_{RC}) Same as above	Same as above	Same as above	Same as above	Same as above
7 Silicon FET N-Chan.	(EB) Same as 6							
	(CB) Same as 6							
8 GER. PNP High Power	(EB) BV_{ebo}	I_C Abs. Max. @ 25^o C			Max. Diss. @ 25^o C (Use all)	Same as above	Max. Diss. @ 25^o C (Use ϕ only)	Same as above
	(CB) BV_{cbo}	Same as above			Same as above	Same as above	Same as above	Same as above

Table 5.2 (cont'd) D.A.T.A. Transistor Parameter Conversions [5.18]

D.A.T.A. Sec.	FOR: V_{BD}	FOR: I_{MAX}	FOR: INJUNCAP/OUTJUNCAP		FOR: θ_{JA} (EQ. 1)		FOR: θ_{JC} (EQ. 2)	
			C_{RE} or C_{RC}	V_{RE} or V_{RC}	P_A	T_J	P_C	T_J
9 GER. NPN High Power	(EB) BV_{ebo}	I_C Abs. Max. @ 25^0 C			Max. Diss. @ 25^0 C (Use all)	Max. Temp. (Use J only)	Max. Diss. @ 25^0 C (Use ϕ only)	Max. Temp. (Use J only)
	(CB) BV_{cbo}	Same as above			Same as above	Same as above	Same as above	Same as above
10 Silicon PNP High Power	(EB) BV_{ebo}	I_C Max. @ 25^0 C			Same as above	Same as above	Same as above	Same as above
	(CB) BV_{cbo}	Same as above			Same as above	Same as above	Same as above	Same as above
11 Silicon NPN High Power	(EB) BV_{ebo}	Same as above			Same as above	Same as above	Same as above	Same as above
	(CB) BV_{cbo}	Same as above			Same as above	Same as above	Same as above	Same as above
12 Switching	(EB)		C_{ob} (Use § only)	.5 V	Same as above	Same as above	Same as above	Same as above
	(CB)		C_{ob}	1. V	Same as above	Same as above	Same as above	Same as above

COMPONENT TYPE: DIODE	MODEL TYPE: DAMAGE

TOPOLOGY:



$P_F = Kt_p^{-1/2}$

PARAMETERIZATION:

START

$N_D = 4.49 \times 10^{18} (V_{BEBO})^{-1.5}$ — DOPING CONCENTRATION

$V_{BDC} = 4.07 \times 10^{12} (N_D)^{-0.67}$ — BREAKDOWN VOLTAGE AT FAILURE

$\rho_{SC} = 2.48 \times 10^{25} (N_D)^{-1.80}$ — SPACE CHARGE RESISTIVITY

$\rho_{BLK} = 3.61 \times 10^{10} (N_D)^{-0.81}$ — BULK RESISTIVITY

$J_F = 8.26 \times 10^{-11} (N_D)^{0.88}$ — FAILURE CURRENT PER UNIT AREA

A — TO AREA CALCULATION

B

DAMAGE PARAMETER CALCULATIONS

$$R_{BLK} = \rho_{BLK}/\text{AREA}$$

$$R_{SC} = \rho_{SC}/\text{AREA}$$

$$I_{F_{100ns}} = J_F \cdot \text{AREA}$$

$$V_{F_{100ns}} = V_{BDC} + I_{F_{100ns}} (R_{BLK} + R_{SC})$$

$$I_{FP} = I_{F_{100ns}} \left(\frac{t_p}{100 \times 10^{-9}}\right)^{-1/2}$$

$$V_{FP}(t_p) = V_{BDC} + I_{FP} (R_{BLK} + R_{SC})$$

$$K = \left(I_{F_{100ns}} \cdot V_{F_{100ns}}\right) \left(100 \times 10^{-9}\right)^{1/2}$$

Figure 5.6 Diode Damage Computation [15]

DIODE

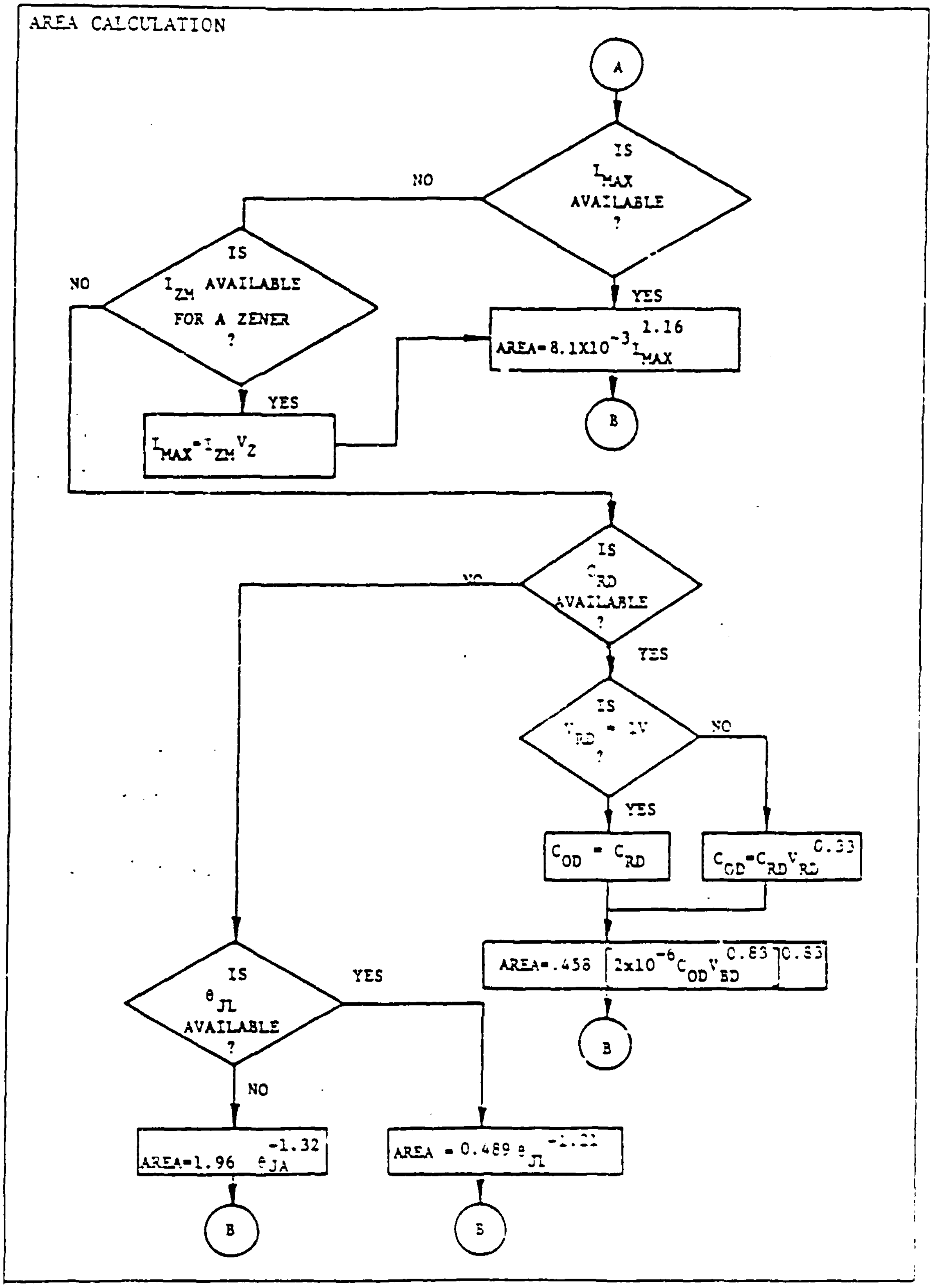


Figure 5.6 (cont'd) Diode Damage Computation [5.15]

DIODE

Definitions and units:

R_{BLK} = Resistance of bulk semiconductor in ohms

V_{BDC} = Breakdown voltage at the critical failure temperature, in volts

R_{SC} = Resistance associated with the space charge in an avalanching junction, in ohms

I_F = Current required for failure, in amperes

V_F = Voltage required for failure in volts

N_D = Doping concentration of the lightly doped side of the junction, in atoms/cm^3

V_{BD} = Rated breakdown voltage of the diode in volts

ρ_{SC} = Space charge resistivity in $\Omega \cdot cm^2$

ρ_{BLK} = Bulk resistivity in $\Omega \cdot cm^2$

J_F = Failure current density in A/cm^2

AREA = Effective area of a junction in square centimeters

I_{F100NS} = Failure current for a 100 nanosecond rectangular pulse, in amperes. Note: I_{FP} is the failure current for other pulse widths.

V_{F100NS} = Failure voltage for a loo nanosecond rectangular pulse, in volts. Note: V_{FP} is the failure voltage for other pulse widths.

K = Wunsch damage constant in $W \cdot s^{1/2}$

t_p = Rectangular pulse width, in seconds

I_{MAX} = Rated maximum forward current in amperes

I_{ZM} = Rated maximum zener current in amperes

C_{RD} = Reverse biased capacitance in picofarads

V_{RD} = Voltage at which C_{RD} is measured in volts

C_{OD} = Capacitance at 1 volt reverse bias in picofarads

V = Zener Voltage

Figure 5.6 (cont'd) Diode Damage Computation [5.15]

DIODE

Definitions and units:

Θ_{JL} = Junction to lead thermal resistance in °C/W (specified for 1/8 inch lead length)

Θ_{JA} = Junction to ambient thermal resistance in °C/W

Figure 5.6 Diode Damage Computation (Concluded) [5.15]

and

$$V_F = V_{BD} + I_F R_S \qquad (5.7)$$

If any one or all of these characteristics are unknown, then Figure 5.6 shows the method of estimating them from data obtained from the manufacturers' specification sheets.

When an experimental damage constant is unavailable, it is necessary to determine two parameters of the diode's fabrication in order to make an estimate [5.15]. First it is necessary to know the doping concentration of the lightly doped side of the junction, because this controls the current density required for second breakdown. It also controls the values of both bulk resistance and space charge resistance (the two components of surge resistance) as well as the critical breakdown voltage. Second, it is necessary to know the effective junction area, because a larger junction can clearly handle more power than a smaller one.

Figure 5.6 shows the parameterization procedures. The doping concentration, N_D, is determined from the rated (or measured) breakdown voltage, (for example, DC blocking voltage in Figure 5.5). This value is then used to predict the critical breakdown voltage (that is, the breakdown voltage at the critical failure temperature). Next, the value of N_D is used to predict the space charge resistivity. This is the resistivity associated with an avalanching junction and contributes to junction failure through I^2R heating. The bulk resistivity is then predicted from N_D. This is the resistivity associated with the bulk semiconductor material and does not contribute to junction failure. It has been found necessary to include both space charge and bulk resistivity in order to accurately predict the response of all diodes. Finally, the failure current density is predicted from N_D.

The resistances and failure current will be scaled by device area. There are a number of possible ways to estimate device area, depending on which parameters are available. These are shown in Figure 5.6 in order of priority, with the best estimators first. The maximum current rating of the diode is highly correlated with effective junction area. The reverse biased capacitance is also well correlated, as expected. If neither of these is known, the junction to lead and junction to ambient thermal resistances may be used to provide an area estimate.

When the failure current density is multiplied by area, the diode failure current for a 100 nanosecond rectangular pulse is obtained. Failure current and voltage of other pulse widths (I_{FP} and V_{FP}) can be calculated directly using the equation in Figure 5.6. A damage constant may also be calculated if the analyst so desires.

An example using the procedure outlined in Figure 5.6 for obtaining the failure current, voltage, and power is illustrated. From Figure 5.5, the DC blocking voltage of the 1N3659 diode is 50 volts. The maximum (DC) forward current is 25 amperes. These two parameters are all that is required to determine the failure characteristics. This results in a damage constant of [illegible] and

and a failure current of 6.9 kA and failure voltage of 109 V for the 10 MHz damped sine pulse. Recall that the damage constant should be derated by 50 to give $K = 3.5\ W \cdot \sqrt{s}$. This results in a failure power of 14.8 kW. A quick check of the damage can be found using the range of damage constants from Figure 5.5. For rectifiers the range of damage constants are 0.3 to $50\ W \cdot \sqrt{s}$. (Note that the derated damage constant in the above example is in this range).

Some experimental values for the Wunsch damage constants for particular diodes are shown in Table 5.3. Both the simple Wunsch damage constant of (5.1) and the more general Wunsch damage constants of (5.4) are presented.

5.2.1.2 Transistors

Because transistors are basically back-to-back diodes, the collector-base and emitter base junction models for a transistor are similar to the diode. One major difference between diodes and transistors is that transistors have an effective junction area whereas the diode junction area is the physical junction area used in estimating the device failure thresholds.

For transistors, there is more than one junction. The emitter-base junction and the collector-base junction are analyzed separately. With these few minor differences, the transistor is analyzed in the same manner as the diode.

The failure power, surge impedance, failure current and voltage for each junction are given by equations 5.1, 5.5, 5.6 and 5.7, respectively. Figures 5.7 and 5.8 contain the parameter estimation techniques for the emitter-base junction and collector-base junction, respectively.

Some experimental Wunsch damage constants for transistors are shown in Tables 5.4 and 5.5 for transistors. The Wunsch damage constants for both (5.1) and (5.4) are shown for the emitter-base (Table 5.4) and collector-base (Table 5.5).

5.2.1.3 Integrated Circuits

Integrated circuits and microprocessors can contain thousands of diodes and transistors and can be modeled as a black box. The black box model takes into account the fact that there are many current paths through an IC with one primary current path which causes IC failure. The integrated circuit follows the general Wunsch model [5.25] in (5.4), i.e.

$$P_f = A\ t_p^{-B}$$

where A and B are constants that depend on the device technology (e.g. DTL [diode-transistor logic], TTL [transistor-transistor logic], etc.) and the port type (e.g. input, output, or power). Figure 5.9 shows the black box model. The required damage parameters required for each IC port are given in Table 5.6. Also shown in Table 5.6 are the upper and lower 95% limits for the constant A. These limits are also shown in Figures 5.2 and 5.3 for an IC using DTL. As integrated circuit and microprocessor technology progresses, it is possible that the new devices may deviate even more from the 95% bounds in Table 5.6. It should be noted in Table 5.6 that the exponent of (5.4) for the input of MOS devices is nearly 1/2. This is because MOS inputs are voltage sensitive and are generally protected by voltage limiting diodes. Consequently, MOS inputs, usually have the burnout characteristics of diodes.

Table 5.3 Diode Damage Parameters [5.8]

DEVICE	WUNSCH K	GENERALIZED WUNSCH A	GENERALIZED WUNSCH B
FD777	7.170E-03	2.420E-05	3.360E-01
LVA351	1.300E-01	1.000E-01	5.000E-01
LVA51A	1.290E+01	1.290E+00	5.970E-01
LVA91A	1.000E-01	1.000E-01	5.000E-01
DT254	1.200E+00	2.100E-02	1.000E+00
1N1095	2.800E-01	5.600E-01	5.000E-01
1N1124A	5.750E+00	7.760E-05	1.220E+00
1N1126A	1.510E+01	1.510E-01	5.000E-01
1N1202A	1.120E-01	1.120E-01	5.000E-01
1N1202A	4.670E+00	1.210E-02	2.700E-01
1N1206	1.590E+01	1.590E-01	5.000E-01
1N1614	4.380E+00	2.500E-03	3.200E-02
1N1615	1.290E-01	1.290E-01	5.000E-01
1N1733A	1.130E-01	1.130E-01	5.000E-01
1N21B	1.600E-03	1.600E-03	5.000E-01
1N21C	2.700E-03	2.700E-03	5.000E-01
1N21E	2.300E-03	2.300E-03	5.000E-01
1N21F	2.000E-03	2.000E-03	5.000E-01
1N21WE	1.300E-03	1.300E-03	5.000E-01
1N215B	3.060E-01	3.060E-01	5.000E-01
1N23B	1.500E-03	1.500E-03	5.000E-01
1N23D	1.200E-03	1.200E-03	5.000E-01
1N23E	2.700E-03	2.700E-03	5.000E-01
1N23F	1.000E-03	1.000E-03	5.000E-01
1N23G	3.500E-04	3.500E-04	5.000E-01
1N23RF	9.400E-04	9.400E-04	5.000E-01
1N23WE	2.900E-04	2.300E-04	5.000E-01
1N25	5.600E-03	5.600E-03	5.000E-01
1N25	2.600E-02	2.600E-02	5.000E-01
1N25A	1.300E-02	1.300E-02	5.000E-01
1N25B	8.500E-01	8.500E-01	5.000E-01
1N270	3.382E-02	3.392E-02	5.000E-01
1N270A	2.300E-01	1.000E-02	1.000E+00
1N277	2.700E-02	2.700E-02	5.000E-01
1N2929A	7.300E-02	7.300E-02	5.000E-01
1N2970B	2.340E-01	2.340E-01	5.000E-01
1N2984B	1.590E-01	1.590E-01	5.000E-01
1N2985B	1.670E-01	1.670E-01	5.000E-01
1N2985B9	2.620E-01	2.620E-01	5.000E-01
1N2988B	2.770E-01	2.770E-01	5.000E-01
1N2989B	2.970E-01	2.970E-01	5.000E-01
1N2991B	3.810E-01	3.870E-01	5.000E-01
1N3015B	3.790E-01	5.310E-03	1.500E-01
1N3017B	1.060E-01	1.060E-01	5.000E-01
1N3019B	2.680E-01	2.680E-01	5.000E-01
1N3022B	1.380E-01	1.380E-01	5.000E-01
1N3031B	2.340E-01	2.340E-01	5.000E-01
1N3035B	3.940E-01	1.230E-03	2.500E-01
1N3037B	5.170E-01	5.170E-01	5.000E-01
1N3040B	7.050E-01	7.050E-01	5.000E-01
1N3047B	6.300E+00	6.300E+00	5.000E-01
1N3064	3.000E-01	3.000E-01	5.000E-01
1N3064	1.700E-01	5.000E-02	5.700E-01

Table 5.3 Diode Damage Parameters (continued) [5.8]

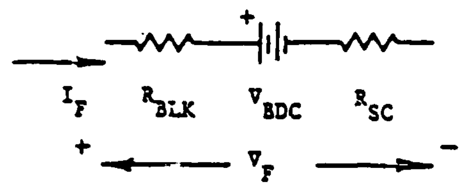
DEVICE	WUNSCH K	GENERALIZED WUNSCH A	GENERALIZED WUNSCH B
1N3157	2.793E-01	1.000E+00	7.600E-01
1N3189	7.430E+00	7.430E+00	5.000E-01
1N3191	4.122E+00	9.462E-02	9.725E-02
1N34A	1.400E-02	1.400E-02	5.000E-01
1N3595	7.040E-01	9.620E-04	9.510E-01
1N3600	1.370E-01	6.400E-03	7.190E-01
1N3600	1.200E-01	1.300E-01	5.000E-01
1N3600	1.900E-01	1.300E-03	8.400E-01
1N3821A	1.200E-01	1.200E+01	5.000E-01
1N3828A	1.960E-01	9.600E+00	5.000E-01
1N4003	2.200E+00	2.200E+00	5.000E-01
1N4005	3.467E-01	3.999E-02	6.594E-01
1N4006	5.310E-01	2.040E-03	6.820E-01
1N4122	9.000E+00	3.000E+00	5.000E-01
1N4127	1.486E-01	1.257E-02	1.007E+00
1N4148	1.130E-02	5.540E-04	7.120E-01
1N4152	5.960E-02	1.750E-01	4.390E-01
1N4154	6.090E-02	1.600E-03	7.470E-01
1N4156	4.100E-03	4.100E-03	5.000E-01
1N4244	1.000E-02	1.000E-02	3.350E-01
1N429	6.000E-01	6.000E-01	5.000E-01
1N4370	1.190E-01	1.190E+00	5.700E-01
1N43850A	2.960E-01	4.530E-01	4.720E-01
1N4450	1.360E-01	3.300E-02	5.880E-01
1N456	4.960E-01	2.410E-02	7.140E-01
1N457	1.200E-01	1.200E-01	5.000E-01
1N459	5.900E-01	5.900E-01	5.000E-01
1N459A	9.600E-01	3.300E-01	5.000E-01
1N4727	1.250E-01	2.400E-02	6.140E-01
1N482	4.410E-01	1.970E-02	7.130E-01
1N482A	9.600E-01	9.300E-01	5.000E-01
1N483B	1.020E+00	4.790E+00	4.000E-01
1N484A	4.500E-01	4.500E-01	5.000E-01
1N486	2.100E-01	1.910E-01	1.900E-01
1N4937	7.500E-01	7.500E-01	5.000E-01
1N5233	8.000E+00	3.000E+00	5.000E-01
1N5253A	-0.	2.160E-01	9.130E-01
1N5257	-0	3.860E+00	5.950E-01
1N5356	2.800E-01	2.800E-01	5.000E-01
1N537	5.100E-01	5.100E-01	5.000E-01
1N5378	3.300E-01	3.300E-01	5.000E-01
1N5388	8.530E+00	2.340E+02	7.500E-01
1N539	9.200E-01	9.200E-01	5.000E-01
1N540	9.300E-01	9.300E-01	5.000E-01
1N547	1.210E+01	1.210E+01	5.000E-01
1N5552	4.810E+00	1.220E+01	4.410E-01
1N5556	4.130E+01	4.130E+01	5.000E-01
1N5614	4.360E+00	6.100E-04	1.350E+00
1N5616	3.620E+00	1.250E-03	1.000E+00
1N64	4.100E-02	4.100E-02	5.000E-01
1N643A	1.000E-01	1.000E-01	5.000E-01

Table 5.3 Diode Damage Parameters (Concluded) [5.8]

DEVICE	WUNSCH	GENERALIZED WUNSCH	
	K	A	B
1N645	7.130E-01	3.200E+00	3.960E-01
1N645	5.600E-01	5.600E-01	5.000E-01
1N646	2.290E+00	2.290E+00	5.000E-01
1N647	4.200E+00	4.200E+00	5.000E-01
1N647	3.900E+00	3.900E+00	5.000E-01
1N658	9.200E-01	9.200E-01	5.000E-01
1N660	2.900E-01	3.750E-02	5.370E-01
1N661	4.600E-01	4.600E-01	5.000E-01
1N662	5.400E-01	5.700E-04	9.540E-01
1N702A	1.000E+00	1.000E+00	5.000E-01
1N711A	2.100E+00	2.100E+00	5.000E-01
1N746A	1.600E+00	3.470E+00	4.400E-01
1N750A	2.340E+00	5.000E-02	7.900E-01
1N751A	6.300E+00	6.300E+00	5.000E-01
1N751A	1.200E+00	1.200E+00	5.000E-01
1N752A	1.059E+01	3.200E-01	7.700E-01
1N753A	1.479E+01	4.300E-01	7.300E-01
1N754A	1.120E+00	2.000E-02	7.900E-01
1N755A	1.334E+01	3.000E-02	9.600E-01
1N756	2.042E+01	9.200E-01	7.400E-01
1N757A	7.670E+00	1.000E-01	8.000E-01
1N758A	6.170E+00	2.630E-01	7.300E-01
1N763-2	3.000E+00	3.000E+00	5.000E-01
1N78	1.200E-03	1.200E-03	5.000E-01
1N733	7.700E-04	7.700E-04	5.000E-01
1N730A	2.000E-03	2.000E-03	5.000E-01
1N730	1.300E-03	1.300E-03	5.000E-01
1N816	5.200E+00	5.200E+00	5.000E-01
1N815	1.300E+00	1.500E+00	5.000E-01
1N82A	2.300E-03	2.300E-03	5.000E-01
1N82A	7.300E-04	7.300E-04	5.000E-01
1N821	1.910E-01	2.950E-01	8.300E-01
1N323	1.900E+00	1.900E+00	5.000E-01
1N914	7.200E-02	1.510E-03	7.600E 01
1N914	2.100E-01	2.200E-01	1.000E+00
1N914	9.600E-02	9.600E-02	5.000E-01
1N9330	1.000E-01	1.000E-01	5.000E-01
1N956B	1.500E+00	1.500E+00	5.000E-01
1N963B	5.170E+00	1.200E-01	8.000E-01
1N964B	1.300E+00	1.000E-04	1.170E+00
1N965B	1.300E+00	1.800E+00	5.000E-01
1N966B	7.590E+00	4.200E-02	6.600E-01
1N967	7.300E-01	7.300E-01	5.000E-01
1N970B	6.460E+00	2.300E-01	7.400E-01
1N972B	2.400E-01	7.590E-01	7.200E-01
1N973B	4.270E-01	9.120E-12	2.760E+00
1N974B	7.910E+00	2.570E-03	1.060E+00
1N981B	1.400E+00	1.400E+00	5.000E-01

COMPONENT TYPE: TRANSISTOR EMITTER-BASE	MODEL TYPE: DAMAGE

TOPOLOGY:



$$P_F = Kt^{-1/2}$$

PARAMETERIZATION:

START

$N_D = 4.49 \times 10^{18} \, (V_{BEBO})^{-1.5}$ — DOPING CONENTRATION

$V_{BDC} = 4.07 \times 10^{12} \, (N_D)^{-0.67}$ — BREAKDOWN VOLTAGE AT FAILURE

$\rho_{SC} = 2.48 \times 10^{25} \, (N_D)^{-1.80}$ — SPACE CHARGE RESISTIVITY

$\rho_{BLK} = 3.61 \times 10^{10} \, (N_D)^{-0.81}$ — BULK RESISTIVITY

$J_F = 3.8 \times 10^{-11} \, (N_D)^{0.88}$ — FAILURE CURRENT PER UNIT AREA

A — TO AREA CALCULATION

B

DAMAGE PARAMETER CALCULATIONS

$$R_{BLK} = \rho_{BLK}/AREA$$

$$R_{SC} = \rho_{SC}/AREA$$

$$I_{F_{100ns}} = J_F \cdot AREA$$

$$V_{F_{100ns}} = V_{BDC} + I_{F_{100ns}} (R_{BLK} + R_{SC})$$

$$I_{FP} = I_F \left(\frac{t_p}{100 \times 10^{-9}} \right)^{-1/2}$$

$$V_{FP} = V_{BDC} + I_{FP}(R_{BLK} + R_{SC})$$

$$K = \left(I_{F_{100ns}} \cdot V_{F_{100ns}} \right) \left(100 \times 10^{-9} \right)^{1/2}$$

Figure 5.7 Transistor-Emitter-Base Damage Prediction [5.15]

AREA CALCULATIONS:

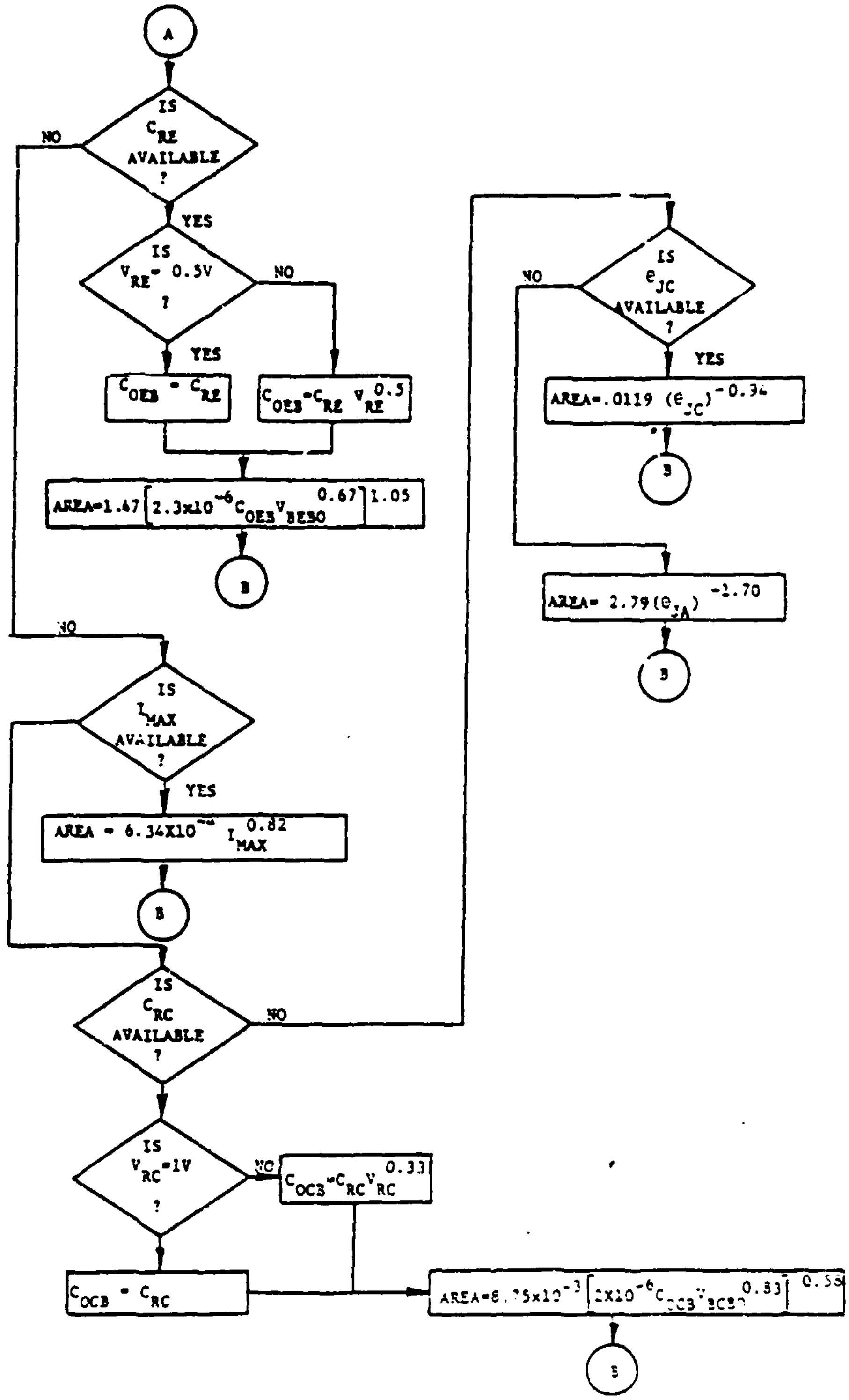


Figure 5.7 Transistor-Emitter Base Damage Prediction (cont'd) [illegible]

Definitions and Units:

R_{BLK} = Resistance of bulk semiconductor in ohms

V_{BDC} = Breakdown voltage at the critical failure temp, in volts

R_{SC} = Resistance associated with the space charge in an avalanching junction, in ohms

I_F = Current required for failure, in amperes

V_F = Voltage required for failure, in volts

N_D = Doping concentration of lightly doped side of the junction, in atoms/cm^3

V_{BEBO} = Breakdown voltage in emitter-base junction with collector open, in volts

V_{BCBO} = Breakdown voltage of collector-base junction with emitter open, in volts

ρ_{SC} = Space charge resistance per unit area in $\Omega \cdot cm^2$

ρ_{BLK} = Bulk resistance per unit area in $\Omega \cdot cm^2$

J_F = Failure current density in A/cm^2

AREA = Effective area of junction in square centimeters

I_{F100NS} = Failure current for a 100 nanosecond rectangular pulse, in amperes

V_{F100NS} = Failure voltage for a 100 nanosecond rectangular pulse, in volts

K = Wunsch damage constant in $W \cdot s^{1/2}$

t_p = Rectangular pulse width, in seconds

C_{RE} = Emitter-base reverse biased capacitance, in picofarads

V_{RE} = Voltage at which C_{RE} is measured, in volts

C_{OEB} = Emitter-base capacitance at 0.5 volt reverse bias in picofarads

I_{M} = Maximum rated collector current in amperes

Figure 5.7 Transistor-Emitter-Base Damage Prediction (cont'd) [5.15]

TRANSMITTER EMITTER-BASE

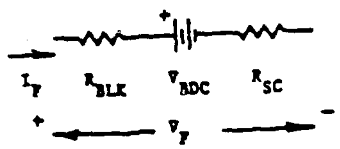
Definitions and units:

θ_{JC}	=	Thermal resistance, junction to case in °C/W
θ_{JA}	=	Thermal resistance, junction to ambient in °C/W
C_{RC}	=	Collector-base reverse biased capacitance, in picofarads
V_{RE}	=	Voltage at which C_{RC} is measured, in volts
C_{OCB}	=	Collector-base capacitance at 1 volt reverse bias, in picofarads

Figure 5.7 Transistor-Emitter-Base Damage Prediction (Concluded) [5.15]

COMPONENT TYPE:	MODEL TYPE:
Transistor Collector-Base	Damage

TOPOLOGY:



$$P_F = K t_p^{-1/2}$$

PARAMETERIZATION:

START

$$N_D = 4.49 \times 10^{18} (V_{BCBO})^{-1.5}$$ DOPING CONCENTRATION

$$V_{BDC} = 4.07 \times 10^{12} (N_D)^{-0.67}$$ BREAKDOWN VOLTAGE AT FAILURE

$$\rho_{SC} = 2.48 \times 10^{25} (N_D)^{-1.80}$$ SPACE CHARGE RESISTIVITY

$$\rho_{BLK} = 3.61 \times 10^{10} (N_D)^{-0.81}$$ BULK RESISTIVITY

$$J_F = 8.26 \times 10^{-11} (N_D)^{0.68}$$ FAILURE CURRENT PER UNIT AREA

A — TO AREA CALCULATION

B

DAMAGE PARAMETER CALCULATIONS

$$R_{BLK} = \rho_{BLK}/AREA$$

$$R_{SC} = \rho_{SC}/AREA$$

$$I_{F_{100ns}} = J_F \cdot AREA$$

$$V_{F_{100ns}} = V_{BDC} + I_{F_{100ns}} (R_{BLK} + R_{SC})$$

$$I_{FP} = I_F \left(\frac{t_p}{100 \times 10^{-9}} \right)^{-1/2}$$

$$V_{FP}(t_p) = V_{BDC} + I_{FP} (R_{BLK} + R_{SC})$$

$$K = \left(I_{F_{100ns}} \cdot V_{F_{100ns}} \right) \left(100 \times 10^{-9} \right)^{1/2}$$

Figure 5.8 Transistor Collector-Base Damage Predictions [5.15]

TRANSISTOR COLLECTOR BASE

AREA CALCULATION:

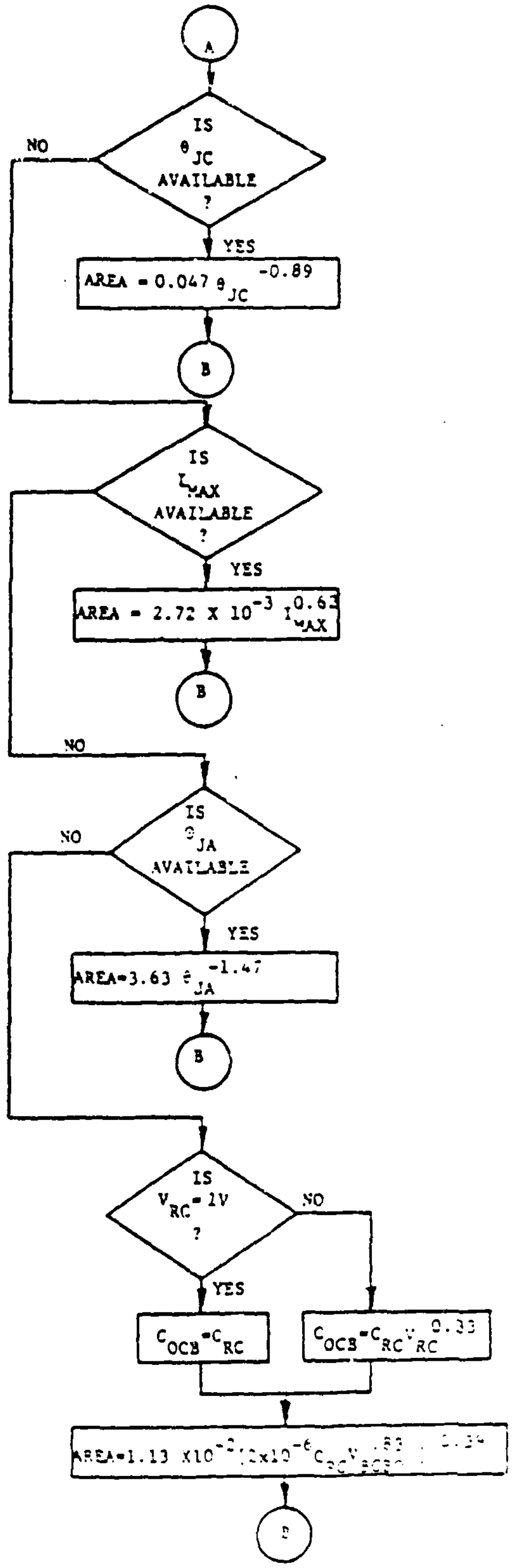


Figure 5.8 Transistor Collector-Base Damage Predictions (cont'd) [5.15]

DEFINITIONS AND UNITS:

R_{BLK}	=	Resistance of bulk semiconductor in ohms
V_{BDC}	=	Breakdown voltage at the critical failure temp, in volts
R_{SC}	=	Resistance associated with the space charge an avalanching junction, in ohms
I_F	=	Current Required for failure, . . amperes
V_F	=	Voltage required for failure, in volts
N_D	=	Doping concentration of lightly doped side of the junction, in atoms/cm3
V_{BCBO}	=	Breakdown voltage of collector-base junction with emitter open, in volts
ρ_{SC}	=	Space charge resistance per unit area in $\Omega \cdot cm^2$
ρ_{BLK}	=	Bulk resistance per unit area in $\Omega \cdot cm^2$
J_F	=	Failure current density in A/cm^2
AREA	=	Effective area of junction in square centimeters
I_{F100NS}	=	Failure current for a 100 nanosecond rectangular pulse, in amperes
V_{F100NS}	=	Failure voltage for a 100 nanosecond rectangular pulse, in volts
K	=	Wunsch damage constant in $W \cdot s^{1/2}$
t_p	=	Rectangular pulse width, in seconds
I_{MAX}	=	Maximum rated collector current, in amperes
θ_{JC}	=	Thermal resistance, junction to case in °C/W
θ_{JA}	=	Thermal resistance, junction to ambient in °C/W
C_{RC}	=	Collector-base reverse biased capacitance, in picofarads
V_{RC}	=	Voltage at which C_{RC} is measured, in volts
C_{JCB}	=	Collector-base capacitance at 1 volt reverse bias, in picofarads

Figure 5.8 Transistor Collector-Base Damage Predictions (Concluded) [5.15]

Table 5.4 Transistor Emitter-Base Damage Parameters [5.8]

DEVICE	MUNSCH K	GENERALIZED MUNSCH A	GENERALIZED MUNSCH B
SM692-1	5.000E-03	5.000E-03	5.000E-01
2N1016A	1.500E+00	1.500E+00	5.000E-01
2N1039	1.400E+00	1.400E+00	5.000E-01
2N1099	1.000E+00	1.000E+00	5.000E-01
2N1115	3.300E-01	3.300E-01	5.000E-01
2N1116A	9.300E-01	9.300E-01	5.000E-01
2N1118	1.900E-01	1.900E-01	5.000E-01
2N1132	2.300E-01	2.300E-01	5.000E-01
2N1132A	1.300E-01	1.300E-01	5.000E-01
2N1132A	2.100E-01	2.100E-01	5.000E-01
2N1132A	5.700E-01	5.700E-01	5.000E-01
2N1204	1.000E-02	1.000E-02	5.000E-01
2N1308	1.300E-01	1.300E-01	5.000E-01
2N1308	1.000E-02	4.500E-03	5.507E-01
2N1469	6.500E-01	6.500E-01	5.000E-01
2N1485	2.390E+00	1.560E-04	1.170E+00
2N1486	1.560E+00	1.350E-01	5.320E-01
2N1613	1.000E+00	1.000E+00	5.000E-01
2N1642	1.300E-01	1.300E-01	5.000E-01
2N1711	1.300E-01	1.300E-01	5.000E-01
2N1711	1.299E-01	2.640E-01	4.500E-01
2N176	1.010E+00	3.330E+00	4.200E-01
2N1893	4.000E-01	4.000E-01	5.000E-01
2N190	5.800E-01	5.800E-01	5.000E-01
2N2102	4.390E-01	1.370E-02	7.210E-01
2N2193	5.500E-01	5.500E-01	5.000E-01
2N2222	1.100E-01	3.000E-02	5.000E-01
2N2222	3.000E-02	-0.	5.000E-01
2N2297	5.000E-01	5.000E-01	5.000E-01
2N2297	1.000E+00	1.000E+00	5.000E-01
2N2405	2.367E-01	1.372E+00	3.300E-01
2N2432	9.566E-02	1.389E-01	4.409E-01
2N2453	3.000E-02	3.000E-02	5.000E-01
2N2453	6.000E-02	6.000E-02	5.000E-01
2N2481	2.330E-02	1.540E-02	5.280E-01
2N2483	3.400E-02	4.250E-01	3.230E-01
2N2484	6.500E-02	3.100E-02	5.440E-01
2N270	5.000E-01	2.000E-02	1.000E+00
2N2708	9.701E-03	1.223E-01	3.120E-01
2N2727	2.100E+00	1.200E-03	1.000E+00
2N2801	1.100E-01	1.100E-01	5.000E-01
2N2801	2.200E-01	2.200E-01	5.000E-01
2N2857	8.500E-03	2.450E-01	2.570E-01
2N2894	3.500E-02	2.370E-02	5.290E-01
2N2906	4.400E-02	4.400E-02	5.000E-01
2N2907	1.400E-01	1.400E-01	5.000E-01
2N2907A	1.000E-01	1.000E-01	5.000E-01
2N2920	4.000E-02	4.000E-02	5.000E-01
2N2945	2.258E-02	1.673E-03	6.337E-01
2N297A	1.300E+00	1.300E+00	5.000E-01
2N297A	9.000E-01	9.000E-01	5.000E-01
2N3019	4.410E-01	5.740E-02	5.400E-01
2N3057	1.444E-01	2.734E-01	4.323E-01
2N3114	1.340E-01	1.610E-01	4.370E-01
2N3251	6.400E-02	3.020E-04	3.350E-01

Table 5.4 Transistor-Emitter-Base Parameters (Concluded) [5.8]

DEVICE	WUNSCH	GENERALIZED WUNSCH	
	K	A	B
2N328A	4.200E-02	1.600E-01	1.000E+00
2N329	2.200E-01	2.200E-01	5.000E-01
2N335	5.500E-01	5.500E-01	5.000E-01
2N335	5.300E-01	5.300E-01	5.000E-01
2N336	5.500E-01	5.500E-01	5.000E-01
2N336A	3.400E-01	3.400E-01	5.000E-01
2N338	4.600E-02	7.640E+00	1.400E-01
2N343	4.700E-02	4.700E-02	5.000E-01
2N3440	1.100E+00	1.100E+00	5.000E-01
2N3468	4.420E-01	7.060E-02	6.230E-01
2N3503	3.197E-01	1.454E+00	3.929E-01
2N3585	3.430E+00	9.320E-01	6.360E-01
2N3636	1.000E+00	1.000E+00	5.000E-01
2N3677	7.515E-02	6.294E-01	3.502E-01
2N3700	4.010E-01	4.540E+00	3.131E-01
2N375	1.020E+00	1.020E+00	5.000E-01
2N389	2.140E+00	2.140E+00	5.000E-01
2N4033	3.095E-01	7.627E-01	4.359E-01
2N4044	-0.	2.730E-03	3.230E-01
2N463	5.700E+00	5.700E+00	5.000E-01
2N495A	5.500E-01	8.000E-01	5.000E-01
2N498	8.000E-01	3.000E-01	5.000E-01
2N5117	-0.	3.290E-03	3.900E-01
2N525	3.900E-01	3.900E-01	5.000E-01
2N526	1.100E+00	1.100E+00	5.000E-01
2N576A	2.300E-02	2.300E-02	5.000E-01
2N598	5.000E-01	5.000E-01	5.000E-01
2N613	3.300E-01	3.300E-01	5.000E-01
2N656	2.000E-01	2.000E-01	5.000E-01
2N657	6.200E-01	6.200E-01	5.000E-01
2N657A	1.070E+00	1.070E+00	5.000E-01
2N697	1.140E+00	4.340E+00	2.460E-01
2N699	2.500E-01	2.500E-01	5.000E-01
2N706	7.500E-03	7.500E-03	5.000E-01
2N706	3.000E-02	3.000E-02	5.000E-01
2N713A	3.253E-01	1.613E+00	3.712E-01
2N736	1.000E-01	1.000E-01	5.000E-01
2N733	1.100E-01	5.300E-01	1.000E+00
2N750	3.400E-02	3.400E-02	5.000E-01
2N834	1.500E-02	6.200E-02	4.000E-01
2N854	1.300E-01	1.300E-01	5.000E-01
2N869A	1.700E-02	3.100E-01	3.000E-01
2N916	5.100E-02	4.900E-02	5.030E-01
2N918	3.600E-03	2.090E+00	7.320E-02
2N927	9.500E-02	9.500E-02	5.000E-01
2N930	4.600E-02	4.600E-02	5.000E-01
2N930	5.400E-02	8.300E-03	6.290E-01
2N930A	2.000E-02	2.000E-02	5.000E-01
2N956	1.104E-01	6.161E-01	3.571E-01

Table 5.5 Transistor collector-base damage parameters [5.8]

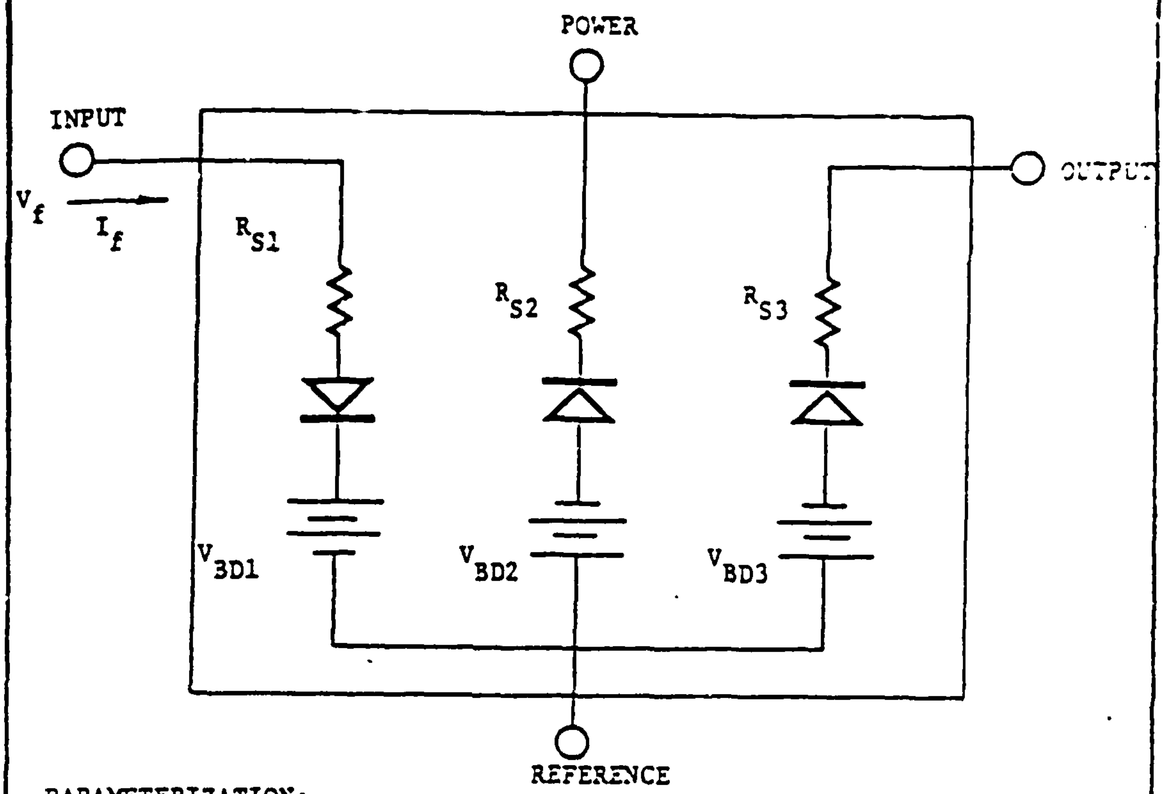
DEVICE	GENERALIZED WUNSCH A	B
2N1485	1.010E+00	5.000E-01
2N1486	2.660E-02	1.060E-01
2N1711	2.377E-01	5.000E-01
2N176	9.580E-01	5.000E-01
2N2102	4.710E-01	5.000E-01
2N2405	8.502E-02	5.000E-01
2N2432	2.727E-01	4.409E-01
2N2708	1.898E-01	3.135E-01
2N2857	1.730E-02	5.000E-01
2N2907	4.450E-02	5.000E-01
2N2945	9.605E-04	7.514E-01
2N3057	6.465E-02	5.828E-01
2N3114	3.120E-01	5.070E-01
2N3251	6.150E-04	8.810E-01

Table 5.5 Transistor collector-base damage parameters [5.8] (Concluded)

	GENERALIZED WUNSCH	
DEVICE	A	B
2N338	1.160E+01	2.800E-01
2N3503	5.650E-01	5.000E-01
2N3585	1.140E+00	5.000E-01
2N3677	9.359E-02	5.000E-01
2N4033	2.719E-01	5.000E-01
2N697	3.900E+01	1.260E-01
2N706	5.800E-02	5.000E-01
2N718A	4.094E-02	6.416E-01
2N834	2.500E-02	5.000E-01
2N869A	2.000E-02	5.000E-01
2N916	9.750E-02	5.000E-01
2N930	3.820E-03	7.560E-01
2N956	1.223E+00	3.451E-01

COMPONENT TYPE: INTEGRATED CIRCUIT

MODEL TYPE: DAMAGE



PARAMETERIZATION:

START

DETERMINE TECHNOLOGY AND TERMINAL

SELECT VALUES FOR A, B, V_{BD}, RS FROM TABLE A

$$P_F = At_p^{-B}$$

$$I_F = \frac{-V_{BD} + \sqrt{V_{BD}^2 + 4R_S P_F}}{2R_S}$$

$$V_F = V_{BD} + I_F R_S$$

Figure 5.9 Integrated Circuit Damage Prediction [5.15]

INTEGRATED CIRCUIT

		Definitions and units:
A	=	Damage constant in $W\text{-}S^B$
B	=	Exponent of damage equation, unitless
V_{BD}	=	Equivalent breakdown voltage in volts
R_S	=	Total surge resistance in ohms
P_F	=	Failure power in watts
I_F	=	Failure currents in amperes
V_F	=	Failure voltage in volts
t_p	=	Pulse width of rectangular pulse in seconds

Figure 5.9 Integrated Circuit Damage Prediction (Concluded) [5.15]

Table 5.6 Integrated Circuit Damage Model Parameters by Category [5.15]

Category: Family	Category: Terminal	A	B	V_{BD} (Volts)	R_S (Ohms)	Lower 95% A	Upper 95% A
TTL	Input	0.00216	0.689	7	16	0.00052	0.00896
	Output	0.00359	0.722	15	2.4	0.00098	0.013
RTL	Input	0.554	0.384	6	40	0.12	2.6
	Output	0.0594	0.508	5	18.9	0.0096	0.39
	Power	0.0875	0.555	5	20.8	0.026	0.70
DTL	Input	0.0137	0.580	7	25.2	0.0046	0.041
	Output	0.0040	0.706	1	-15.8	0.012	0.136
	Power	0.0393	0.576	1	30.6	0.009	0.17
ECL	Input	0.152	0.441	20	15.7	0.045	0.51
	Output	0.0348	0.558	0.7	7.6	0.0031	0.397
	Power	0.456	0.493	0.7	8.9	0.22	0.935
MOS	Input	0.0546	0.403	30	9.2	0.0063	0.47
	Output	0.0014	0.319	0.6	11.6	0.00042	0.0046
	Power	0.105	0.513	3	10.4	0.038	0.29
Linear	Input	0.0743	0.509	7	13.2	0.0054	1.01
	Output	0.0139	0.714	7	5.5	0.0045	0.043

At present there are no parameterization techniques for IC's which use measured data or specification sheet values. However, because of the tight tolerances used in IC manufacturing, the category parameters usually predict the failure levels quite well. One should use caution when applying the categories, especially the linear category. Power regulators are frequently much harder than predicted by the category models. On the other hand, some interface circuits may actually be softer. To insure a conservative analysis, it is best to use the lower 95 percent values of A.

Measured damage constants for some integrated circuits are presented in Tables 5.7 and 5.8 for digital and linear ICs respectively.

5.2.1.4 Other Semiconductor Devices

Failure models for other semiconductor devices such as silicon controlled rectifiers (SRCs), silicon control switches (SCSs), thyristors, are not well established. SRCs, thyristors, and other switching semiconductors have been tested to failure [5.26]. The Wunsch model for transistors is used for three terminal devices and the general Wunsch model for ICs can be used for devices with more than two junctions. A sample SUPERSAP2 listing in Table 5.9 shows the Wunsch damage constants for some SRCs and biased junction switches. Measured damage constants for some three junction devices are shown in Table 5.10.

5.2.2 Resistors

Resistors have been found to fail by thermal effects. The most susceptible resistor types are metal film and carbon composition resistors. In the time regime of 100 ns to 10 μs, resistors fail adiabatic heating of the material. Hence, the power required for failure is

$$P_f = K\, t_p^{-1} \tag{5.8}$$

where t_p is the rectangular pulse width. Note the power relation in (5.8) is different from that in (5.1) which corresponds to quasiadiabatic heating of the material. Figure 5.10 and 5.11 show the process for determining the Wunsch damage constants from the physical dimensions of the two resistor types. These damage constants can then be used to compute the failure power, current, and voltage of the device.

5.2.3 Capacitors

Capacitors fail by dielectric breakdown caused by transients at higher voltages than the voltage rating of the capacitor. The failure voltage and current are given by:

$$V_f = V_{BR} \tag{5.9}$$

with V_{BR} the capacitor voltage breakdown rating, and

$$I_f = C \frac{d}{dt} V_f \approx 2\pi f C V_f, \tag{5.10}$$

with C the capacitance and f is the frequency of the damped sinusoid pulse.

Table 5.7 Digital Integrated Circuit Damage Parameters [5.8]

NUMBER	FAMILY	INPUT A	INPUT B	OUTPUT A	OUTPUT B	POWER A	POWER B
AM9621	DTL	-0.	-0.	4.000E-02	4.780E-01	-0.	-0.
CD4000A	CMOS	2.976E-01	4.053E-01	-0.	-0.	-0.	-0.
CD4000AD	CMOS	7.620E-01	3.550E-01	2.230E-02	5.950E-01	2.400E-01	5.150E-01
CD4000AE	CMOS	4.500E+00	2.630E-01	5.530E-04	3.330E-01	3.930E-01	4.110E-01
CD4024	CMOS	1.600E+00	5.000E-01	1.900E-01	5.000E-01	-0.	-0.
DM6820AJ	TTL	2.340E-01	2.680E-01	-0.	-0.	-0.	-0.
DM8830J	TTL	-0.	-0.	1.220E-01	6.360E-01	-0.	-0.
DM933N	DTL	4.410E-01	3.730E-01	3.370E-02	5.340E-01	-0.	-0.
DM946	DTL	3.624E-01	3.569E-01	7.112E-03	6.388E-01	6.177E-02	5.000E-01
DM946N	DTL	4.200E-03	6.480E-01	2.400E-03	7.230E-01	9.200E-03	5.420E-01
DM948	DTL	2.630E-02	5.430E-01	3.410E-02	5.190E-01	1.450E-02	5.700E-01
DRA2001	TTL	9.000E-02	5.000E-01	-0.	-0.	-0.	-0.
DTMUL93359	DTL	2.500E-03	7.620E-01	1.917E-01	4.540E-01	-0.	-0.
DTMUL94459	DTL	2.120E-01	5.110E-01	1.917E-01	4.540E-01	-0.	-0.
HD-4000-01	CMOS	2.259E-03	7.540E-01	-0.	-0.	-0.	-0.
INS4007	CMOS	1.000E-04	5.000E-01	1.700E-02	5.000E-01	-0.	-0.
INS4012S	CMOS	1.465E-02	5.000E-01	-0.	-0.	-0.	-0.
I3101	STTL	1.000E-01	5.000E-01	-0.	-0.	-0.	-0.
MC14000CL	MOS	1.990E+00	1.340E-01	1.570E-04	9.910E-01	2.100E-02	6.360E-01
MC14000CP	MOS	1.140E+00	2.080E-01	5.310E-03	7.530E-01	4.370E-02	5.620E-01
MC1488L	DTL	6.470E-02	4.360E-01	2.300E-03	7.370E-01	-0.	-0.
MC1489L	DTL	1.540E-01	4.000E-01	3.130E-05	9.360E-01	-0.	-0.
MC1678	ECTL	2.000E-01	5.000E-01	-0.	-0.	-0.	-0.
MC2255L	CMOS	1.151E-01	5.000E-01	-0.	-0.	-0.	-0.
MC301	ECTL	3.120E-01	7.290E-01	2.410E-01	7.990E-01	3.370E-00	1.570E-00
MC304G	ECTL	1.630E-01	6.350E-01	3.640E-02	6.290E-01	7.950E-01	4.420E-01
MC308G	ECTL	3.420E-01	3.820E-01	8.600E-03	5.510E-01	3.350E-01	5.490E-01
MC317F	ECTL	2.990E-02	5.550E-01	9.000E-03	6.900E-01	3.630E-02	5.030E-01
MC351	ECTL	8.000E-03	5.000E-01	-0.	-0.	-0.	-0.
MC4006	TTL	6.270E-02	4.750E-01	2.290E-03	7.930E-01	-0.	-0.
MC4043P	TTL	5.700E-04	8.460E-01	6.730E-01	4.350E-01	-0.	-0.
MC7400L	TTL	5.640E-06	1.060E+00	3.440E-04	8.520E-01	-0.	-0.
MC914	RTL	5.745E-02	5.000E-01	4.203E-02	5.000E-01	4.366E-02	5.000E-01
N7400P	TTL	2.190E-04	9.490E-01	6.300E-01	3.170E-01	-0.	-0.
RC930	DTL	3.100E-03	6.720E-01	1.490E-04	9.380E-01	2.450E-02	5.730E-01
SE140	TTL	1.550E-01	8.370E-01	1.230E-01	9.010E-01	4.310E-01	3.540E-01
SE156W	TTL	5.350E-03	6.240E-01	1.300E-03	8.200E-01	1.630E-02	5.660E-01
SE160J	TTL	1.050E-01	4.340E-01	1.300E-03	3.200E-01	-0.	-0.
SN15-946	DTL	4.350E-02	1.070E+00	5.750E-02	8.590E-01	3.090E-01	7.470E-01

Table 5.7 Digital Integrated Ciruit Damage Parameters (Concluded) [5.8]

NUMBER	FAMILY	INPUT		OUTPUT		POWER	
		A	B	A	B	A	B
SN54S191	STTL	5.000E-03	5.000E-01	-0.	-0.	-0.	-0.
SN5420	TTL	1.300E-02	5.000E-01	-0.	-0.	-0.	-0.
SN74H00	TTL	6.260E-03	5.900E-01	2.970E-04	8.950E-01	-0.	-0.
SN74H05	TTL	3.500E-02	7.020E-01	-0.	-0.	-0.	-0.
SN74H60N	TTL	4.600E-06	7.250E-01	-0.	-0.	-0.	-0.
SN74L00	TTL	1.590E+00	2.220E-01	1.300E-03	8.200E-01	-0.	-0.
SN74L71	TTL	3.740E-01	3.420E-01	1.300E-03	3.200E-01	-0.	-0.
SN74L73	TTL	2.090E-02	4.520E-01	1.300E-03	8.200E-01	2.390E-01	5.430E-01
SN74L95	TTL	3.550E-02	5.080E-01	-0.	-0.	-0.	-0.
SN74S00	STTL	7.400E-03	5.360E-01	3.260E-02	6.770E-01	-0.	-0.
SN7400	TTL	6.140E-03	6.270E-01	2.010E-03	7.970E-01	-0.	-0.
SN7402	TTL	1.480E-03	7.530E-01	4.290E-03	7.240E-01	-0.	-0.
SN7413N	DTL	2.270E-01	4.320E-01	1.600E-03	8.380E-01	-0.	-0.
SN74163N	TTL	3.500E-03	6.480E-01	3.400E-04	7.910E-01	3.300E-04	7.830E-01
SN7490	TTL	5.000E-04	6.190E-01	2.450E-02	5.390E-01	2.400E-02	6.550E-01
SN751071	TTL	7.300E-03	6.220E-01	-0.	-0.	-0.	-0.
0456	PMOS	6.000E-02	5.000E-01	-0.	-0.	-0.	-0.
1101	PMOS	1.200E-02	5.000E-01	-0.	-0.	-0.	-0.
1402	PMOS	4.100E-02	5.000E-01	-0.	-0.	-0.	-0.
4501	DTL	6.000E-03	5.000E-01	-0.	-0.	-0.	-0.
7400DC	TTL	3.720E-05	9.550E-01	3.370E-01	3.540E-01	-0.	-0.
3223	STTL	3.000E-03	5.000E-01	-0.	-0.	-0.	-0.
3431	DTL	1.080E-01	9.020E-01	1.250E-01	7.350E-01	5.330E-01	1.090E+00
9093DC	DTL	9.432E-04	7.983E-01	-0.	-0.	5.033E-03	6.201E-01
9109	DTL	-0.	-0.	3.456E-01	3.556E-01	3.224E+00	3.332E-01
9344	TTL	1.000E-01	-0.	-0.	-0.	-0.	-0.
9908HC	DTL	5.390E+00	2.380E-01	5.100E-03	6.700E-01	2.360E-01	4.710E-01
9909HC	RTL	2.590E-01	4.210E-01	6.400E-03	6.370E-01	3.300E-03	7.490E-01
9910HC	RTL	3.100E-03	6.600E-01	1.140E-02	6.020E-01	3.390E-01	3.350E-01
9911HC	RTL	4.450E-02	5.290E-01	1.220E+00	2.120E-01	2.800E-02	6.490E-01
9912HC	RTL	3.610E-01	4.310E-01	3.490E+00	1.990E-01	7.400E-02	5.670E-01
4930	DTL	2.130E-01	1.130E+00	1.260E-01	9.630E-01	2.070E-01	1.010E+00
9930HC	DTL	8.300E-03	5.300E-01	2.410E-02	5.420E-01	4.390E-02	5.210E-01
9932HC	DTL	7.310E-01	2.730E-01	4.400E-03	5.840E-01	2.100E-01	4.150E-01
9944DM	DTL	5.200E-03	6.110E-01	2.310E-02	5.330E-01	5.700E-02	4.410E-01
9945DM	DTL	1.130E-02	5.640E-01	9.700E-03	5.990E-01	1.750E-01	5.140E-01
9945HC	DTL	1.110E-01	4.230E-01	9.100E-06	1.070E+00	2.600E-01	5.070E-01
9946HC	DTL	1.700E-03	7.380E-01	4.000E-05	1.003E+00	1.250E-01	5.400E-01
9948HC	DTL	6.300E-03	6.340E-01	1.300E-03	7.300E-01	1.030E-02	7.040E-01

Table 5.8 Linear integrated circuit damage parameters [5.8]

NUMBER	INPUT		OUTPUT		POWER	
	A	B	A	B	A	B
AM111	1.000E-02	3.980E-01	1.990E-01	6.690E-01	-0.	-0.
CA3015A	1.075E-02	5.000E-01	-0.	-0.	2.659E-01	5.396E-01
LM103-1.8V	2.290E-02	5.720E-01	-0.	-0.	-0.	-0.
LM103-5.6V	7.620E-03	6.440E-01	-0.	-0.	-0.	-0.
LM105H	3.300E-03	7.210E-01	1.152E-01	4.290E-01	7.200E-04	8.770E-01
LM111H	1.010E-01	3.260E+02	9.580E-03	7.060E-01	1.290E-02	7.090E-01
LM302	2.650E-02	6.320E-01	8.610E-03	7.270E-01	-0.	-0.
MC1530	4.900E-03	5.660E-01	7.200E-01	8.900E-01	6.400E+00	2.300E-01
MC1530G	2.062E-03	6.135E-01	2.805E-01	5.000E-01	7.000E+00	2.289E-01
MC1533	3.744E-02	3.797E-01	6.043E-01	3.533E-01	1.064E-01	5.000E-01
N57101	5.290E-03	6.900E-01	2.560E-01	4.500E-01	-0.	-0.
SNR3600	2.363E+00	3.345E-01	-0.	-0.	-0.	-0.
SNR3610	-0.	-0.	7.006E-01	4.408E-01	-0.	-0.
SN72709	3.960E-01	6.530E-01	3.690E+00	1.750E-01	2.050E+00	3.980E-01
UA709	1.100E-02	5.000E-01	1.100E-02	5.000E-01	-0.	-0.
UA715	1.019E-01	5.820E-01	2.189E-01	5.420E-01	-0.	-0.
UA740	1.620E-01	5.380E-01	6.500E-02	6.620E-01	-0.	-0.
UA741	2.740E-03	7.190E-01	-0.	-0.	-0.	-0.
UA747	1.890E+00	3.580E-01	1.510E-02	7.500E-01	-0.	-0.
UA776	2.500E-03	7.250E-01	3.860E-02	6.580E-01	1.101E-01	5.690E-01
709HC	7.700E-03	5.020E-01	1.620E-02	6.680E-01	7.420E-01	4.530E-01
709R	2.690E-02	9.340E-01	3.150E-02	6.620E-01	7.150E-02	6.750E-01

Table 5.9 Sample SUPERSAP2 Listing for Selected Semiconductors

RECORD	NUMBER	VENDOR	FUNCTION	STRUCTURE	PACKAGE	POWER	FREQUENCY	RISETIME	NUMSCH
97	2N6256	MOTA	MISC		T066	50.0	0.	0.	.131
98	2N656	TII	BJTSN	D.PL	T05	0.	0.	0.	.200
99	2N657	TII	BJTSN	D.PL	T05	4.00	0.	0.	.620
100	2N657A	GESY	BJTSN	ME.	T05	0.	0.	0.	1.07
101	2N685	GESY	SCR		T018	0.	0.	0.	1.40
102	2N687	GESY	SCR		T048	0.	0.	0.	11.7
103	2N697	MOTA	BJTSN	D.ME	T05	.600	100.	0.	1.14
104	2N699	FSC	BJTSN	D.PL	T05	0.	0.	0.	.250
105	2N706	TII	BJTSN	D.ME	T018	0.	0.	0.	7.500E-03
106	2N708	FSC	BJTSN	PL.	T018	0.	0.	0.	3.000E-02
107	2N718A	MOTA	BJTSN	D	T018	.500	60.0	0.	.326
108	2N716	MOTA	BJTSN	PL.	T018	0.	0.	0.	.100

RECORD	CURRENT	GAIN	DATA	REFERENCE	INPUT	INVOLT	INZ	INCASETR	INAMBTR	INJUNCAP
97	4.00	4.00	M-00	BASE	EMITTER	5.00	0.	3.50	3.93	49.5
98	0.	0.	M-05	BASE	EMITTER	8.00	0.	0.	0.	60.0
99	0.	0.	M-01	BASE	EMITTER	8.00	0.	43.0	219.	60.0
100	0.	0.	M-01	BASE	EMITTER	100.	0.	0.	0.	0.
101	0.	0.	M-01	BASE	EMITTER	200.	0.	0.	0.	0.
102	0.	0.	M-04	BASE	EMITTER	300.	0.	0.	0.	0.
103	0.	0.	M-12	BASE	EMITTER	5.00	0.	0.	0.	0.
104	0.	0.	M-01	BASE	EMITTER	5.00	0.	0.	0.	0.
105	0.	0.	M-04	BASE	EMITTER	3.00	0.	0.	0.	0.
106	0.	0.	M-04	BASE	EMITTER	5.00	0.	0.	0.	0.
107	0.	30.0	D-15	BASE	EMITTER	4.20	0.	0.	0.	0.
108	0.	0.	M-01	BASE	EMITTER	5.00	0.	0.	0.	0.

RECORD	INMODELF	INKF1	INMODELR	INKR1	INKR2	OUTPUT	OUTVOLT	OUTCASETR	OUTAMBTR	OUTJUNCAP
97	EXPO	20.7		4.600E-02	-.522	COLLECTOR	60.0	0.	0.	33.0
98		0.	NUMSCH	.200	0.	COLLECTOR	60.0	0.	0.	13.0
99		0.	NUMSCH	.620	0.	COLLECTOR	100.	0.	0.	13.0
100		0.	NUMSCH	1.07	0.		100.	0.	0.	0.
101		0.	NUMSCH	1.[illegible]	0.		0.	0.	0.	0.
102		0.	NUMSCH	1[illegible]	0.		0.	0.	0.	0.
103		0.	EXPO	4.34	.246	COLLECTOR	60.0	87.5	292.	20.0
104		0.	NUMSCH	.250	0.	COLLECTOR	120.	0.	0.	12.6
105		0.	NUMSCH	7.500E-03	0.	COLLECTOR	25.0	0.	0.	5.00
106		0.	NUMSCH	3.000E-02	0.	COLLECTOR	40.0	0.	0.	6.00
107		0.	EXPO	1.61	.171	COLLECTOR	139.	0.	350.	25.0
108		0.	NUMSCH	.100	0.	COLLECTOR	40.0	0.	0.	10.0

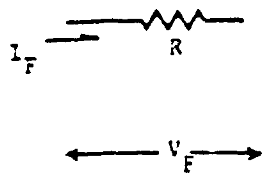
RECORD	OUTMODELF	OUTKF1	OUTMODELR	OUTKR1	OUTKR2	INZBLKS	INZBLKS0	INKFZ	OUTZBLKS	OUTZBLKS0
97		0.		0.	0.	33.0	0.	-.170	26.7	0.
98		0.		0.	0.	0.	0.	0.	0.	0.
99		0.		0.	0.	0.	0.	0.	0.	0.
100		0.		0.	0.	0.	0.	0.	0.	0.
101		0.		0.	0.	0.	0.	0.	0.	0.
102		0.		0.	0.	0.	0.	0.	0.	0.
103		0.	EXPO	31.0	.126	0.	0.	0.	0.	0.
104		0.		0.	0.	0.	0.	0.	0.	0.
105		0.		0.	0.	0.	0.	0.	0.	0.
106		0.		0.	0.	0.	0.	0.	0.	0.
107		0.	EXPO	4.410E-02	.062	4.25	0.	0.	1.40	0.
108		0.		0.	0.	0.	0.	0.	0.	0.

Table 5.10 Damage Parameters for Other Three Terminal Devices [5.8]

Device	Wunsch K	Breakdown Voltage	Bulk Resistance	Forward Failure Constant	Failure	A	B
				JFET			
				GATE-SOURCE DAMAGE PARAMETERS			
2N3069	1.1E-01	5.0E+01	0.0	0.0	VOLT	1.00E+02	0.0
2N4393	1.5E-01	4.0E+01	0.0	0.0	EXPO	1.24E-02	6.14E-01
				SCR			
				GATE-CATHODE DAMAGE PARAMETERS			
2N1596	9.04E-01	1.0E+02	0.0	0.0	WUNSCH	9.40E-01	0.0
2N1602	4.00E-01	0.0	0.0	0.0	"	4.00E-01	0.0
2N1777A	4.00E+00	0.0	0.0	0.0	"	4.00E+00	0.0
2N2323	4.00E-01	5.0E+01	0.0	0.0	"	4.00E-01	0.0
2N2346	3.80E+00	0.0	0.0	0.0	"	3.80E+00	0.0
2N685	1.40E+00	2.0E+02	0.0	0.0	"	1.40E+00	0.0
2N687	1.17E+01	3.0E+02	0.0	0.0	"	1.17E+01	0.0
				UJT			
				EMITTER-BASE 1 DAMAGE PARAMETERS			
2N489A	1.6E-01	6.0E+01	6.0E+01	0.0	TASCA	1.00E+02	0.0
2N491	0.0	0.0	0.0	0.0	EXPO	4.97E+00	5.33E-01

COMPONENT TYPE:	MODEL TYPE:
FILM RESISTOR	DAMAGE

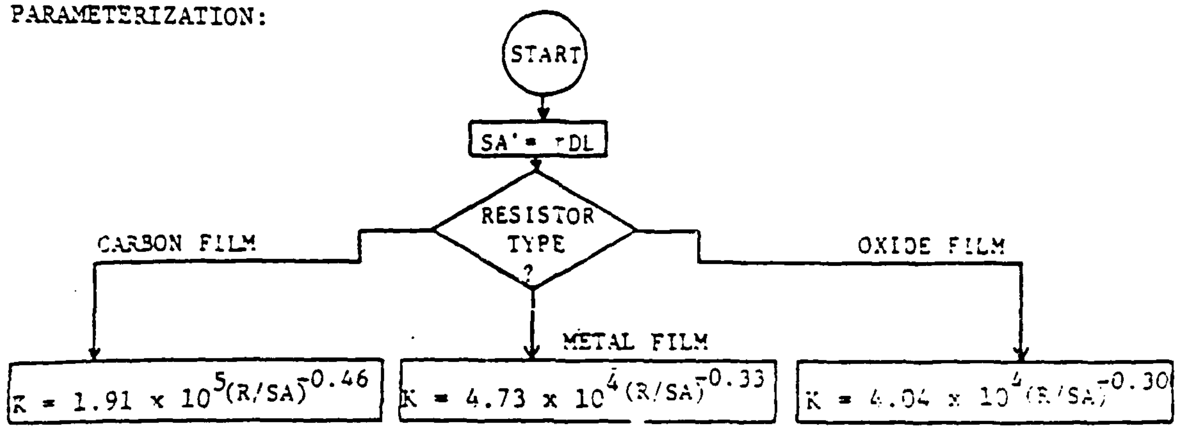
TOPOLOGY:



$$P_F = I_F V_F = K t_p^{-1}$$

$$I_F = \sqrt{\frac{P_F}{R}} \qquad V_F = \sqrt{P_F R}$$

PARAMETERIZATION:



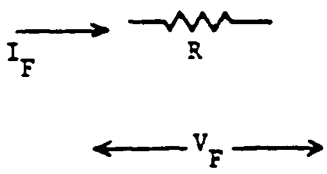
Definitions and units:

R	=	Rated resistance value in ohms
I_F	=	Failure current in amperes
V_F	=	Failure voltage in volts
P_F	=	Failure power in watts
K	=	Damage constant in W·s
t_p	=	Pulse width in seconds
SA	=	Surface area in square centimeters
D	=	Diameter of resistor inside end caps in centimeters
L	=	Length of resistor inside end caps in centimeters

Figure 5.10 Film Resistor Damage Predictions [5.15]

COMPONENT TYPE: CARBON COMPOSITION RESISTOR	MODEL TYPE: DAMAGE

TOPOLOGY:



$$P_F = V_F I_F = K t_p^{-1}$$

$$I_F = \sqrt{\frac{P_F}{R}} \qquad V_F = \sqrt{P_F R}$$

PARAMETERIZATION:

START

$$\boxed{V = \pi \left(\frac{D}{2}\right)^2 L}$$

$$\boxed{K = 1.85 \times 10^6\ V^{0.62}}$$

Definitions and units:

R = Rated resistance value in ohms

I_F = Failure current in amperes

V_F = Failure voltage in volts

P_F = Failure power in watts

K = Damage constant in W·s

t_p = Pulse width in seconds

V = Volume in cubic centimeters

D = Diameter of the resistor in centimeters

L = Length of the resistor in centimeters

Figure 5.11 Carbon Composition Resistor Damage Predictions [5.15]

5.2.4 Inductors and Transformers

For EMP induced transients, inductors and transformers may experience coil-to-coil arcing. This coil-to-coil arcing can degrade the performance of the inductor or transformer by providing a permanent shunt path for currents from one coil to another where arcing has previously occurred. The failure voltage can be estimated by the wire diameter (i.e. gauge) used in windings. The failure voltage is

$$V_f \cong D_s \cdot T \qquad (5.11)$$

where D_s is the dielectric strength of the insulation (V/in) and T is the insulation thickness (in). The insulation thickness can be estimated from Table 5.11. The dielectric strengths for plastics and enamels range from 20-750 kV/in. Some measured and predicted arcing voltages are shown in Table 5.12. The failure current is

$$I_f \cong V_f / (2\pi fL) \qquad (5.12)$$

where L is the inductance and f is the frequency of the damped sine pulse.

It should be noted that the pulse breakdown voltage of inductors and transformers can be less than the DC voltage rating. This is because DC voltage ratings are determined from the maximum current that can flow through the device which will not cause melting of the wires. Pulsed voltages can cause breakdown of the dielectric between coils. Thus, the breakdown voltage/current of the inductor or transformer should be taken to be the lesser of the two voltage/current ratings.

5.2.5 SUPERSAP2

The previous sections showed techniques for estimating device damage constants from the manufacturers' specification sheets. SUPERSAP2 is a damage constant data base containing experimental failure data on over 86,000 devices including diodes, transistors, linear ICs, digital ICs, and passive components. The use of SUPERSAP2 is described in AFWL-TR-75-70, Users Manual for SUPERSAP2. Even though SUPERSAP2 is not required for an interface susceptibility analysis, its use is highly recommended because its damage constants based on experimental data are more accurate than the constants calculated from device parameters. The damage constants which are analytically derived (indicated with C.W. under DATA heading) can also be used and derated accordingly.

5.3 Device Damage Analysis

A current or voltage transient injected on the equipment interface pins eventually distributes among the circuit elements in most circuits. Thus only a fraction of the interface transient pulse will appear on some circuit elements. Division of the transient pulse among the circuit elements can and usually does become complex. For this reason, careful documentation of the various current paths through the circuit are important for a thorough circuit susceptibility analysis.

Most of this section deals with determining whether or not existing circuitry needs to be hardened. That is, this section shows how to use circuit analysis techniques to extrapolate component terminal levels to interface pin levels. If the extrapolated value is less than the pin level, the component will be damaged.

Table 5.11 Dielectric Thickness Around Solid Copper Wire [5.27]

AWG	Diameter over Bare, in			Insulation Additions		Diameter over Insulation	
	Minimum	Nominal	Maximum	Minimum	Maximum	Minimum	Maximum
4	0.2025	0.2043	0.2053	0.0037	0.0045	0.2060	0.2098
5	0.1801	0.1819	0.1828	0.0036	0.0044	0.1837	0.1872
6	0.1604	0.1620	0.1628	0.0035	0.0043	0.1639	0.1671
7	0.1429	0.1443	0.1450	0.0034	0.0041	0.1463	0.1491
8	0.1272	0.1285	0.1292	0.0033	0.0040	0.1305	0.1332
9	0.1133	0.1144	0.1150	0.0032	0.0039	0.1165	0.1189
10	0.1009	0.1019	0.1024	0.0031	0.0037	0.1040	0.1061
11	0.0898	0.0907	0.0912	0.0030	0.0036	0.0928	0.0948
12	0.0800	0.0808	0.0812	0.0029	0.0035	0.0829	0.0847
13	0.0713	0.0720	0.0724	0.0028	0.0033	0.0741	0.0757
14	0.0635	0.0641	0.0644	0.0032	0.0038	0.0667	0.0682
15	0.0565	0.0571	0.0574	0.0030	0.0035	0.0595	0.0609
16	0.0503	0.0508	0.0511	0.0029	0.0034	0.0532	0.0545
17	0.0448	0.0453	0.0455	0.0028	0.0033	0.0476	0.0488
18	0.0399	0.0403	0.0405	0.0026	0.0032	0.0425	0.0437
19	0.0355	0.0359	0.0361	0.0025	0.0030	0.0380	0.0391
20	0.0317	0.0320	0.0322	0.0023	0.0029	0.0340	0.0351
21	0.0282	0.0285	0.0286	0.0022	0.0028	0.0302	0.0314
22	0.0250	0.0253	0.0254	0.0021	0.0027	0.0271	0.0281
23	0.0224	0.0226	0.0227	0.0020	0.0026	0.0244	0.0253
24	0.0199	0.0201	0.0202	0.0019	0.0025	0.0215	0.0227
25	0.0177	0.0179	0.0180	0.0018	0.0023	0.0195	0.0203
26	0.0157	0.0159	0.0160	0.0017	0.0022	0.0174	0.0182
27	0.0141	0.0142	0.0143	0.0016	0.0021	0.0157	0.0164
28	0.0125	0.0126	0.0127	0.0016	0.0020	0.0141	0.0147
29	0.0112	0.0113	0.0114	0.0015	0.0019	0.0127	0.0133
30	0.0099	0.0100	0.0101	0.0014	0.0018	0.0113	0.0119
31	0.0088	0.0089	0.0090	0.0013	0.0018	0.0101	0.0108
32	0.0079	0.0080	0.0081	0.0012	0.0017	0.0091	0.0095
33	0.0070	0.0071	0.0072	0.0011	0.0016	0.0081	0.0088
34	0.0062	0.0063	0.0064	0.0010	0.0014	0.0072	0.0078
35	0.0055	0.0056	0.0057	0.0009	0.0013	0.0064	0.0070
36	0.0049	0.0050	0.0051	0.0008	0.0012	0.0057	0.0063
37	0.0044	0.0045	0.0046	0.0008	0.0011	0.0052	0.0057
38	0.0039	0.0040	0.0041	0.0007	0.0010	0.0046	0.0051
39	0.0034	0.0035	0.0036	0.0006	0.0009	0.0040	0.0045
40	0.0030	0.0031	0.0032	0.0006	0.0008	0.0036	0.0040
41	0.0027	0.0028	0.0029	0.0005	0.0007	0.0032	0.0036
42	0.0024	0.0025	0.0026	0.0004	0.0006	0.0028	0.0032

Table 5.12 Dielectric Strength of Inductor Insulation [5.15]

Device	TH Insulation thickness (cm)	$\widetilde{DS}$ Dielectric strength V/cm	Turns	Predicted ARC voltage	Minimum ARC voltage
IDIT-309	1.27×10^{-3}	1.39×10^{5}	77	1358	2000
VTH-1.0	4.32×10^{-2}	1.39×10^{5}	10	6000	No Arc
871-3010	4.32×10^{-2}	1.39×10^{5}	15	9000	No Arc
WEE-1000	5.08×10^{-4}	1.43×10^{4}	1,575	11450	No Arc
WEE-100,000	5.08×10^{-4}	1.43×10^{4}	1,575	11450	1700

Further information on circuit analysis is found in References 5.15 through 5.18, and examples are in Section 5.4.

5.3.1 Analysis Organization and Documentation

The analysis starts with the block diagram of the system to be analyzed. Figure 5.12 shows a sample block diagram, with equipment and cable connection designations. Next, each block in the diagram is labelled critical or non-critical, i.e., does failure of the block cause mission-critical operations to fail. All non-critical blocks require no further analysis. For each remaining block in the diagram a table of all cable connector jacks with a list of all their pins is made (See Table 5.13). The threat for each pin and each cable is added to the list. These threats are given in Section 2.4.3. Data necessary for the interface susceptibility analysis is then collected. This includes system schematics, wiring lists, and manufacturers' specification sheets for the components in the system.

5.3.2 Screening

In order to reduce the amount of failure level calculations required, screening is performed. Screening consists of the removal of circuits thought to contain only hard components from further analysis. Hard components usually consist of inductors, motors, relays, transformers, light bulbs, and mechanical switches. Hard components may also include all other components with voltage or current ratings greater than the threat levels. As circuits and components are removed from further analysis, the pins that are connected only to these circuits and components are documented on the lists as hard, and the reasons for these decisions are stated on the list. If there is any uncertainty about the vulnerability of a component, assume it is soft and perform further analysis.

The next step is to eliminate from further analysis vulnerable devices protected by large series impedances or large shunt admittances. An example is shown in Figure 5.13. Even though the capacitor only requires 10 V for failure, over six thousand volts must be on the pin to create this voltage on the capacitor. Also note the amount of documentation and information contained on this single sheet of analysis. At the end of the screening all hard component types, and soft devices protected by a large series impedance or shunt admittance have been removed from further analysis. A detailed example of screening is shown in Section 5.4.

5.3.3 Detailed Analysis

Further analysis is required on all components not previously defined as hard which usually consist of semiconductor devices, resistors, or capacitors connected directly to a pin. The two main methods used for a detailed analysis are hand analysis and computer circuit code analysis.

Hand analysis is shown in Figure 5.13. It consists of applying Kirchoff's current and voltage laws to a simplified circuit containing the unanalized component. Several different elements can be included in the model but as complexity grows, computer solutions become necessary.

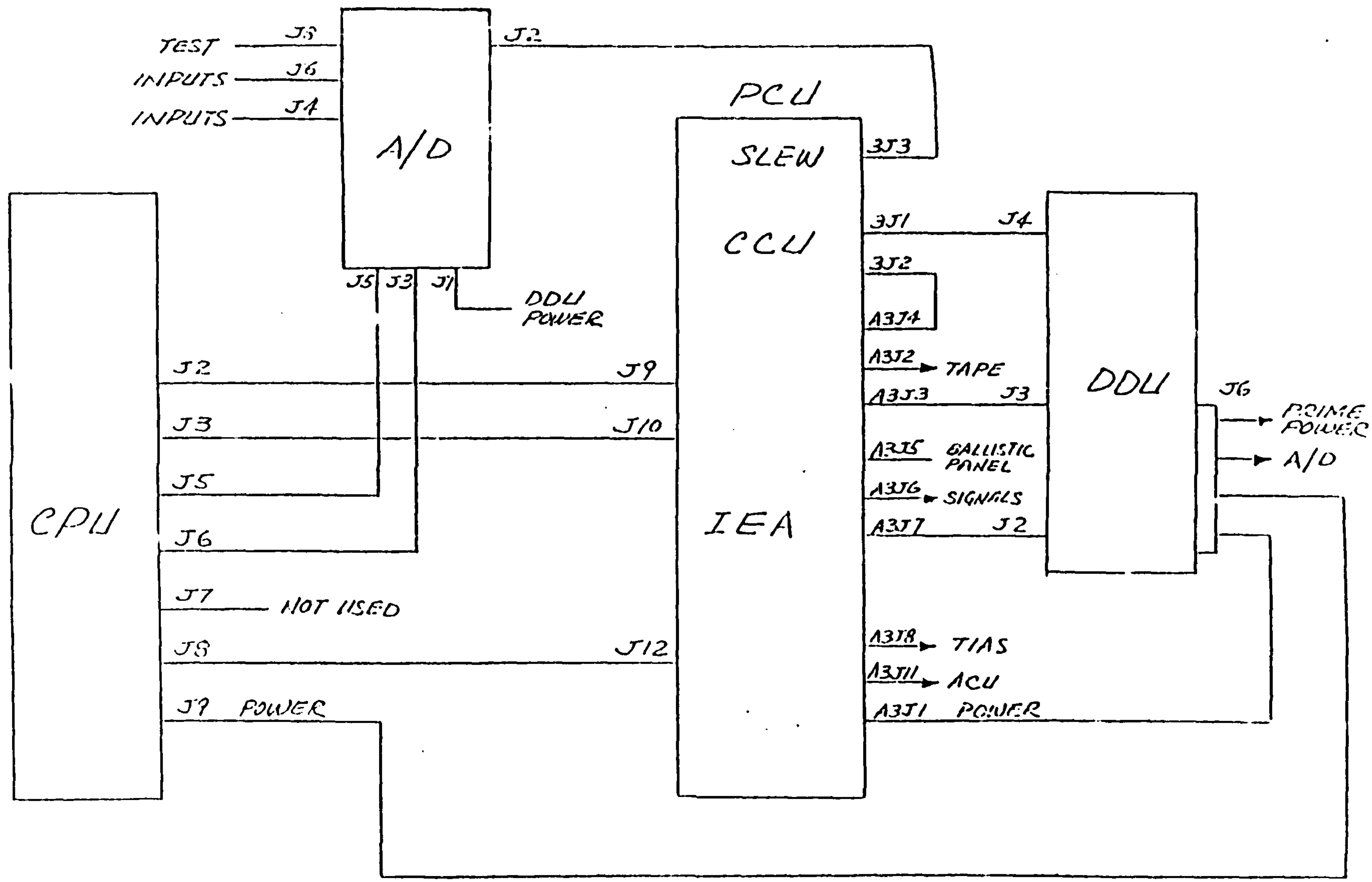
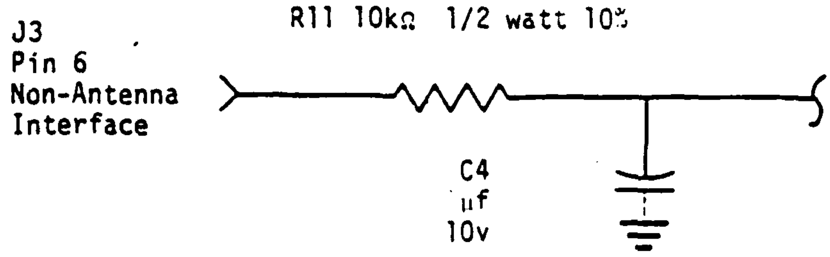


Figure 5.12 Sample Block Diagram (Ballistic Computer Set) [5.2]

Table 5.13 Sample Master List [5.16]

CONN.	SYS:	BOX:				ENG:
PINS	SCHEMATIC	COMPONENT REF. DES.	PART TYPE	FAILS SPEC.	REF. CALC.	COMMENTS

System: AN/ALT-31	Jack: J3	Pin: 6	Analyst: R. Cook



For C4 $V_f = 10_v$

Will have lowest failure current at lowest frequency

Lowest frequency is $10kH^z$ from Handbook Figure 2.5a

$I_f = C4 x 2\pi f V_f = 1.0E\text{-}6 x 2\pi 1.0E4 = 628ma$

Failure current at Pin 6 = 628ma

Threat current from Figure 2.5a@$10kH_z$=200ma

Failure voltage at Pin 6 = $I_f x(R11 + \frac{1}{2\pi f C4})$ = 6.3Kv

Threat voltage from Figure 2.5a @$10kH^z$=20v

Safety Margins: SM_I = 10db SM_V = 50db

Reference: T.O. 1243-18C4,p27	Date: 4/29/81

Figure 5.13 Sample Analysis Sheet

Typical computer circuit codes that can be used for an interface susceptibility analysis are HANAP [5.19], NET-2 [5.20], and SCEPTRE [5.21]. HANAP is a frequency domain code, SCEPTRE is a time domain code, and NET-2 can solve both frequency and time-domain problems. Frequency-domain codes are useful when the threat is specified for different frequencies and time-domain codes are useful when the threat is a function of time. Time-domain codes are also used when the circuit of interest contains non-linear devices, such as zener diodes, between the threat and component of interest. Examples of the use of these codes are given in Section 5.4.

5.3.4 Hardness Margins

Once each soft component failure voltage and current extrapolated to the interface pin have been determined, the comparison of these levels to the threat level determines the hardness margins. The hardness margins provide a ranking of the vulnerability of different pins. The hardness margins are usually given in dB as:

$$\text{Hardness margin (dB)} = 20 \log \frac{I_p}{I_t} \text{ or } 20 \log \frac{V_p}{V_t}, \qquad (5.13)$$

whichever is smaller. The p subscript refers to pin failure voltage or current, and the subscript t refers to the threat voltage or current. In Figure 5.13, the current hardness margin of 10 dB is determined by:

$$SM_I = 20 \log \frac{I_p}{I_t} = 20 \log \frac{628\text{ma}}{200\text{ma}} = 9.94 \text{ dB} \qquad (5.14)$$

The voltage safety margin is determined similarly. Because the damage constants are approximate and the analysis does not cover every detail of the circuits. the analysis should be derated by requiring a safety margin of at least 10 dB.

5.4 Examples of Analysis

The previous sections of this chapter described the methods of performing an interface susceptibility analysis. This section demonstrates how to implement these techniques by examples.

5.4.1 Example 1

This example demonstrates screening techniques. Figure 5.14 shows the schematic of a subsystem. Each pin of this subsystem (pins 1 through 12) should already on the list of pins for this connector. Pins 5, 11 and 12 have no connection to them. Pin 7 connects to chassis ground. Pin 4 connects to a one megaohm series resistor at the connector which is not shown on this diagram. A voltage divider is therefore formed between the one megaohm resistor and R460, which is 3300 Ω. The failure voltage at the connector pin is therefore:

$$V_f = \frac{1M\Omega + 3300\ \Omega}{3300\ \Omega} V_{BE} = 304\ V_{BE}, \qquad (5.15)$$

where V_{BE} is the base-emitter voltage of Q453. The base-emitter junction of Q453. which is a 2N3393, is rated at 5 vdc. Therefore, V_f = 1520v, which is higher than the one thousand volt non-antenna interface pin spec. Pin 4 should be listed

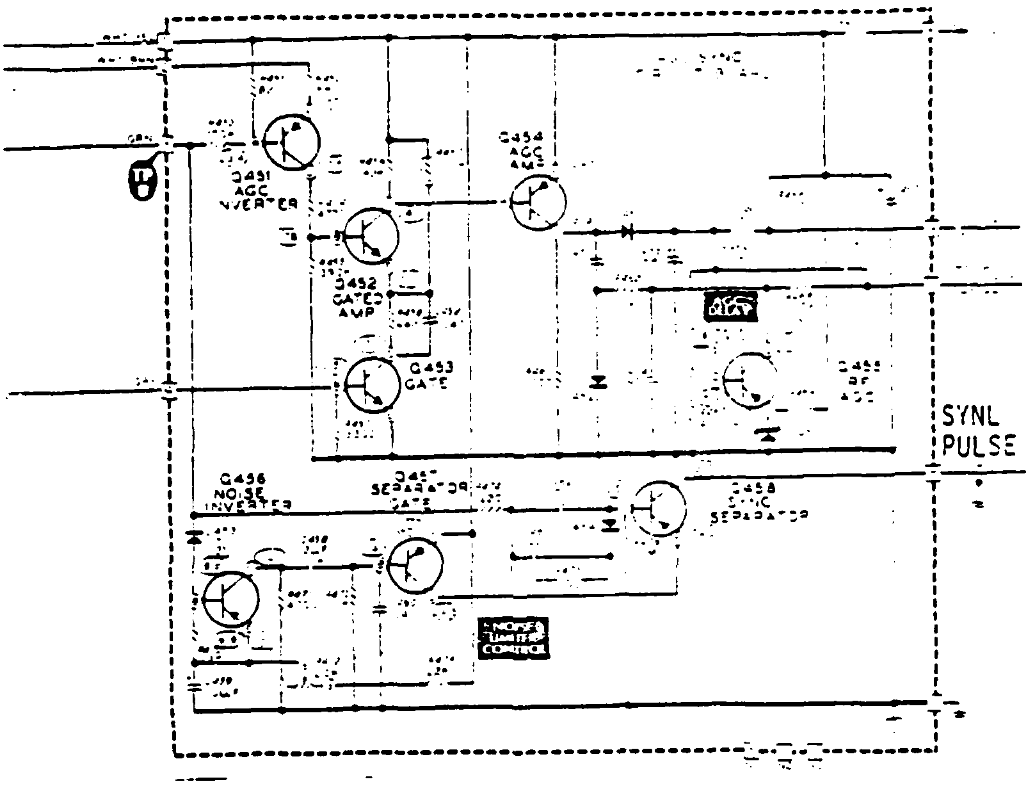


Figure 5.14 Subsystem Schematic for Examples 1 and 2

as hard, with a voltage safety margin of:

$$SN_V = 20 \log \frac{1520 \text{ v}}{1000 \text{ v}} = 2 \text{ dB} \tag{5.16}$$

which is not a very large safety margin. This pin should therefore be assumed soft, and a more detailed analysis is made. At pin 3, D453, Q456, Q457, Q458, D454, Q451, Q452, Q453, Q454, D451, and D452 are assumed soft and require further analysis. At pin 2, the same devices are assumed soft. At pins 1, 8, 9 and 10 the same devices in addition to ZD451 and Q455 are assumed soft. At pin 6, Q458, D454, D453, Q456, and Q457 are assumed soft. Note that screening on the this subsystem did not eliminate many pins from analysis. This is due to the large threat levels that exist. Detailed analysis will probably show that many of these are safe due to the number of components in series.

5.4.2 Example 2

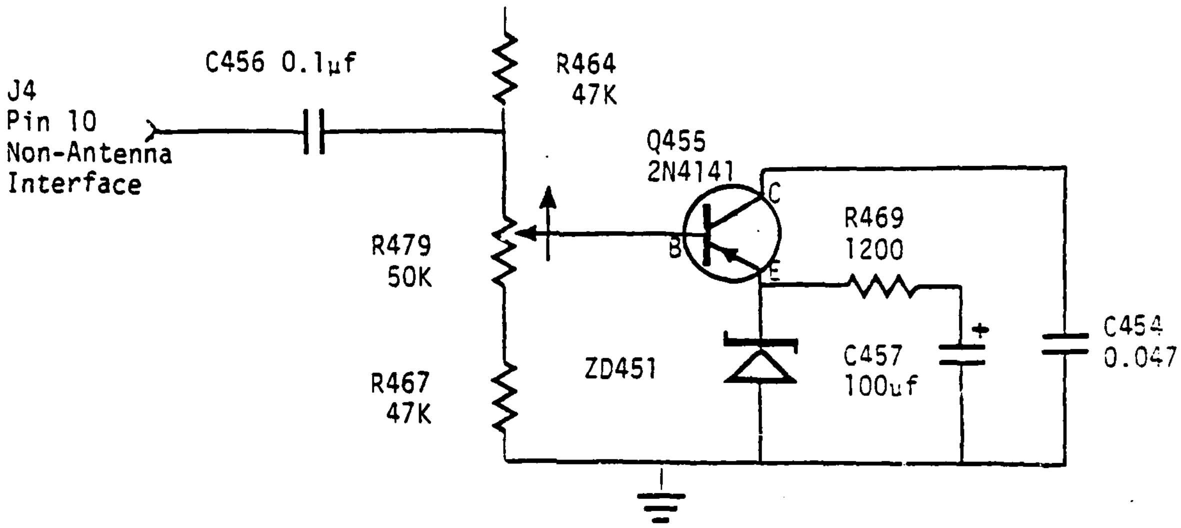
This example continues the previous problem with a more detailed analysis of some of the pins. The example starts at pin 10.

The first analysis is for Q455, which is a 2N4121. The lowest impedance path from pin 10 is through C456, R479, and the B-C junction of Q455 to ground. At 100 MHz, C456 can be neglected, and R479 can be assumed to be at the zero resistance position. Therefore, pin 10 is shorted directly to the B-C junction of Q455. ZD451 is a 9.1v reference zener diode, and Q455 is rated with BV_{EBO} = 5 vdc, and BV_{CBO} = 40 vdc. The equivalent circuit is shown in Figure 5.15. The analysis follows the transistor base-collector junction of Figure 5.8. The base-emitter junction of Q455, ZD451, resistors, capacitors, and other pins are analyzed similarly. At the conclusion of the detailed analysis, the lowest safety margins at each pin should be listed on a masterlist, along with the most susceptible component description.

5.4.3 Example 3

This example demonstrates the use of a computer circuit code (HANAP) to determine pin threshold levels for an IF amplifier diode. The diode is modeled with $R_S = 10_r$, $V_{BC} = 10_V$, and $K = 10^{-3}$. Figure 5.16 shows the representation of the circuit. All units are in ohms, farads, henries, amps and volts. The failure model of diodes is a primary feature of HANAP. The current source of the input is a dummy source required by HANAP. The input to the HANAP program is shown in Figure 5.17. The DATA card says there are 5 nodes excluding ground, and 25 frequency points each in 4 decades starting at 10 kHz. The next 9 cards describe the circuit elements, nodes they are connected to, and values. The other cards describe the diode, and the type of failure calculation. Figure 5.18 and Figure 5.19 show the output of the program. The X represents threat currents or voltages, and the * represents the calculated pin failure voltage or current. It can be seen from the plots that the diode will fail by a large margin.

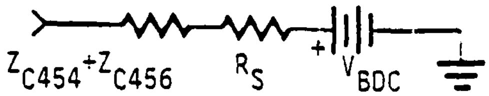
System: GR-900	Jack: J4	Pin: 10	Analyst: R. Cook



Base-Collector

@100MHz $Z_{C454} = \frac{1}{2\pi fC454} = 33.9m\Omega$ $Z_{C456} = \frac{1}{2\pi fC456} = 15.9m\Omega$

Equivalent Circuit:



$N_D=4.49\times10^{18}(BV_{CBO})^{-1.5}=1.775\times10^{16}$ $V_{BDC}=4.07\times10^{12}(N_D)^{-0.67}=52.8v$

$C_{SC}=2.48\times10^{25}(N_D)^{-1.8}=1.399\times10^{-4}$ $C_{BLK}=3.61\times10^{10}(N_D)^{-0.81}=2.427\times10^{-3}$

$J_F=8.26\times10^{-11}(N_D)^{0.88}=1.645\times10^{4}$ $AREA=2.72\times10^{-3}(I_{MAX})^{0.62}=1.003\times10^{-3}$

Safety Margins: SM_I=37 db SM_V=8 db

Reference: Schematic 183-A401	Date: 4/29/81

Figure 5.15 Detailed Analysis Example 2

System: GR-900	Jack: J4	Pin: 10	Analyst: R. Cook

$R_{BLK}=C_{BLK}/AREA=2.48\Omega \quad R_{SC}=C_{SC}/AREA=0.14\Omega$

$R_S=R_{BLK}+R_{SC}=2.62\Omega$

$I_{F_{100ns}}=J_F\ AREA=16.5a$

$V_{F_{100ns}}=V_{BDC}+I_{F_{100ns}}(Rs)=96v$

$K=(I_{F_{100ns}} \times V_{F_{100ns}})\ (100 \times 10^{-9})^{1/2} = 0.501$

$I_{FP}=I_F\left(\frac{tp}{100x10^{-9}}\right)^{-1/2}=16.5a\left(\frac{1/(1.8x100x10^6)}{100x10^{-9}}\right)^{-1/2}=70a$

$V_{FP}=V_{BDC}+I_{FP}(Rs)=236v$

I_f @ pin 10 = I_{FP} = 70a

V_f @ pin 10 = $I_f \times (Z_{C454}+Z_{C456})+V_{FP}=239v$

$SM_I = 20 \log \frac{70a}{1a} = 37db \quad SM_V = 20 \log \frac{239v}{100v} = 8\ db$

Safety Margins: SM_I=37 db SM_V=8 db

Reference: Schematic 183-4401	Date: 4/29/81

Figure 5.15 Detailed Analysis Example 2 (Concluded)

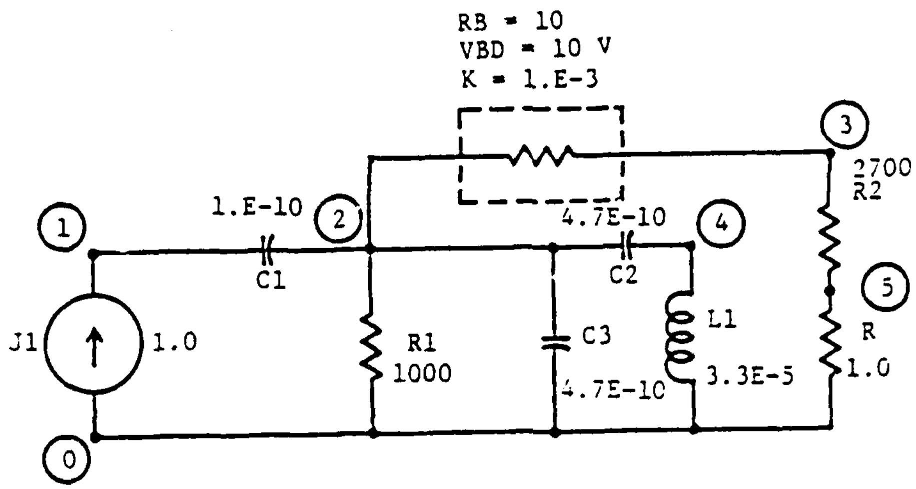


Figure 5.16 IF Amplifier [5.19]

```
       BURNOUT OF IF AMP
DATA         5    25                 1.E4     4
J1           0    1        1.0
C1           1    2         1.0     E-10
C2           2    4        4.7      E-10
L1           4    0         3.3     E-05
R1           2    0      1000.
C3           2    0      4.7        E-10
RB           2    3                  10.
R2           3    5                2700.
R            0    5                   1.
OUTPUT       1                   1.E-03   1                         .5 3
VBD                      10.
A                                     1.
END
```

Figure 5.17 Input Deck [5.19]

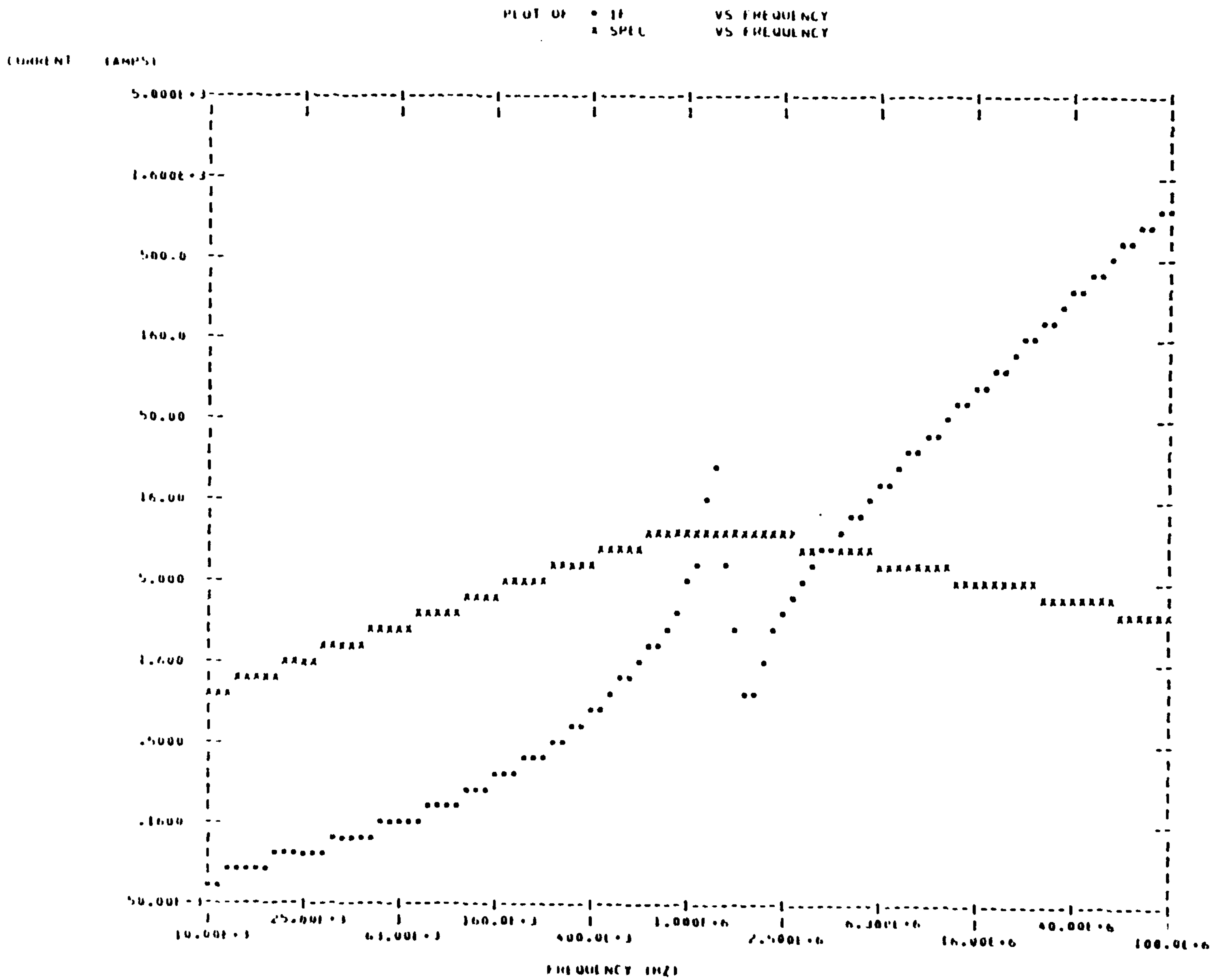


Figure 5.18 Output of Example 3 [5.19]

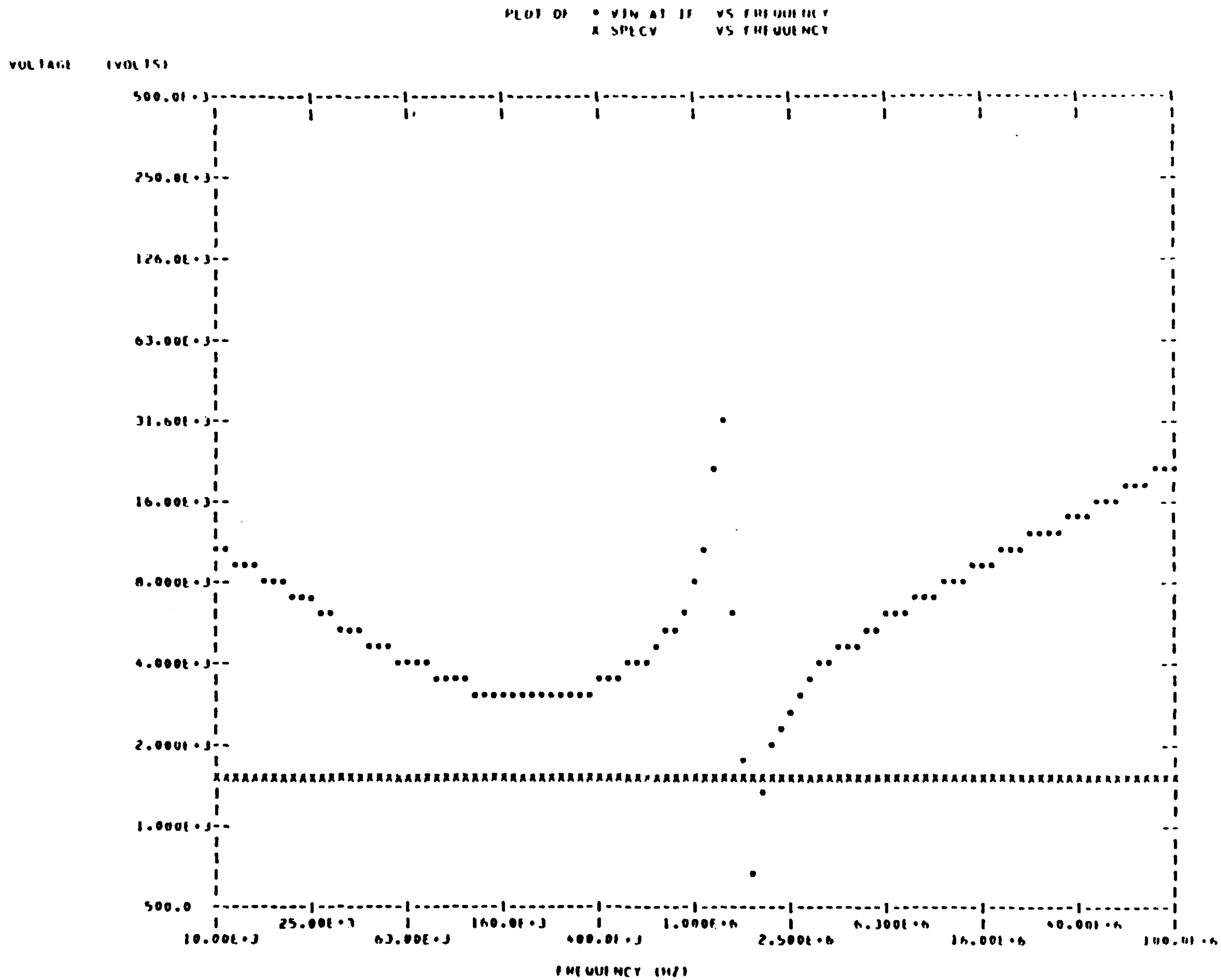


Figure 5.19 Output of Example 3 [5.19]

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CHAPTER 6

TERMINAL PROTECTIVE DEVICES

6.0 Executive Summary

Chapter 6 discusses components used to protect equipment at equipment interfaces (terminals). Techniques used for choosing and installing these terminal protection devices (TPDs) are also presented. However, hardening equipment at the interfaces using TPDs can degrade equipment performance.

Equipment protected by TPDs can be substantially degraded on terminals operating at high frequencies. Consequently, some test measures used for evaluating system degradation after installing TPDs on high frequency equipment is presented in detail.

6.1 Background

Transient suppression techniques reduce the effects of unwanted signals by altering their characteristics (magnitude, rise time, frequency and energy content, etc.) without altering the desired signal. Transient suppression involves the use of terminal protection devices (TPDs) to create low impedance shunt paths and/or high impedance series paths for the unwanted transients. TPDs are both linear or nonlinear devices. The former includes resistors, inductors, capacitors, and delay lines which compose filters. The latter includes spark gaps, varistors, semiconductor diodes, and switching devices.

In order to protect equipment by the application of TPDs, it is necessary to know some specific information about the equipment's ambient operating conditions as well as its vulnerability to EMP-induced transients. The equipment vulnerability can be assessed by performing a circuit susceptibility analysis (Chapter 5) and upset analysis (Chapter 7). This establishes the equipment damage/upset threshold (i.e. peak current, peak voltage, peak energy, etc. that the equipment can withstand without damage and/or upset). The equipment damage threshold determines the amount of transient suppression required for hardening (i.e. TPD clamping voltage, power rating, etc.) required for hardening at the equipment interface. The equipment's ambient operating conditions determine the allowable insertion loss of the TPD such that normal operation of the equipment is maintained. Thus, selection of the TPD is dependent upon insertion loss of the TPD as well as the equipment damage/upset threshold.

In the remainder of this chapter, the TPD characteristics are presented and the use of TPDs as transient suppressors. Section 6.2 discusses the general use and application of filters. Section 6.3 discusses the general use of nonlinear devices. Section 6.4 presents use of protective devices at non-antenna interfaces. Section 6.5 presents use of TPDs at antenna interfaces.

6.2 Linear TPDs (Filters)

6.2.1 Introduction

Filters are useful for reducing EMP interference when the normal signal frequency spectrum is different than that of the EMP frequency spectrum. Here the EMP frequency spectrum is that defined in Sections 2.4.3 through 2.4.5. An

effective filter must meet some or all of the following requirements [6.2]:

a. Have extremely high or low input impedance relative to the source in the frequency rejection (stop) band.

b. Have high loss to frequencies in the stop band.

c. Have high DC current carrying capability without changing stop band characteristics.

d. Prevent cross coupling.

e. Prevent arcing across its elements.

f. Have low DC resistance (primarily DC powerline considerations).

g. Have high reliability.

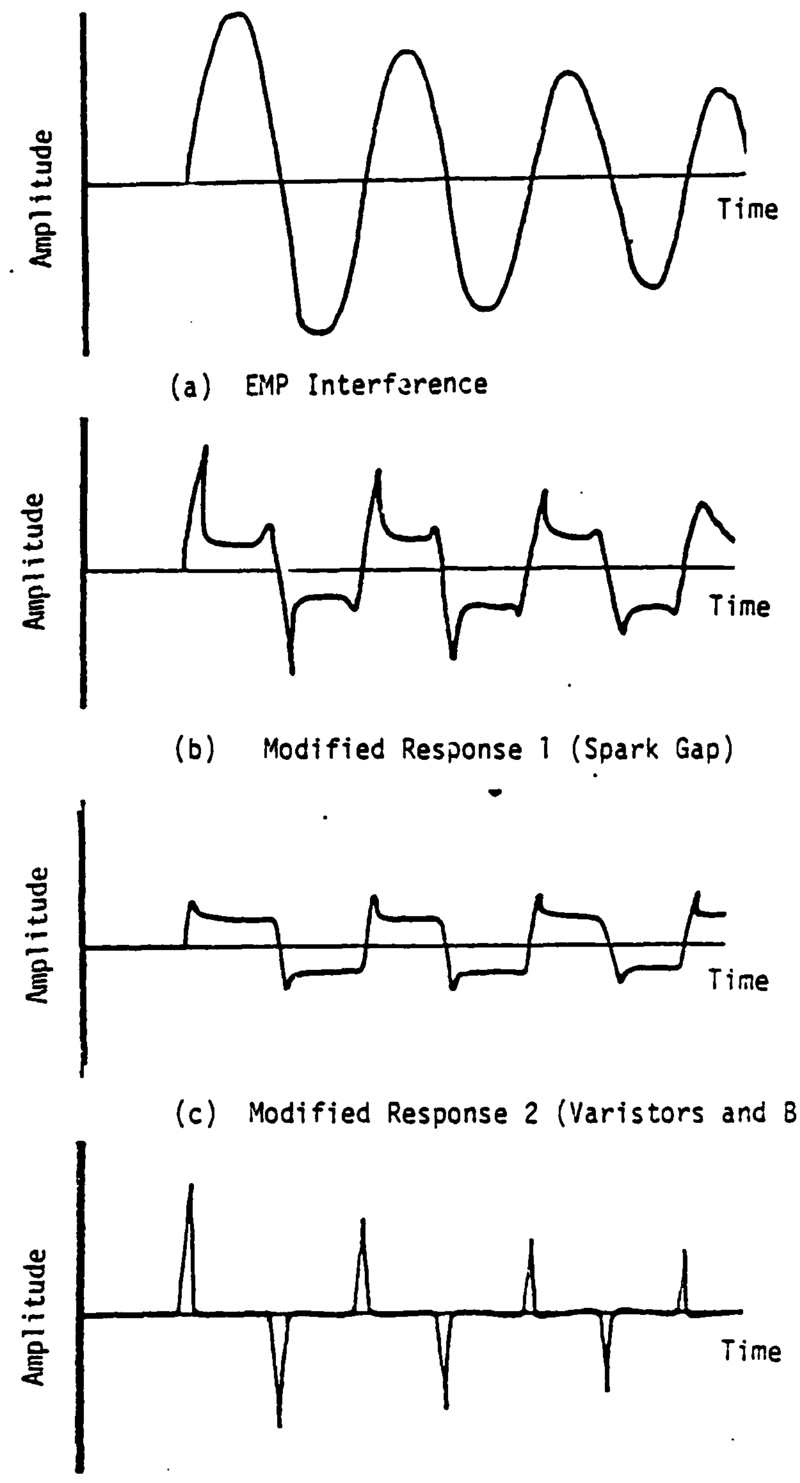
Often filters are used in conjunction with nonlinear limiting devices. Because a nonlinear limiting device can change the EMP signal frequency content, the filter design must account for this change in frequency [6.3]. Figure 6.1 illustrates the effects of a nonlinear limiting device. Part (a) shows a normal EMP damped sinusoid signal, and parts (b), (c), and (d) show the responses of nonlinear devices to the signal. In all three cases, high frequency components which affect filter design are introduced.

In this handbook, filters will be classified as reflective, dissipative, filter pin connectors, and other types.

6.2.2 Reflective Filters

For reflective filters, signals outside the passband are reflected and are not absorbed by the filter. A disadvantage of reflective filters is that the EMP energy must be dissipated elsewhere in the system.

Two basic types of discrete component reflective filters, the π-filter and the T-filter, are illustrated in Figures 6.2 and 6.3. The low-pass π-filters may not adequately protect against EMP because high voltages can develop across the input capacitor and cause degradation or failure if the capacitor resonates with the source [6.2]. Because T-filters are not susceptible to these high voltages, they can be used for EMP hardening. However, with a T-filter, more power can possibly be delivered to the load. In Figure 6.4, if the source and load capacitance resonate with inductances L_1 and L_2, respectively, the voltage across R_L is greater than it would be without the filter. The quarter wave shunt (Figure 6.5) is a reflective filter which consists of a transmission line whose length is one-fourth of the wavelength of the normal signal which is shorted at one end, and which is connected in parallel with the signal transmission line at the other end. The shunt, which acts as a quarter-wave transformer [6.5] and appears as an infinite impedance at the desired signal frequency, appears as a short circuit to all other frequencies and thus functions as a band pass filter. The out-of-band energy is reflected and must be dissipated elsewhere in the system. The quarter wave shunt has a risetime equal to the time it takes for a pulse to travel the length of the shunt and be reflected back to its termination on the original transmission line. Because the quarter wave shunt must be one-fourth wavelength long at the normal frequency, it is useful for high frequency systems such as VHF and higher frequency antenna systems.



(a) EMP Interference

(b) Modified Response 1 (Spark Gap)

(c) Modified Response 2 (Varistors and Bipolar Zeners)

(d) Modified Response 3 (Switching Devices)

Figure 6.1 EMP Interference with and without Nonlinear Device Interaction [6.3]

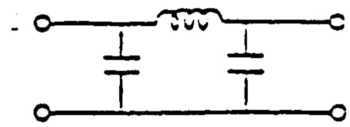


Figure 6.2 Low-Pass -Filter [6.2]

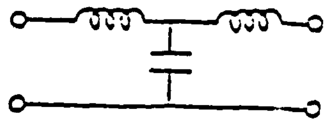


Figure 6.3 Low-Pass T-Filter [6.2]

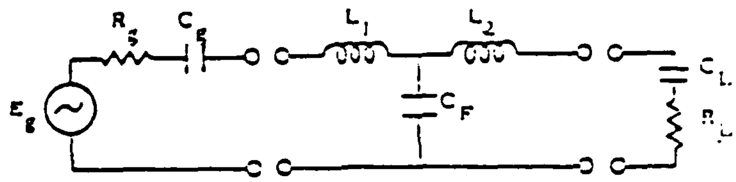


Figure 6.4 Lossless T-Section Filter [6.2]

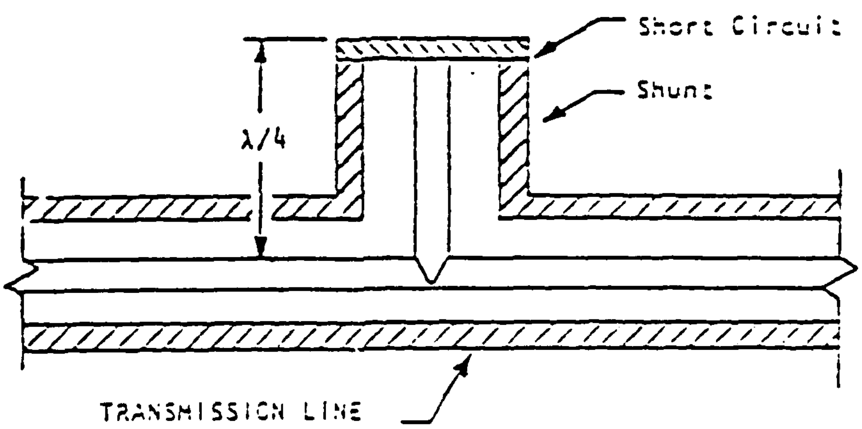


Figure 6.5 Cross Section of Quarter Wave Shunt [6.5]

6.2.3 Dissipative Filters

For dissipating filters, the primary means of filtering is by absorbing instead of by reflecting EMP signal energy. Dissipative filters allow the designer control over the location at which EMP energy is dissipated. For dissipative filters, lossy materials, such as ferrites, provide the means of energy dissipation. For lossy filters the source and load impedances are not as critical as in reflective filters. Figure 6.6 illustrates typical attenuations that may be obtained by lossy filters [6.6].

A ferrite bead, which is a small ferrite torroid whose equivalent circuit is a series RL circuit in the conductor around which it is placed, is used in one type of dissipative filter [6.4].

Figure 6.7 shows a ferrite core (bead) placed around a wire and the equivalent circuit. The resistance and reactance are functions of frequency. Figures 6.8 and 6.9 illustrate the variations of the resistive impedance and reactive impedance as a function of frequency for various types of cores.

An application of ferrite beads is shown in Figure 6.10, where the transfer impedance Z_{tr} as defined in the figure is measured as a function of frequency for five cores. The change in transfer impedance is not particularly significant because of the high load impedance (200 Ω). This suggests that ferrite beads are most effective in low-impedance circuits [6.4].

Sometimes more attenuation can be obtained by using many cores on a given conductor. However, this may result in an impedance reduction at certain frequencies, as illustrated in Figure 6.11. In this figure, 30 beads are more effective above 20 MHz than are 300 beads.

Core saturation at high currents, which should be considered in the use of ferrite beads, varies from material to material; therefore, manufacturer's data on individual materials must be consulted.

An effective way of nullifying the saturation effects of cores in a DC power line is illustrated in Figure 6.12. Here, ferrite torroids are installed in a 28-volt DC power line as EMP filters. The high-side and low-side windings are wound in opposite directions; thus the DC flux, which is reduced almost to zero, does not saturate the core. The coaxial capacitors and C_1 and C_2 short out the high frequency components. As noted in Figure 6.12, input and output leads should be separated to prevent arcing between them. In DC power circuits, the filter resistance is important, but because ferrites have such high permeabilities, only a few turns are needed and, therefore, filters can be made with large wire, which minimizes the resistance.

A standard low pass filter and a lossy low pass filter are compared in Figure 6.13. The lossy construction is also shown. The dips in the insertion loss frequency spectrum for the normal filter are eliminated by the lossy filter [6.7]. Figure 6.14 illustrates a tee filter, whose elements Z_1 and Z_2 could be either lossless inductors or ferrite beads.

6.2.4 Filter Pin Connectors

Reference 6.6 lists the following advantages of filter-pin connectors:

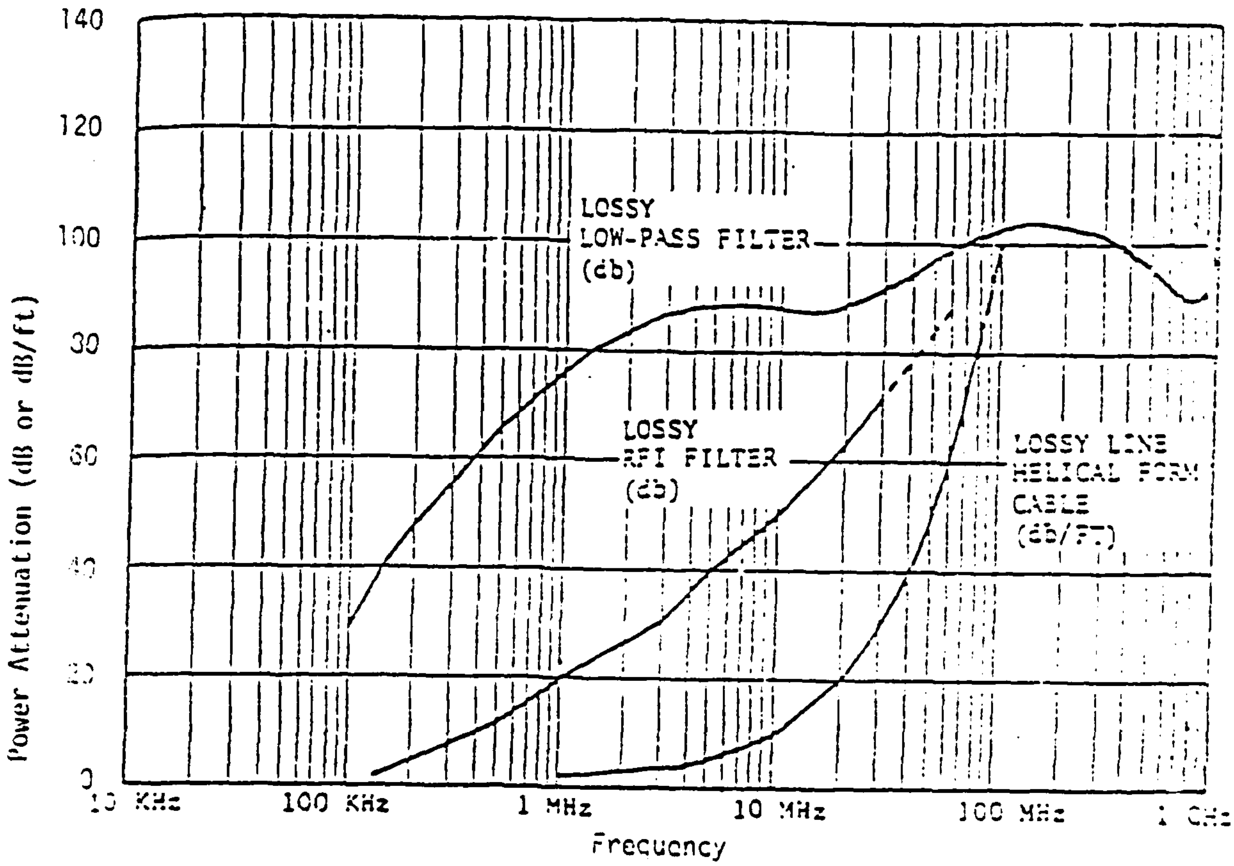


Figure 6.6 Examoles of Lossy Filter Characteristics [6.6]

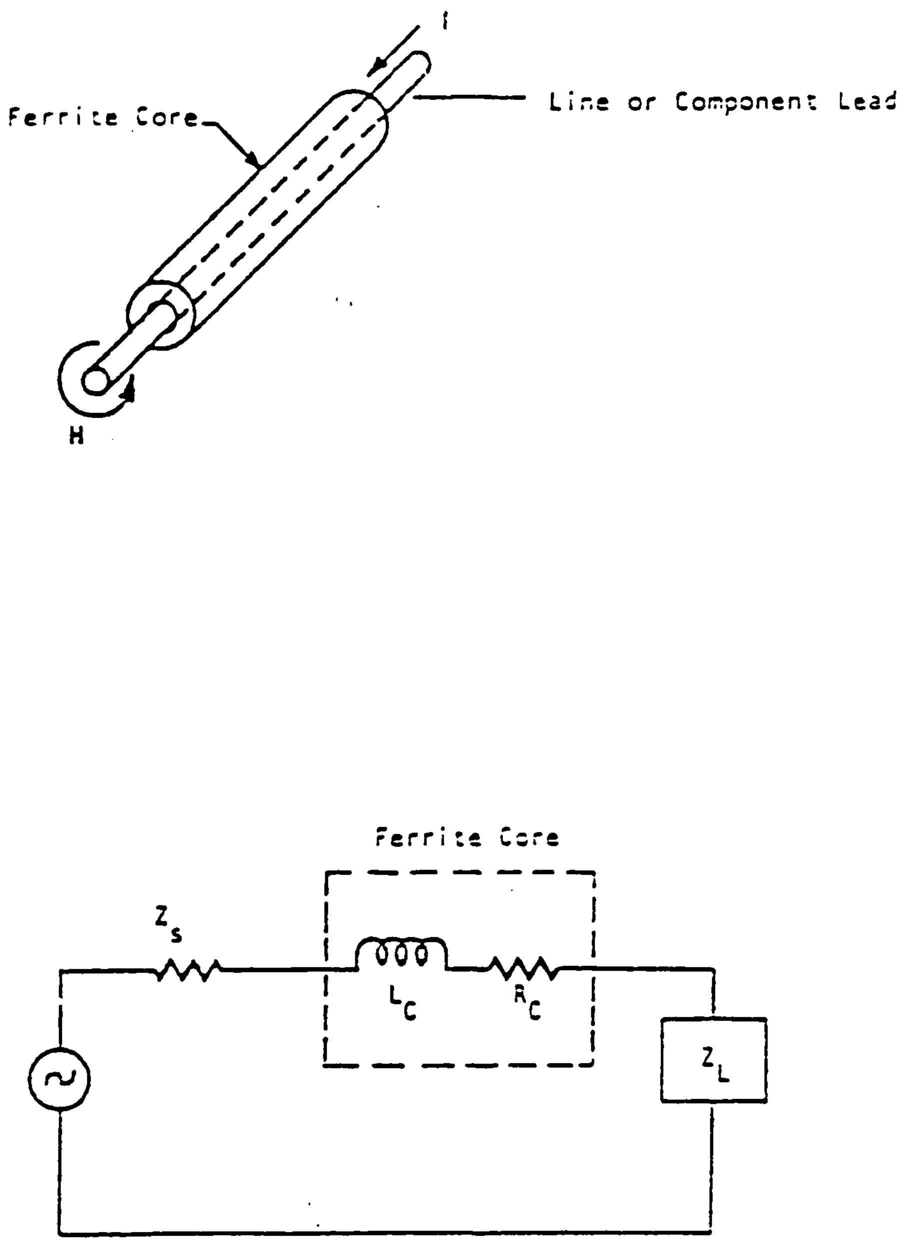
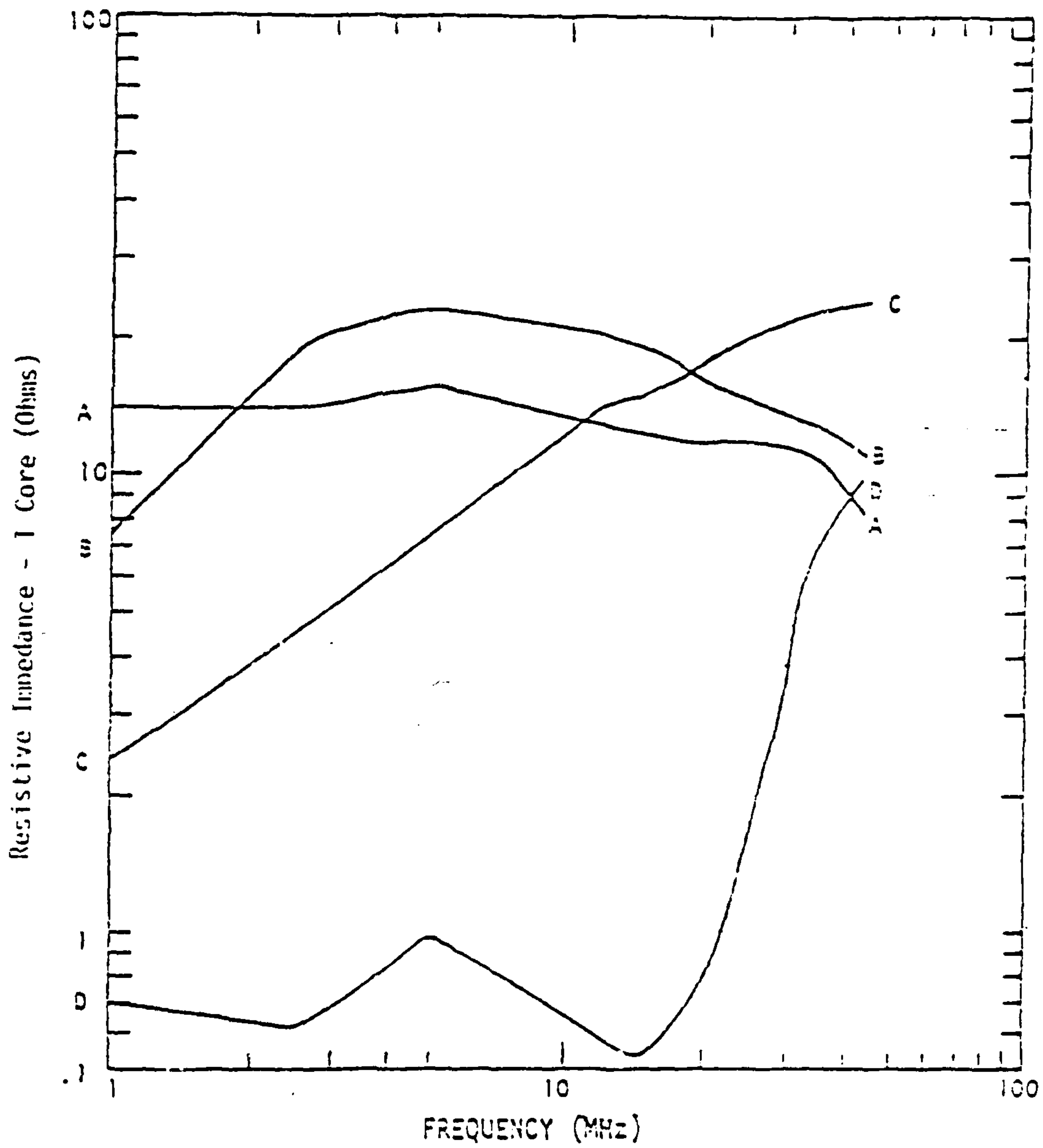


Figure 6.7 Ferrite Core and Equivalent Circuit [6.·]



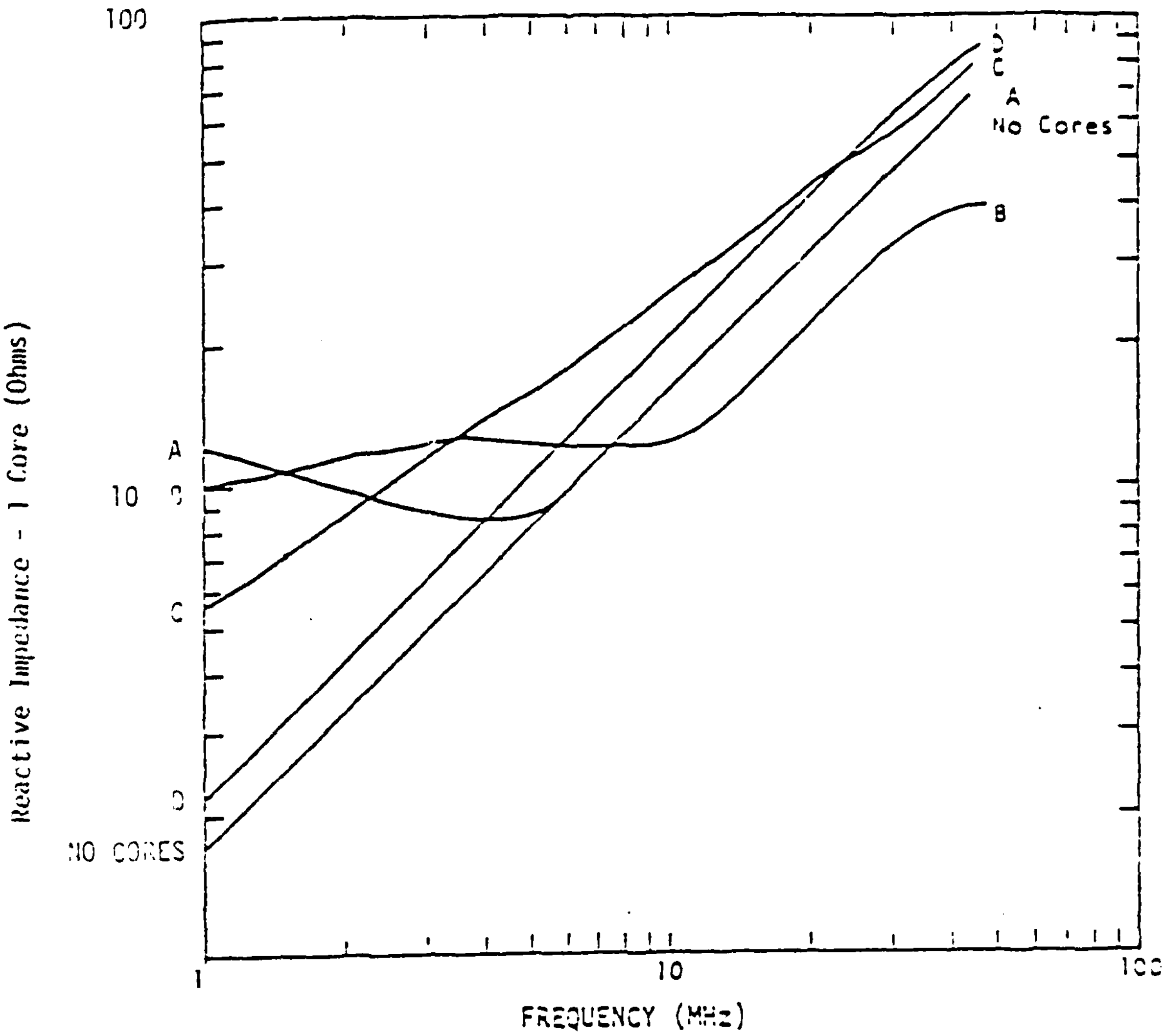
A - INDIANA GENERAL TYPE Q6

B - FERRONICS TYPE B

C - FERROXCUBE TYPE 4A6

D - INDIANA GENERAL TYPE Q1

Figure 6.8 Resistive Impedance per Core of Various Ferrite Cores [6.4]



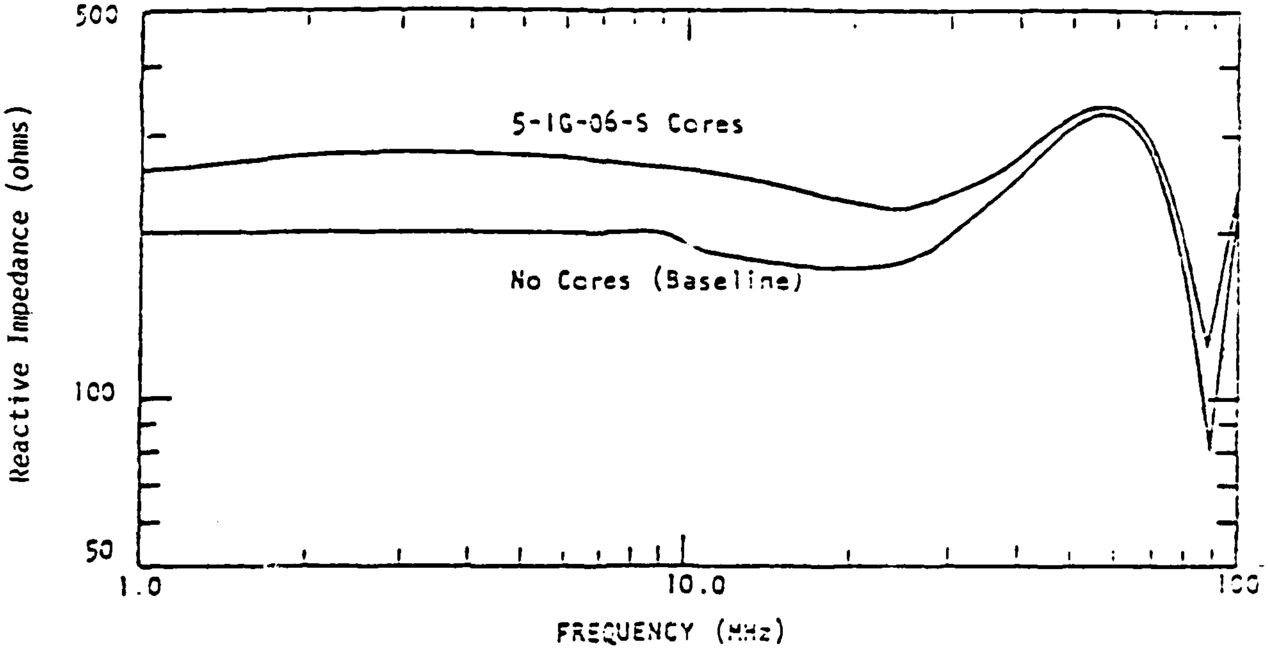
A - INDIANA GENERAL TYPE 06

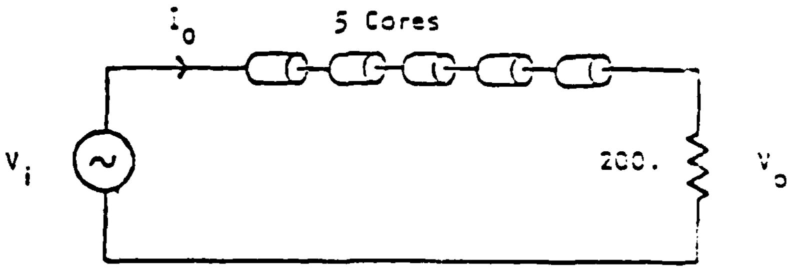
B - FERRONICS TYPE B

C - FERROXCUBE TYPE 4A6

D - INDIANA GENERAL TYPE Q1

Figure 6.9 Reactive Impedance Per Core for Various Ferrite Cores [6.4]





$$Z_{tr} = \frac{V_i}{I_o} = \frac{V_i(200)}{V_o}$$

Figure 6.10 Reactive Impedance and Test Circuit [6.4]

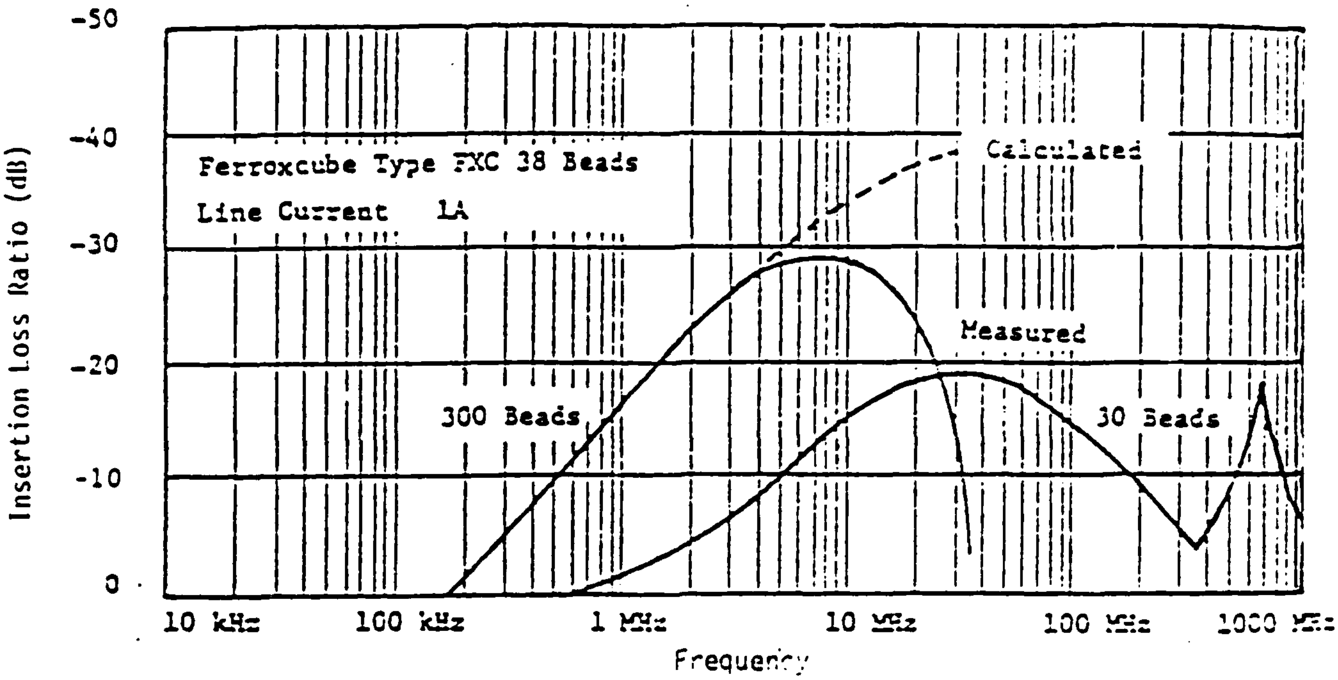


Figure 6.11 Insertion Loss Ratio of 30 Beads Strung on a Line is Very Frequency-Dependent [6.4]

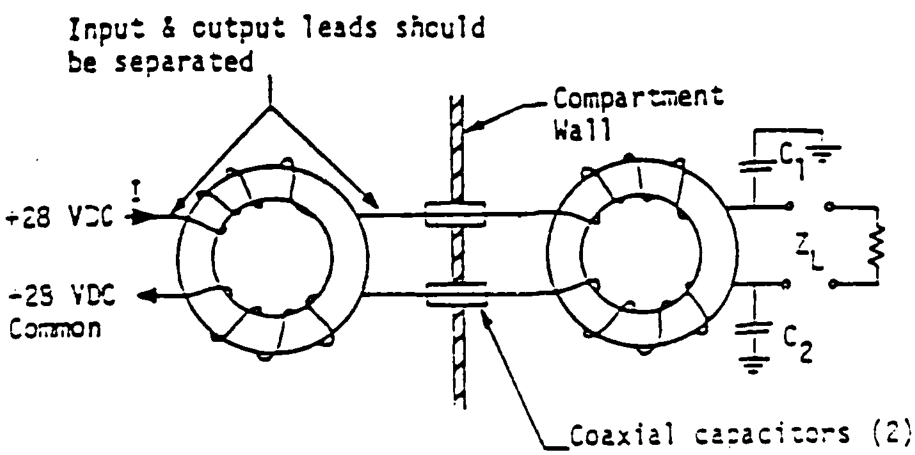
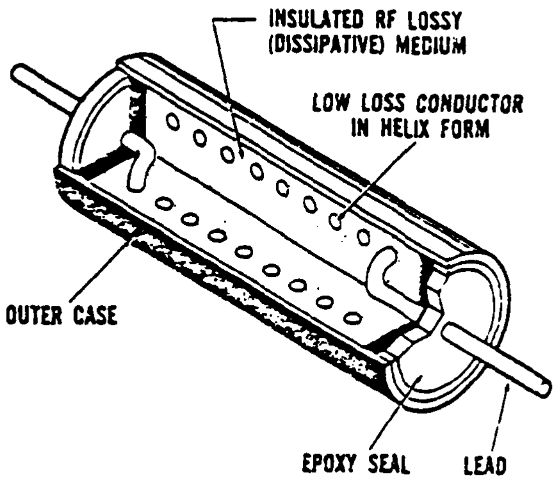


Figure 6.12 Ferrite Cores Designed to Nullify Effects of High DC Currents



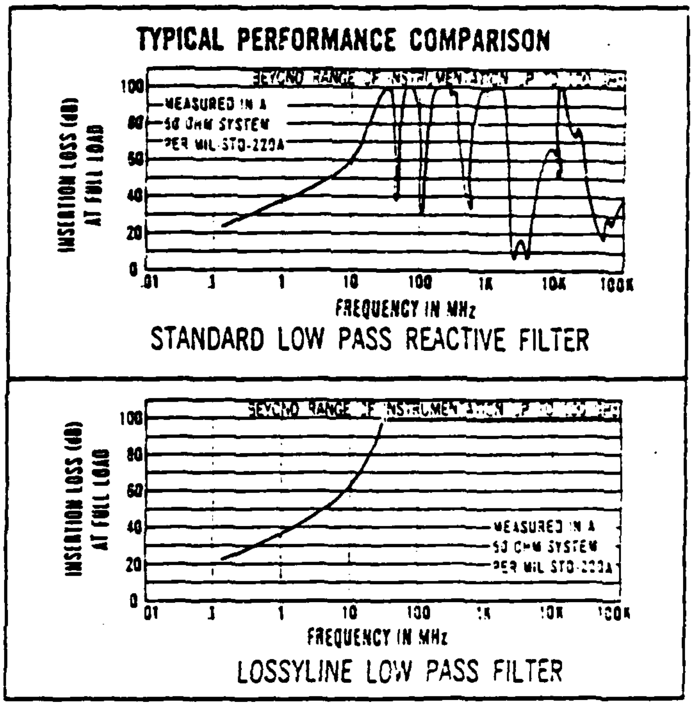


Figure 6.13 Dissipative Filter [6.7]

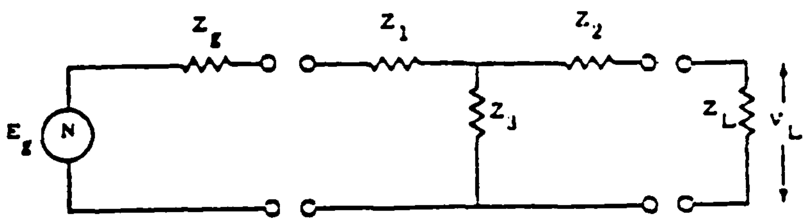


Figure 6.14 General Tee Filter Model [6.4]

a. Up to 70% less weight than separate filter elements.
b. Up to 80% less space than separate filter elements.
c. Reduced number of electrical contacts.
d. Filtering is accomplished at the equipment interface, which is the best location.
e. Elimination of circuit cross talk problems.

Because not much EMP hardness data are available for filter pin connectors, systems qualification tests must be conducted.

Filter pin connectors, available in circular, miniaturized, and subminiaturized rectangular shapes, can accommodate up to 61 contact arrangements, and are available in PI, LC, CL, and the capacitor configurations shown in Figure 6.15. As indicated, ferrite beads can be used to provide dissipative filtering.

Figure 6.16 shows typical insertion loss test results obtained as per MIL-STD-220 on contacts on a filter pin connector.

Reference 6.8 reports some pulse testing data on two types of common filter pin connectors. The type DEJ-9TP is a π section rated with a 2-MHz cutoff frequency. The DEJ-9LP is a special low frequency model with a rated cutoff frequency of 100 kHz. The rated cutoff frequencies were confirmed in both cases, but the π-filter rolled off at 60 dB/decade, while the low frequency model rolled off at 20 dB/decade.

The π-section filter can provide EMP protection because of its higher roll-off. Both of these connectors were tested with rectangular pulses of width 100 ns and 1 μs and amplitudes up to 5 kV. The filters performed according to their frequency characteristics until arcing from pin-to-case occurred as follows:

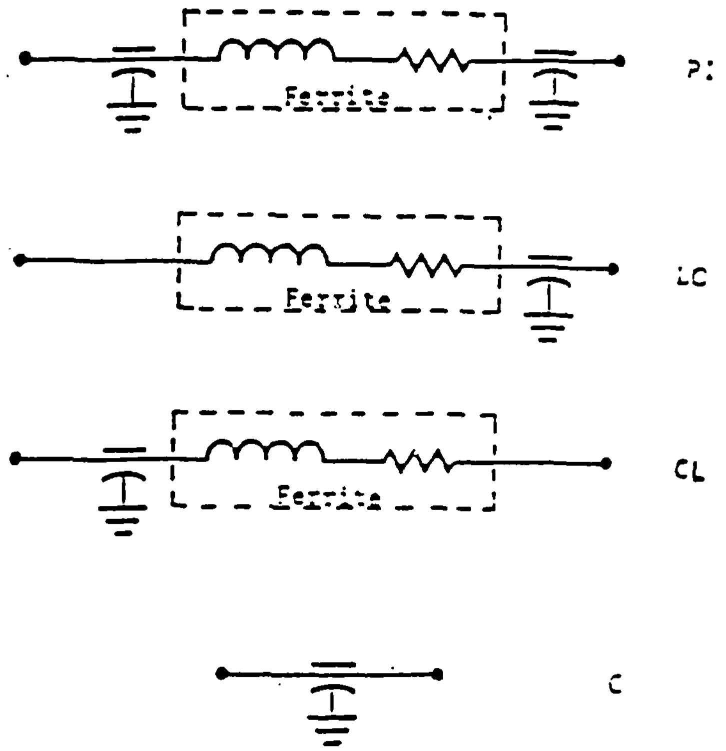


Figure 6.15 Schematics for Filter Pin Configurations [6.6]

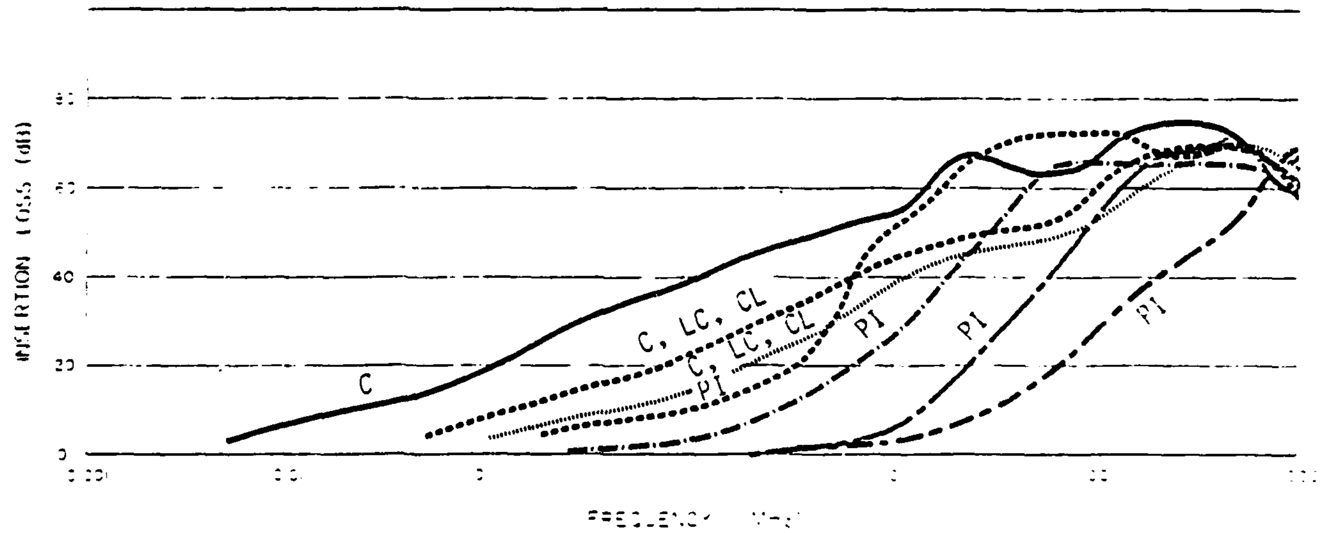


Figure 6.16 Typical Insertion Loss Test Results as per MIL-STD-220 on Filter Contacts in a Filter Pin Connector Mated with a Standard Non-Filter Connector [6.6]

	100 ns	1 μs
DEJ-9TP (π section)	2 kV	1.1 kV
DEJ-9LP (low frequency)	> 5 kV	1.2 kV

No degradation in the frequency characteristics was observed in either connector.

6.2.5 Other Filter Types

Active filters usually include operational amplifiers to perform some filter transfer functions. But, because the operational amplifier is itself an EMP-vulnerable semiconductor device, active filters are not useful for damage hardening. Their usefulness as upset hardening devices is also limited, because operational amplifiers can be upset by saturation.

The piezoelectric effects of monolithic crystal and ceramic devices may be utilized to obtain frequency selectivity. This selectivity depends upon the mechanical resonance of the device. These are high Q bandpass filters with bandwidth on the order of .001 to .7% of their center frequencies. Passive components can be added to make high or low pass filters, which are subject, however, to resonances in the filter stop bands caused by overtones in the fundamental mode of excitation. These filters can operate at frequencies from 5 to 150 MHz.

Mechanical filters make use of mechanical resonators with input and output electro-mechanical transducers. These filters are bandpass devices which are useful in the range of .1 Hz to 50 kHz and which do not present as great a problem with stop band resonances as do the crystal or ceramic filters. Few data are available on the EMP hardness of the above electromechanical filters.

6.2.6 Filter Summary

The type and function of the circuit to be protected and the characteristics of the induced EMP pulse must be considered in selecting filters. Table 6.1 provides a summary of filter characteristics that might help in selecting a particular filter [6.3]. Because all filter types are subject to EMP damage, their damage thresholds should be evaluated.

6.3 Nonlinear TPDs

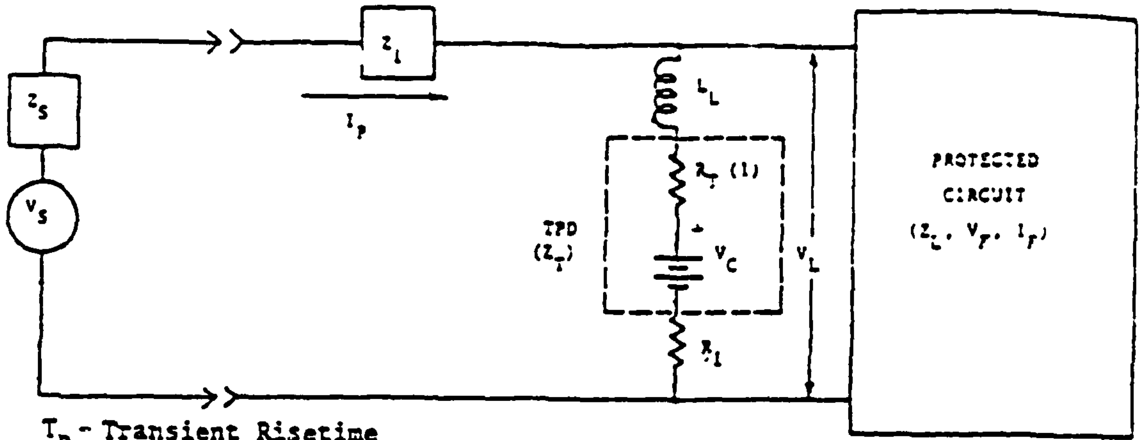
6.3.1 Introduction

Nonlinear terminal protection devices (TPDs) placed across the terminals of the circuit provide protection against EMP transient signal damage. Figure 6.17 illustrates a typical protection configuration and TPD response [6.4]. The purpose of the TPD is to reduce the transient signal voltage to a safe level. Because the TPD is a nonlinear device, it will alter the pulse frequency spectrum. Also, because much of the incident energy is reflected, it must be dissipated elsewhere. For reference purposes, a review of various nonlinear protection devices including their characteristic curves and general application areas is shown in Table 6.2.

Table 6.1 Filter Comparison Matrix [6.8]

FILTER CLASS	FILTER TYPE *	USEFUL FREQUENCY RANGE (Hz)	SIGNIFICANT ADVANTAGES	SIGNIFICANT DISADVANTAGES
Discrete R, L, C	1, 2, 3, 4	to 10^8	• Versatile • Low Cost	• Large for Low Fraquency • Low Q
Ferrite Beads	1	$10^6 - 10^8$	• Versatile • Dissipative With Low Pass Band Loss	• Spurious Resonances • Saturation
Filter Connector	1	$10^4 - 10^9$	• Design Integration Simplicity • Dissipative	• Spurious Resonances • Saturation
Coaxial	1, 2, 3, 4	$10^7 - 10^9$	• High Frequency Use • Low Parasitics	• Large Size
Crystal	3, 4	$5 \times 10^6 - 1.5 \times 10^8$	• High Q • Small Size	• Spurious Resonances • High Cost
Ceramic	3	$10^5 - 10^7$	• High Q • Small Size	• Spurious Resonances • Not IC Compatible
Mechanical	3, 4	$.1 - 2 \times 10^4$	• High Q	• Limited Range • Not IC Compatible • High Insertion Loss
Active	1, 2, 3, 4	to 10^5	• Small Size • Gain Provision	• Power Requirement • Limited Range • Damage Susceptibility

* 1 - Low Pass 3 - Bandpass
2 - High Pass 4 - Band Reject



T_R - Transient Risetime
V_S - EMP Transient Source
Z_S - Source Impedance
Z_l - Distributed Line Impedance
L_L - TPD Lead Inductance
$R_T(I)$ - TPD Effective Resistance
V_C - TPD Clamping Voltage
R_l - Discrete Current Limiting Resistor
Z_L - Load Impedance
V_F - Damage Threshold Voltage
I_F - Damage Threshold Current
I_P - EMP Surge Current
V_L - Circuit Input Voltage

C_T - Shunt Capacity
V_A - TPD Actuation Voltage
V_{SB} - TPD Static Breakdown Voltage
V_E - TPD Extinguishing Voltage
V_P - Peak EMP Voltage

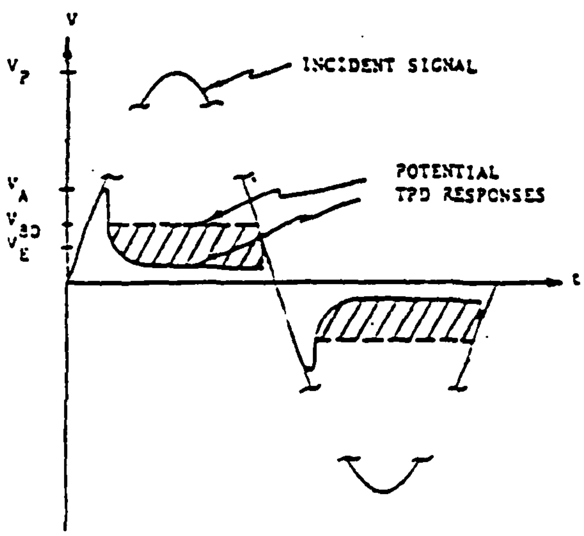
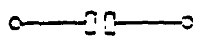
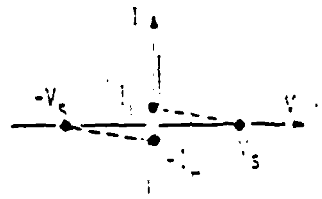
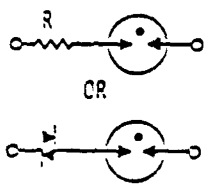
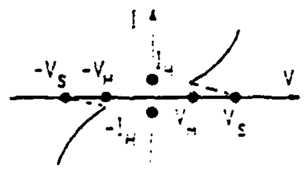
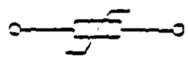
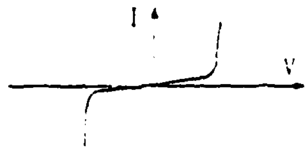
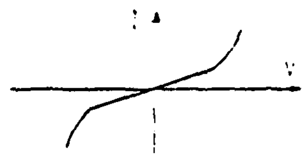


Figure 6.17 Typical Configuration and Response for a Hardened Circuit [6.4]

Table 6.2 Summary of Nonlinear Transient Protection Device Characteristic Curves and General Application Area [6.1]

CATEGORY	NAME	SYMBOL	MAIN V-I CHARACTERISTICS (LINEAR SCALES)	GENERAL APPLICATION
SPARK GAPS	AIR GAP INCLUDING CARBON BLOCK PROTECTOR			SIGNAL AND CONTROL LINES INCLUDING COAX CABLES & ANTENNAS (MEDIUM & HEAVY DUTY)
	GAS TUBE PROTECTOR			
	ARRESTOR (USING GAS TUBE)			AC POWER LINES (MEDIUM & HEAVY DUTY)
VARISTORS	MOV (METAL-OXIDE VARISTOR)			AC & DC POWER LINES (LIGHT & MEDIUM DUTY; HEAVY DUTY IN MULTI-PLES)
	SILICON CARBIDE (SIC) VARISTOR			AC POWER LINES (MEDIUM & HEAVY DUTY SECONDARY ARRESTORS)

LEGEND:

---	SPARKOVER LINE
V	VOLTAGE DROP ACROSS DEVICE
I	CURRENT THROUGH DEVICE
V_S	SPARKOVER VOLTAGE
V_H	HOLDING VOLTAGE
I_H	HOLDING CURRENT
R	LOW-RESISTANCE RESISTOR

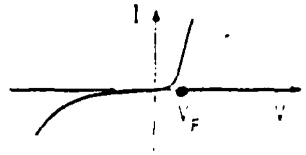
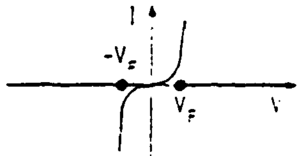
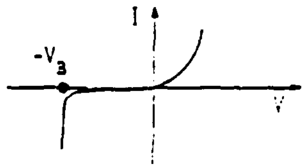
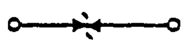
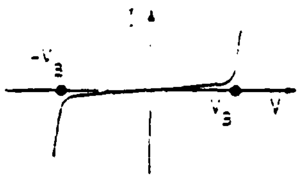
DUTY:

LIGHT - ON PRINTED CIRCUIT CARDS AND INSIDE COMPONENTS

MEDIUM- WITHIN EQUIPMENT

HEAVY - SHIP EXTERIOR

Table 6.2 (cont'd) Summary of Nonlinear Transient Protection Device Characteristic Curves and General Application Area

CATEGORY	NAME	SYMBOL	MAIN V-I CHARACTERISTICS (LINEAR SCALES)	GENERAL APPLICATION
SEMICONDUCTOR OR SELENIUM DIODES	RECTIFIER	SILICON, GERMANIUM, OR SELENIUM 		UNIDIRECTIONAL TRANSIENT SUPPRESSION (LIGHT DUTY)
	BIPOLAR FORWARD			BIDIRECTIONAL TRANSIENT SUPPRESSION (LIGHT DUTY)
	REVERSE BREAKDOWN	SILICON ZENER  SELENIUM SUPPRESSOR 		DC POWER LINES (LIGHT TO MEDIUM DUTY)
	BIDIRECTIONAL BREAKDOWN	SILICON  SELENIUM 		SIGNAL & CONTROL AND AC POWER LINES (LIGHT TO MEDIUM DUTY)

LEGEND:

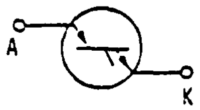
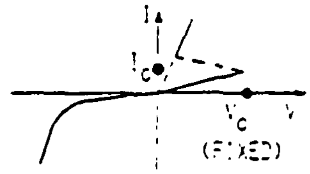
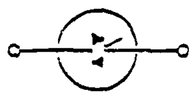
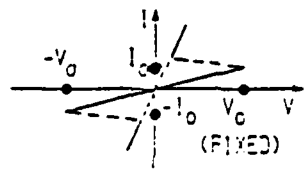
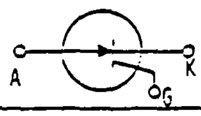
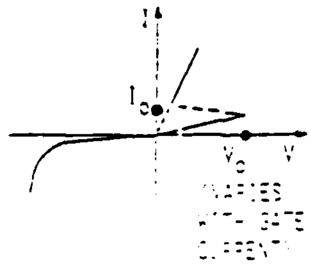
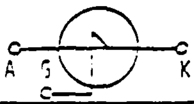
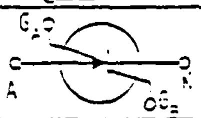
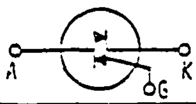
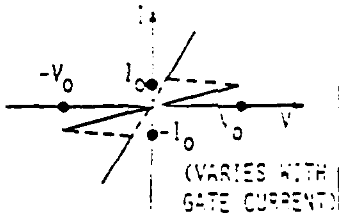
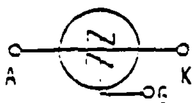
V	VOLTAGE DROP ACROSS DEVICE
I	CURRENT THROUGH DEVICE
V_F	FORWARD THRESHOLD VOLTAGE
V_B	REVERSE BREAKDOWN VOLTAGE
A	ANODE
K	CATHODE

DUTY:

LIGHT - ON PRINTED CIRCUIT CARDS AND INSIDE COMPONENTS

MEDIUM - WITHIN EQUIPMENT

Table 6.2 (cont'd) Summary of Nonlinear Transient Protection Device Characteristic Curves and General Application Area

CATEGORY	NAME	SYMBOL	MAIN V-I CHARACTERISTICS (LINEAR SCALES)	GENERAL APPLICATION
SEMICONDUCTOR THYRISTORS	UNIDIRECTIONAL DIODE THYRISTOR			UNIDIRECTIONAL SUPPRESSOR (LIGHT DUTY)
	DIAC (BIDIRECTIONAL DIODE THYRISTOR)			BIDIRECTIONAL SUPPRESSOR (LIGHT DUTY)
	SCR (SILICON CONTROLLED RECTIFIER)			UNIDIRECTIONAL "CROWBAR SWITCH" (LIGHT TO MEDIUM DUTY)
	SUS (SILICON UNILATERAL SWITCH)			
	SCS (SILICON CONTROLLED SWITCH)			
	TRIAC (BIDIRECTIONAL TRIODE THYRISTOR)			BIDIRECTIONAL "CROWBAR SWITCH" (LIGHT TO MEDIUM DUTY)
	SBS (SILICON BILATERAL SWITCH)			

LEGEND:

---	SWITCHING LINE
V	VOLTAGE DROP ACROSS DEVICE
I	CURRENT THROUGH DEVICE
V_O	BREAKOVER VOLTAGE
I_O	BREAKOVER CURRENT
A	ANODE
K	CATHODE
G	GATE
G_A	GATE A
G_B	GATE B

DUTY:

LIGHT - ON PRINTED CIRCUIT CARDS AND INSIDE COMPONENTS

MEDIUM - WITHIN EQUIPMENT

The most common nonlinear TPDs are classified as dielectric breakdown devices, semiconductor junction breakdown devices, and nonlinear resistors. Dielectric breakdown devices include air or gas-filled spark gap or solid dielectric gap devices. Semiconductor junction devices include zener diodes and ordinary rectifier diodes. In nonlinear resistors (varistors) resistance is a function of the device voltage. TPD characteristics which should be considered in hardening schemes are size, weight, cost, reliability, temperature dependence, damage thresholds, insertion, turnon, protection efficiency, current capability, turn-off, and device polarity.

For system reliability, the normal failure mode of TPDs should be considered, because a TPD is placed directly across a circuit terminal. For example, spark gaps sometimes fail by opening and degrade EMP hardening but do not degrade the intended circuit function. Zener diodes, on the other hand, generally fail by shorting the circuit terminal to ground and degrade circuit function.

TPDs themselves are susceptible to EMP damage. Of these, semiconductor junction devices are particularly susceptible; their damage thresholds may be calculated from Chapter 5.

Two parameters determine the insertion effects of TPDs during normal circuit operation: the shunt capacitance C_T and the leakage current or standby impedance. If the signal source has resistance R_S, and the load resistance is R_L, the 3 dB down insertion loss frequency is given by

$$F_{3db} = \frac{.159}{C_T} \frac{R_S + R_L}{R_S R_L} . \qquad (6.1)$$

The leakage current may be important if power losses or maintenance of high input impedance of the circuit is critical. Insertion loss effects are usually easy to evaluate, since C_T and the leakage current or standby impedance are usually specified by the manufacturer.

The TPD turn-on characteristics refer to the manner in which a TPD responds to an overvoltage pulse. The voltage at which a TPD will initiate its response depends on the rate-of-rise of the pulse's leading edge, and this voltage is often considerably greater than its normal DC breakdown voltage. The worst case rate-of-rise of the leading edge of an EMP signal may be in the range of 62 V/nsec to 6 kV/nsec; few devices respond quickly enough to protect circuits for such high rates of change. Impulse ratio, a measure of the TPD response, is defined as [6.4]

$$IR = \frac{V_A}{V_{BD}} , \qquad (6.2)$$

where V_A is the peak actuation voltage for the actual signal rate of change, and V_{BD} is the DC rated actuation voltage. Figure 6.13 shows the variation in the voltage delivered to the circuit for two different impulse ratios for the same incident voltage waveform [6.4].

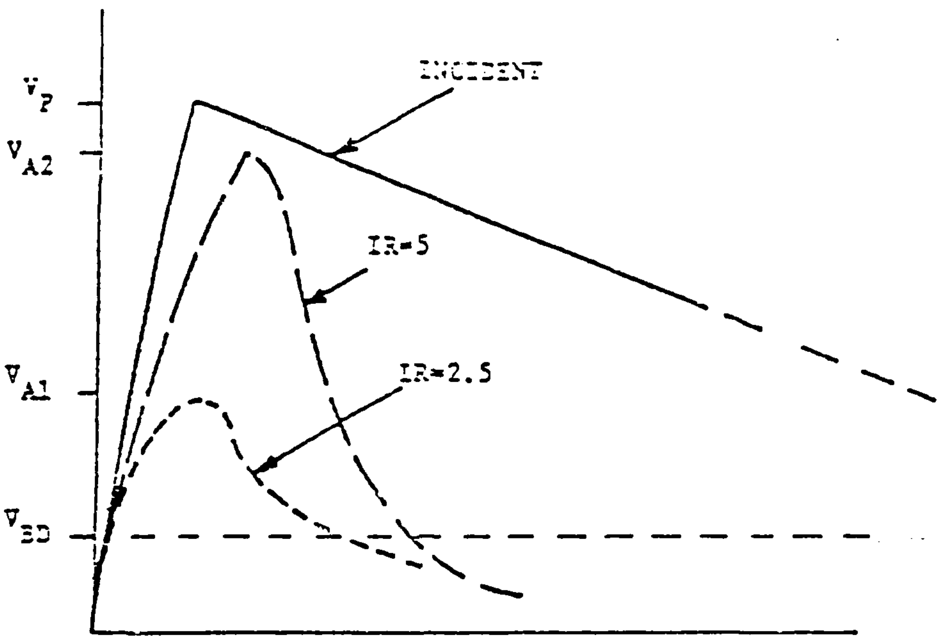


Figure 6.18 Effects of Pulse Ratio on TPD Operation [6.4]

The lead inductance of a TPD affects impulse ratio; this effect is included in (6.2). To isolate the effect of lead inductance, (6.2) may be rewritten as

$$IR = \frac{V_{AI}}{V_{BD}} (1 + \beta_L) , \tag{6.3}$$

where β_L is the voltage overshoot caused by series inductance, and V_{AI} is the TPD actuation voltage with zero external inductance. β_L is given by [6.4].

$$\beta_L = \frac{R_S}{R_T} \left[\frac{L_L}{T_R(R_S + R_T)} \right] \left[1 - e^{-\left(\frac{R_S + R_T}{L_L}\right) T_R} \right] \tag{6.4}$$

where all the quantities are as defined in Figure 6.17. The percent overshoot caused by a series inductance shown in Figure 6.19 where overshoot ($\beta_L \times 100$) is plotted as a function of lead inductance for $R_S = 50\ \Omega$, $R_T = 10\ \Omega$ and T_R = 3 nsec. Lead wire typically has an inductance of 25 to 75 nanohenries per loop inch; thus, the importance of minimizing lead length is emphasized.

The TPD protection efficiency (α) may be defined [6.4] as the ratio of the energy (E_L) delivered to a specified load impedance to the energy (E_i) of the incident transient, i.e.

$$\alpha = \frac{E_L}{E_i} \quad . \tag{6.5}$$

Sometimes, α is defined [6.8] on the basis of the energy delivered to a 50 Ω load by a 1 μsec rectangular pulse as

$$\alpha = \frac{10^{-3}}{E_L(\text{Joules})} \tag{6.6}$$

where E_L is the energy dissipated in the 50 Ω load. The constant of 10^{-3} (1 millijoule) normalizes α to a unity damage constant for a 1 μsec as given by (6.5).

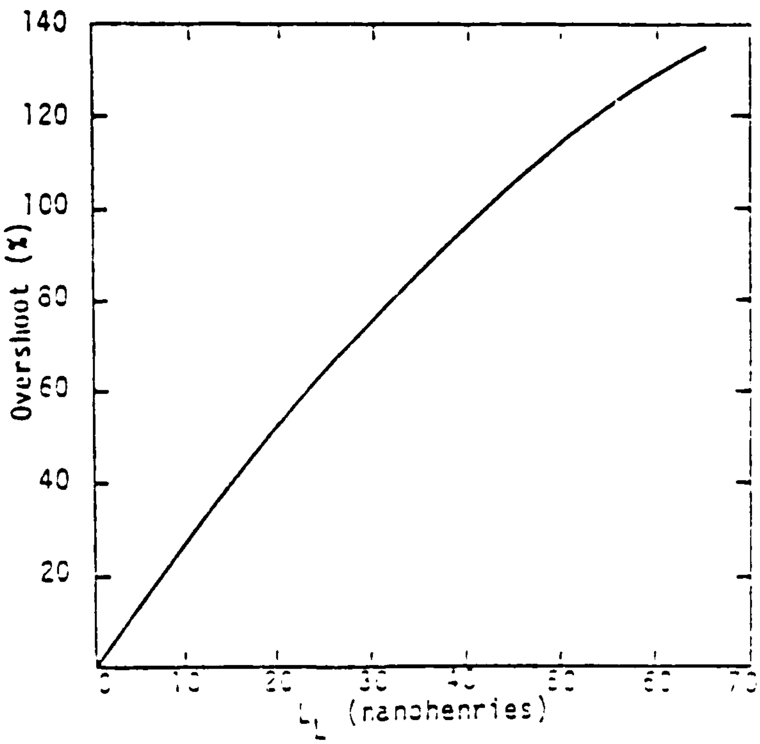


Figure 6.19 Overshoot ($\beta \times 100$) as a Function of Lead Inductance [6.4]

The current capability of a TPD is the amount of current that can flow through the TPD in its breakdown mode. The peak current flowing in the TPD is determined by the transient peak voltage and by the circuit impedances and the internal breakdown resistance and voltage of the TPD.

TPD turn-off is characterized by the way in which the TPD returns to its quiescent operating configuration after breakdown. Sometimes a TPD may stay "latched" in its breakdown state by the normal signals or power being carried on the line. To prevent this, the series resistance of the TPD must be increased to limit the current to the device.

Device polarity refers to the capability of the TPD to limit a bipolar pulse. For example, one gas spark gap performs equally well on a positive or negative pulse, but two back-to-back zener diodes are required to limit a bipolar pulse.

Table 6.3 compares some characteristics of the three most commonly used types of TPDs [6.9].

A list of manufacturers of TPD devices is given in Table 6.4.

6.3.2 Dielectric Breakdown Devices

Dielectric breakdown devices include air and gas-filled spark gaps, neon lamps, surge arrestors, and dielectric simulated breakdown devices. In these latter devices, (though not yet commercially available) a solid dielectric is used to simulate arc formation.

Dielectric breakdown devices are low cost devices used for shunting large overvoltages to ground and are able to handle large power surges. They have low insertion losses at all frequencies below 100 MHz. This enables them to protect antennas and other high frequency equipment. In addition, antennas are capable of picking up large amounts of energy during an EMP event. This, coupled with low insertion losses at high frequency, makes dielectric breakdown devices the principal means of protecting some high frequency equipment. A major disadvantage is their uncertain response time in clamping over voltages.

The response time of a dielectric breakdown device (the time it takes for a spark gap to break down and the breakdown voltage depend upon the rate of transient voltage change, $\frac{dV}{dt}$ (Figure 6.20). Each straight line emanating from the origin corresponds to some constant $\frac{dV}{dt}$. Superimposed on these straight lines are four curved lines, each corresponding to a different spark gap. The intersection of a straight and curved line indicates the voltage and time at which a spark gap will break down for the $\frac{dV}{dt}$ corresponding to that straight line [6.9].

The horizontal lines in Figure 6.20 are the DC breakdown voltages. Although the DC breakdown voltage is not strictly related to EMP because of the fast EMP risetime, the DC level does provide a means of gap checkout.

The responses of two different gaps, along with the surge voltage waveform, are shown in Figure 6.21. Spark gap A fires earlier than spark gap B, because B responds more slowly. The cross hatched area indicates proportionally the additional exposure a sensitive load may have to the voltage surge.

Table 6.3 Comparison Chart of Common Protection Devices Designed for Use in EMP Applications [6.9]

Device	Ability to Divert Large Surge Currents > 500 A	Fast Response to Rapid Transient Voltage Rises	Minimum Capacitance (Minimum Insertion Loss)	Maximum Insulation Resistance	Ability to Protect at Low Voltage Levels < 50 V
Gas-filled spark gap	1	3	1	1	3
Zener diode	3	1	3	2	1
Varistor	2	2	2	3	2

Device	Ability to Protect at High Voltage Levels > 400 V	Ability to Extinguish on DC Systems	Freedom from Susceptibility to Radiation Effects	Capability for Bipolar Operation	Linearity (No Cross Modulation to Voltage Level of Protection)	No Temperature Dependence
Gas-filled spark gap	1	3	1	1	1	1
Zener diode	3	2	3	3	2	3
Varistor	2	1	2	1	3	2

* 1 = most favorable, 3 = least favorable.

Table 6.4 Some TPD Vendors

(1) Gas Filled Spark Gap Vendors

(a) Joslyn
Goleta, California

(b) EG&G
Salem, Massachusetts

(c) Signalite
Neptune, New York

(d) C.P. Clare & Co.
Chicago, Illinoins

(e) Dale Electronics, Inc.
Columbus, Nebraska

(f) TII Industries
Copiague, New York

(g) Siemens Corp.
Iselin, New Jersey

(2) Zener Diode Vendors

(a) General Semiconductor
Tempe, Arizona

(b) Unitrode
Watertown, Massachusetts

(c) Shauer Manufacturing Corp.
Cincinnati, Ohio

(d) Sarkes Tarzian, Inc.
Bloomington, Indiana

(e) Thomson-CSF
Canoga Park, California

(f) Westinghouse
Youngwood, Pennsylvania

(g) Motorola
Phoenix, Arizona

(h) Micro Semiconductor
Santa Ana, California

(3) Varistor Device Vendors

(a) General Electric
Syracuse, New York

(b) ITT
Lorrance, Massachusetts

(c) Midwest Components
Muskegan, Michigan

(d) Fuji Electric Co., Ltd.
Tokyo, Japan

(e) Panasonic
Secaucus, New Jersey

(f) International Rectifier
El Segundo, California

(4) Hybrid TPD Vendors

(a) Transtector Systems, Inc.
Monterey Park, California

(b) MCG Electronics
Deer Park, New York

(c) Lightning Elimination Assoc.
Downey, California

(d) Fischer Custom Communications

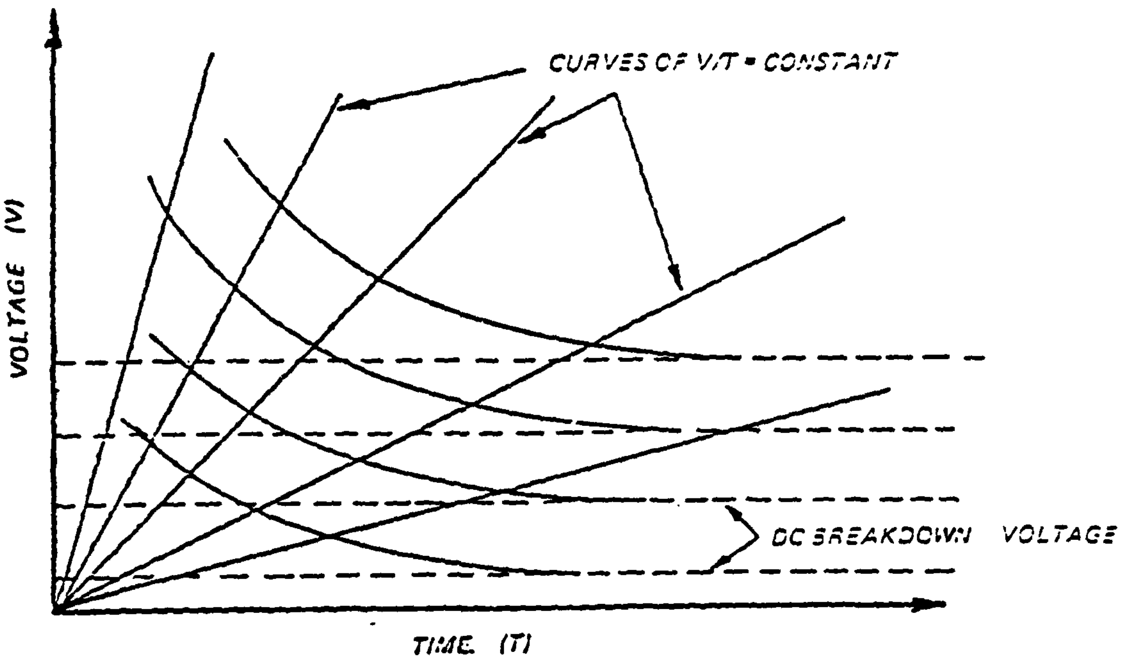


Figure 6.20 Volt-Time Curves [6.9]

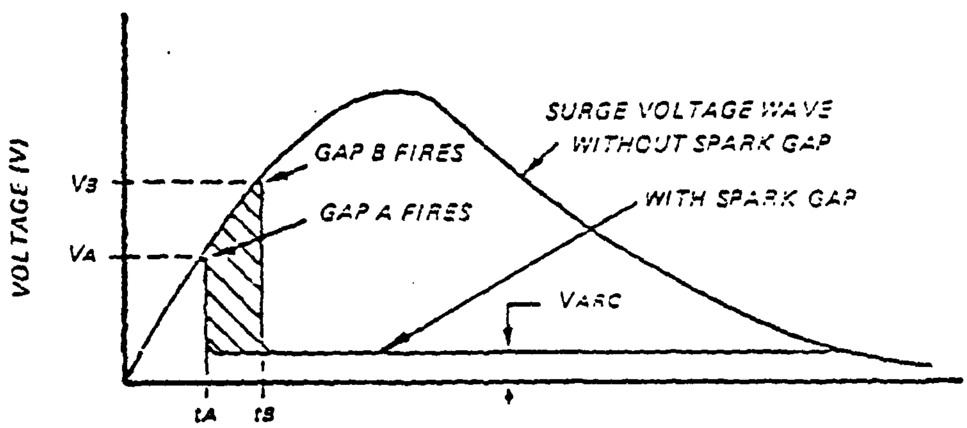


Figure 6.21 Spark Gap Response [6.9]

Figure 6.22 shows the effect of a spark gap on the circuit it is protecting. Part A shows the waveform without the spark gap. Part B shows the waveform with the gap on line; the gap breaks down at time T_A and reduces the voltage to a low level, called the arc voltage.

As illustrated in Figure 6.23, the EMP signal Thevenin equivalent is first determined in order to find the maximum gap current, I_{max}. The gap peak current must be identified because high current levels can physically damage the gap by melting leads or burning away electrodes.

A series limiting resistor provides a method for limiting the gap peak current (Figure 6.24). The resistor has no effect until the TPD breaks down. In this case, the voltage drop, IR, across the resistor is now added to the gap voltage. The voltage across the protected circuit is now increased, which implies less protection. The inductance of the resistor will also slow down the response time. Figure 6.25 illustrates the decrease in gap current caused by the resistor.

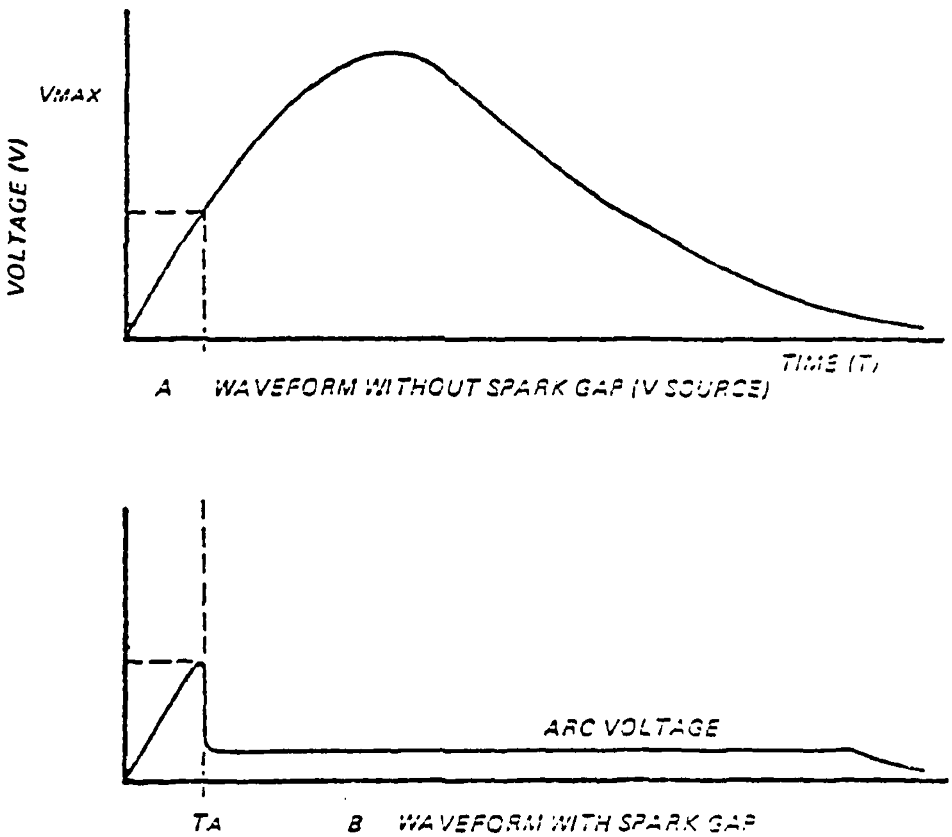


Figure 6.22 Voltage Waveforms [6.9]

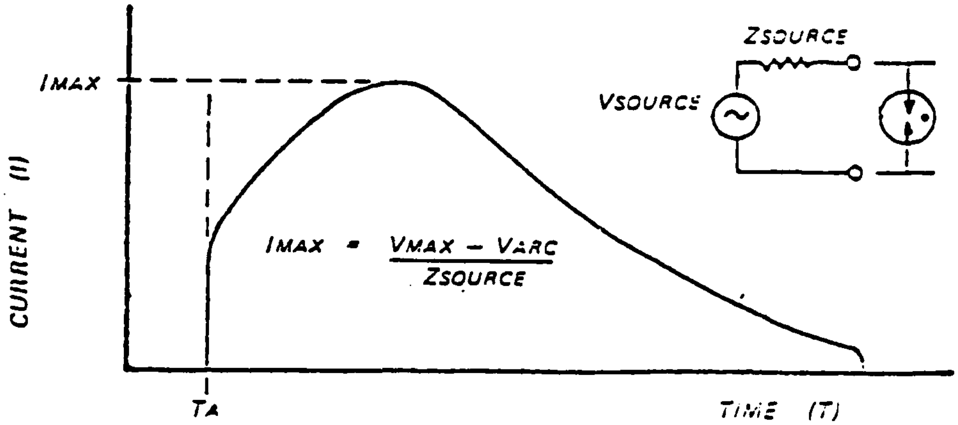


Figure 6.23 Surge Current Waveform [6.9]

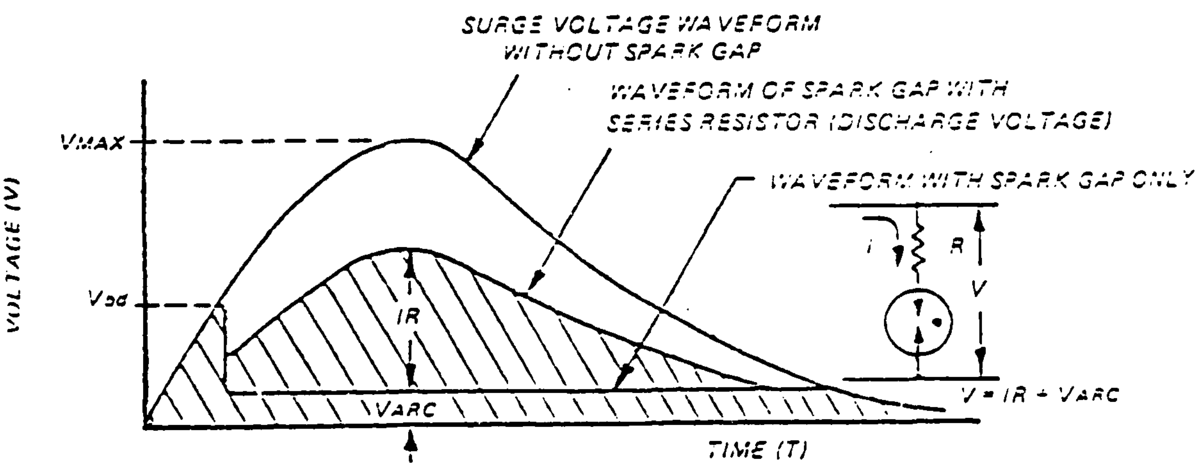


Figure 6.24 Surge Voltage for Gap with Current Limiting Resistor [6.9]

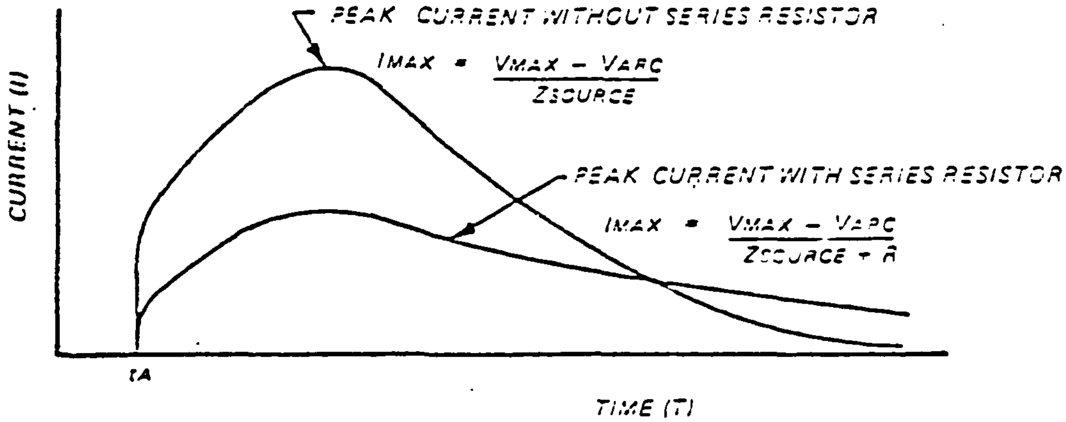


Figure 6.25 Surge Current Waveform for Gap with and without Series Resistor [6.9]

It is important that gap conduction be stopped (extinguished) after the EMP event is terminated. Figure 6.26 shows the relationship between voltage, current, and the extinguishing region. Here, a discharge will extinguish if the TPD operating point lies in the cross-hatched area, whereas the discharge will continue if it lies above the curve. If the only voltage source on the protected line is the EMP signal, the gap will extinguish. However, if the gap protects a DC powerline, the voltage levels and source impedance may be such that the gap will not extinguish. The gap would then continue to short the power supply, and damage could result. Normal circuit operation could not then be obtained until the arc was extinguished.

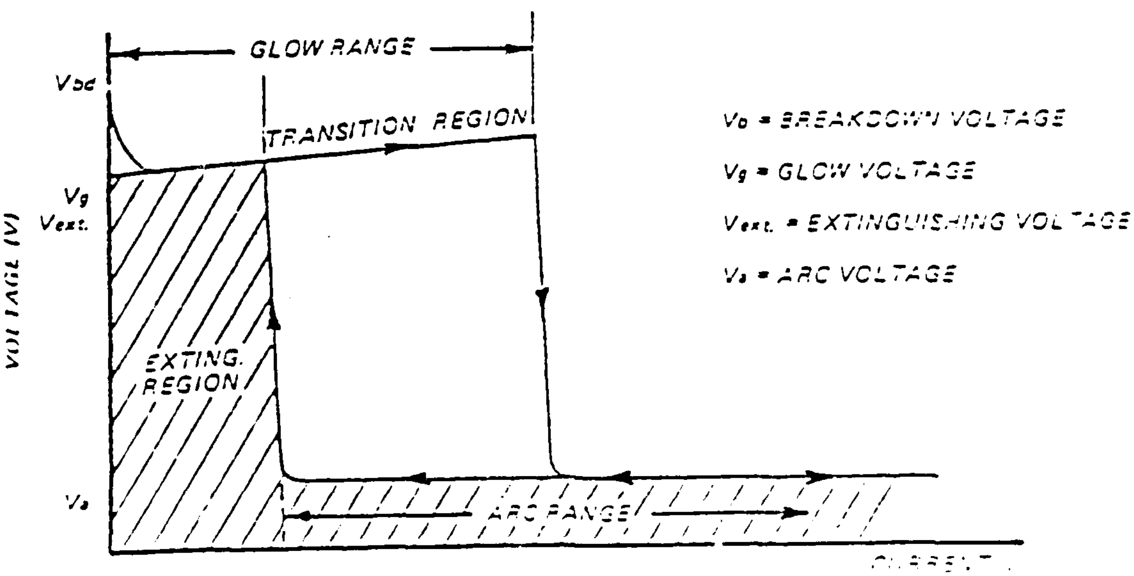


Figure 6.26 DC Holdover Curve [6.9]

If the gap is protecting an AC system, the gap will usually extinguish because the voltage and current return to zero every half cycle. The gap may conduct, however, from the time the surge ends until the end of the half cycle in progress, as shown in Figure 6.27. This phenomenon is called follow current. Even though limited to a half cycle, this follow current can cause deterioration of the spark gap, changes of breakdown voltage, and insulation resistance [6.9].

Spark gaps may be connected in series to extend the extinguishing region, as in Figure 6.28. The breakdown voltage and arc voltage are doubled also.

Neon lamps are designed for operation in a glow rather than an arc mode (Figure 6.26). They perform adequately as TPDs when low energy (< 1 joule) transients are involved.

Test results on the types of spark gaps listed below are reported in Reference 6.8:

Signalite CG Series Spark Gap

Signalite SB Series Spark Gap

Signalite Uni-Imp* Spark Gap, UBD series

Chicago Miniature Neon Lamps (NE-2, NE-51, NE-86)

Dale LA9 Series Surge Arrestor.

The Signalite CGL series "Comm Gap", which is a low voltage surge arrestor with welded leads and miniaturized ceramic construction, is principally used in the telecommunications industry. The CO-75L, 470L, and 1000L were tested. The SB series device is a two-electrode spark gap (dc overvoltage protector) enclosed in a glass envelope. Devices SB-.55, 1.0, and 4.0 were evaluated. The Uni-Imp spark gaps are a special family which activate at their specified breakdown voltages for faster risetimes than the other conventional Signalite spark gaps. The UBD-.55, UBD-1.0, and UGT-4.0 Uni-Imps were evaluated. The Chicago Miniature neon glow lamps are cold-cathode devices with two electrodes separated in a neon-filled envelope. The NE-2, NE-51, and NE-86 lamps were tested.

The Dale LA9 series surge arrestors, which are spark gaps hermetically sealed in a case with a single-ended flange mounting, function as voltage-sensitive switches using a surge-charge coil in conjunction with a tapered spiral electrode. The arc is initiated between the top of the spiral electrode and a cylindrical electrode. When the coil is energized, it produces a magnetic field which causes the arc to rotate down the tapered spiral and to lengthen to the breaking point before excess current is drawn. The spark gap atmosphere is pre-ionized by a radioisotope. Devices designated LA9BIC-500, 1 kV, and 4 kV were evaluated.

For each device type, at least three samples were evaluated during each parameter measurement.

Figure 6.29 to 6.31 show the voltage-time characteristics of the spark gaps evaluated. Table 6.5 is a summary of the characteristics of the devices tested. None of these devices failed. The manufacturers do not specify the power dissipated by the device. The device actually reflects most of the incident energy.

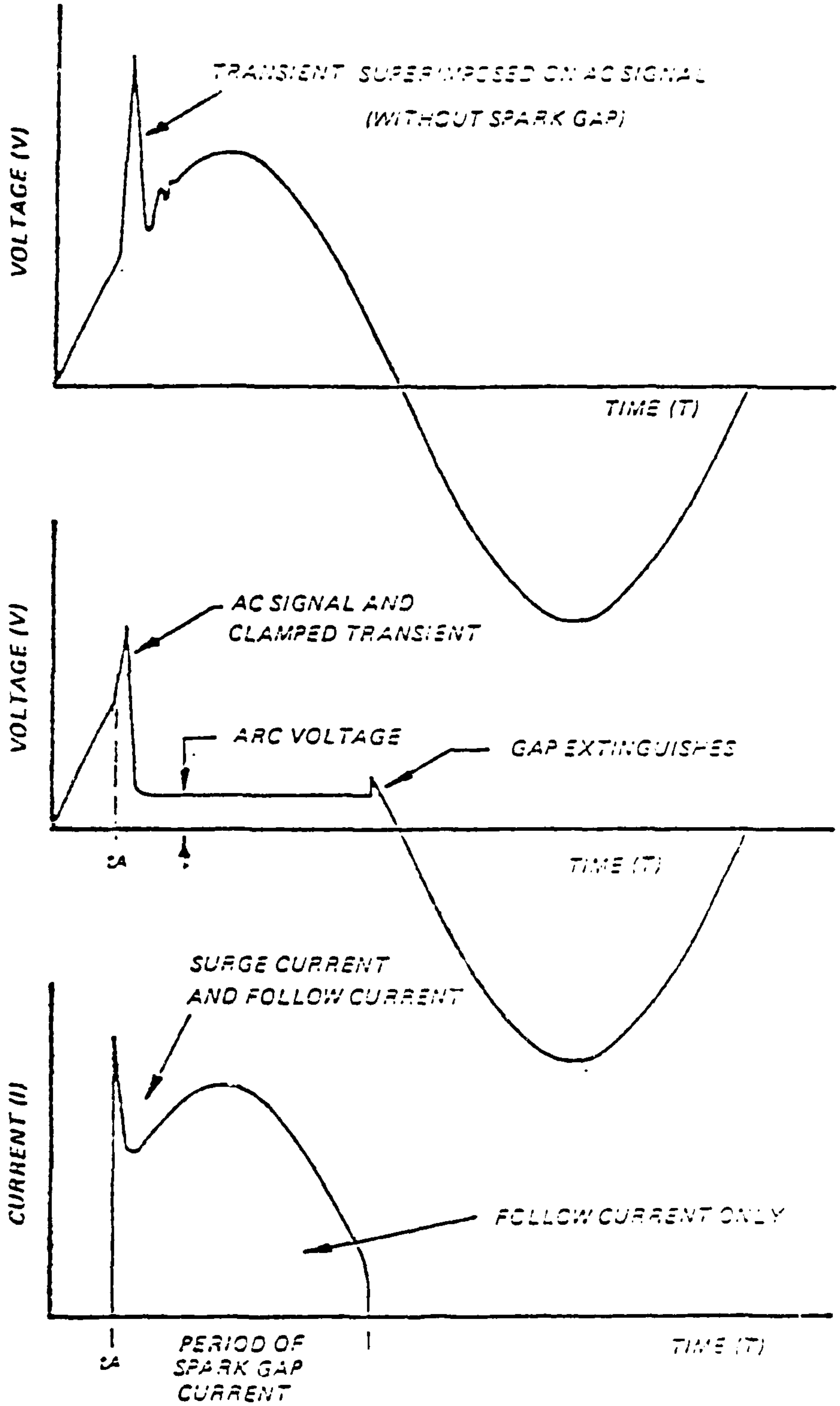


Figure 6.27 Follow Current [6.9]

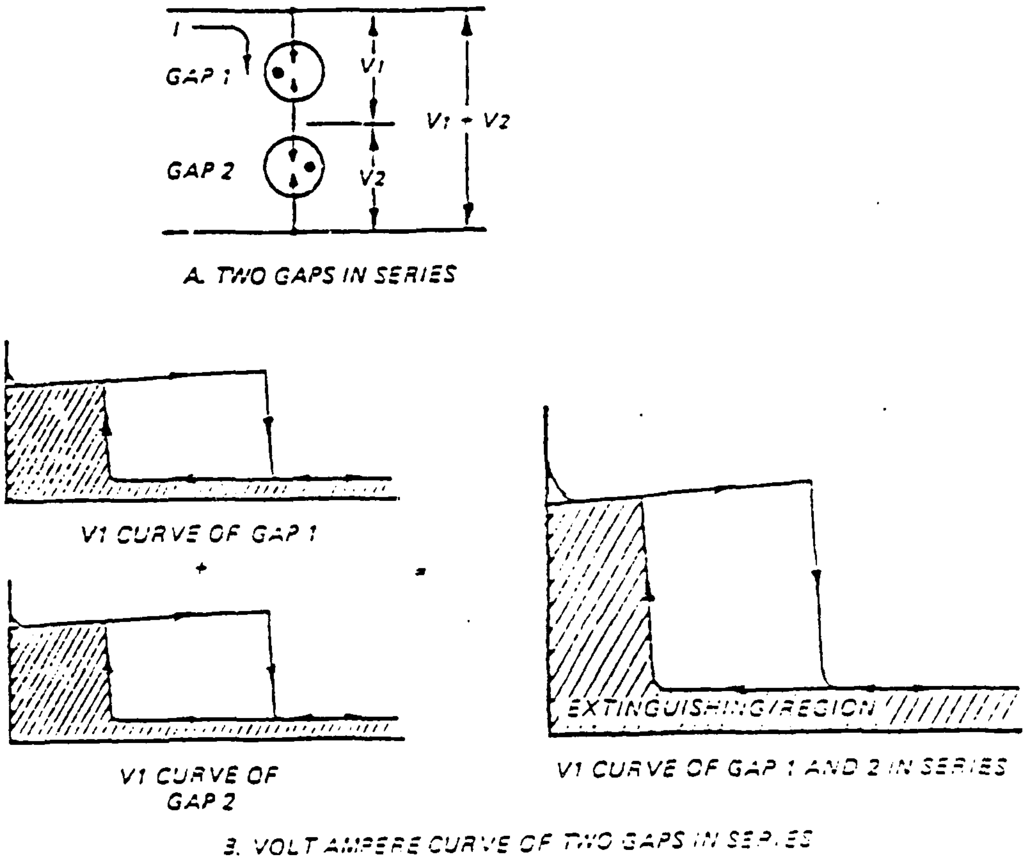


Figure 6.28 The Effect of Adding Spark Gaps in Series [6.9]

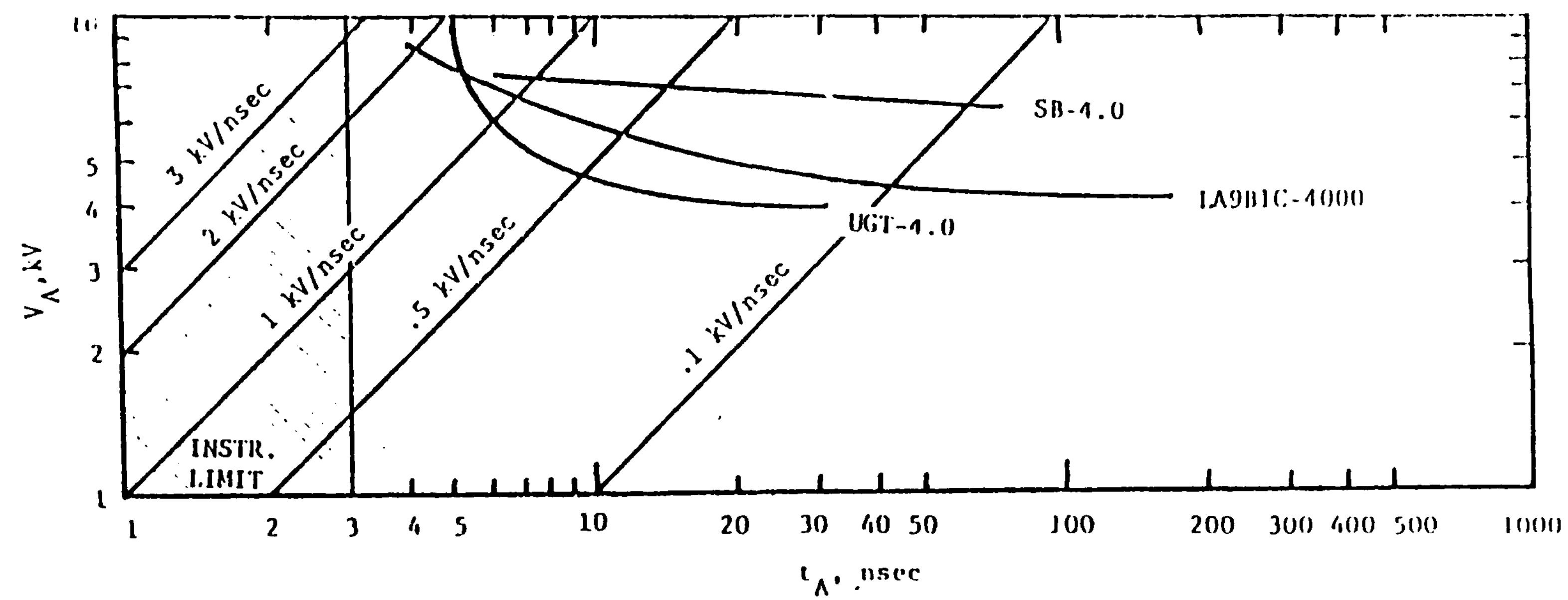


Figure 6.29 Actuation Voltage Versus Time for Several 4000-Volt Dielectric Breakdown IPD's (Ref. [6.8])

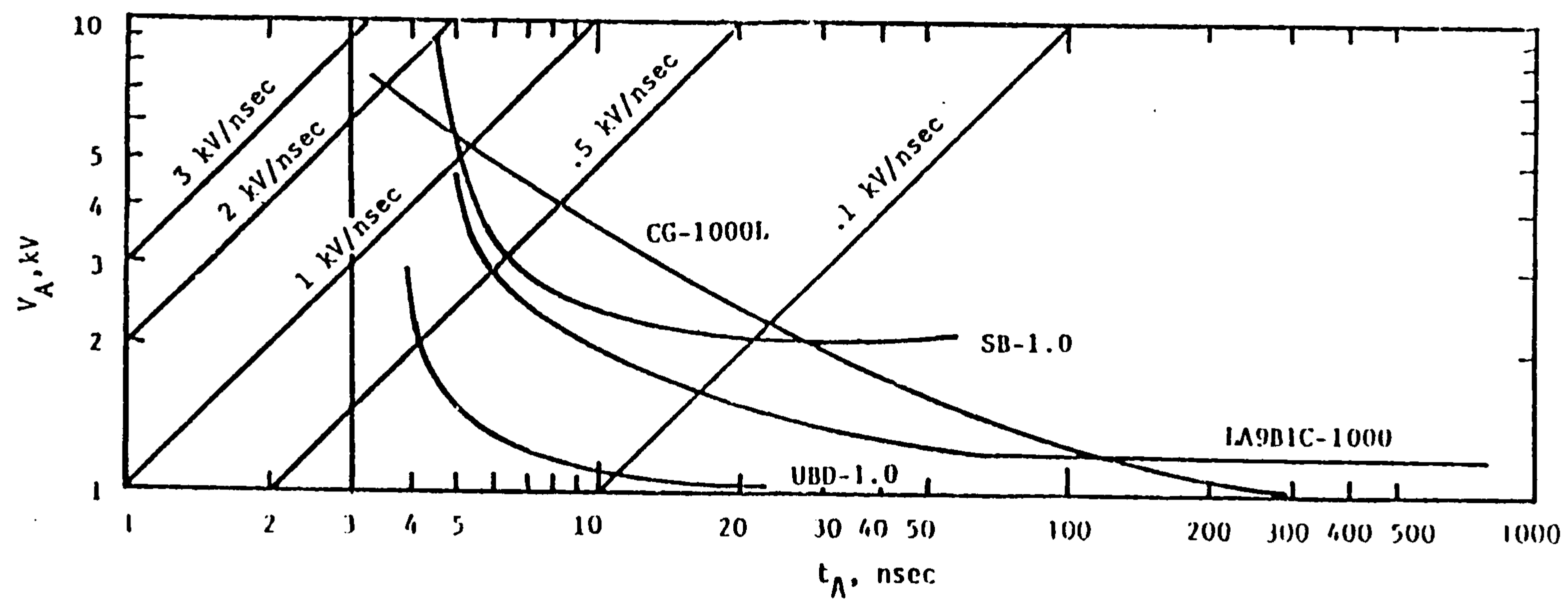


Figure 6.30 Actuation Voltage Versus Time for Several 1000 Volt Dielectric Breakdown IPD's [6.8]

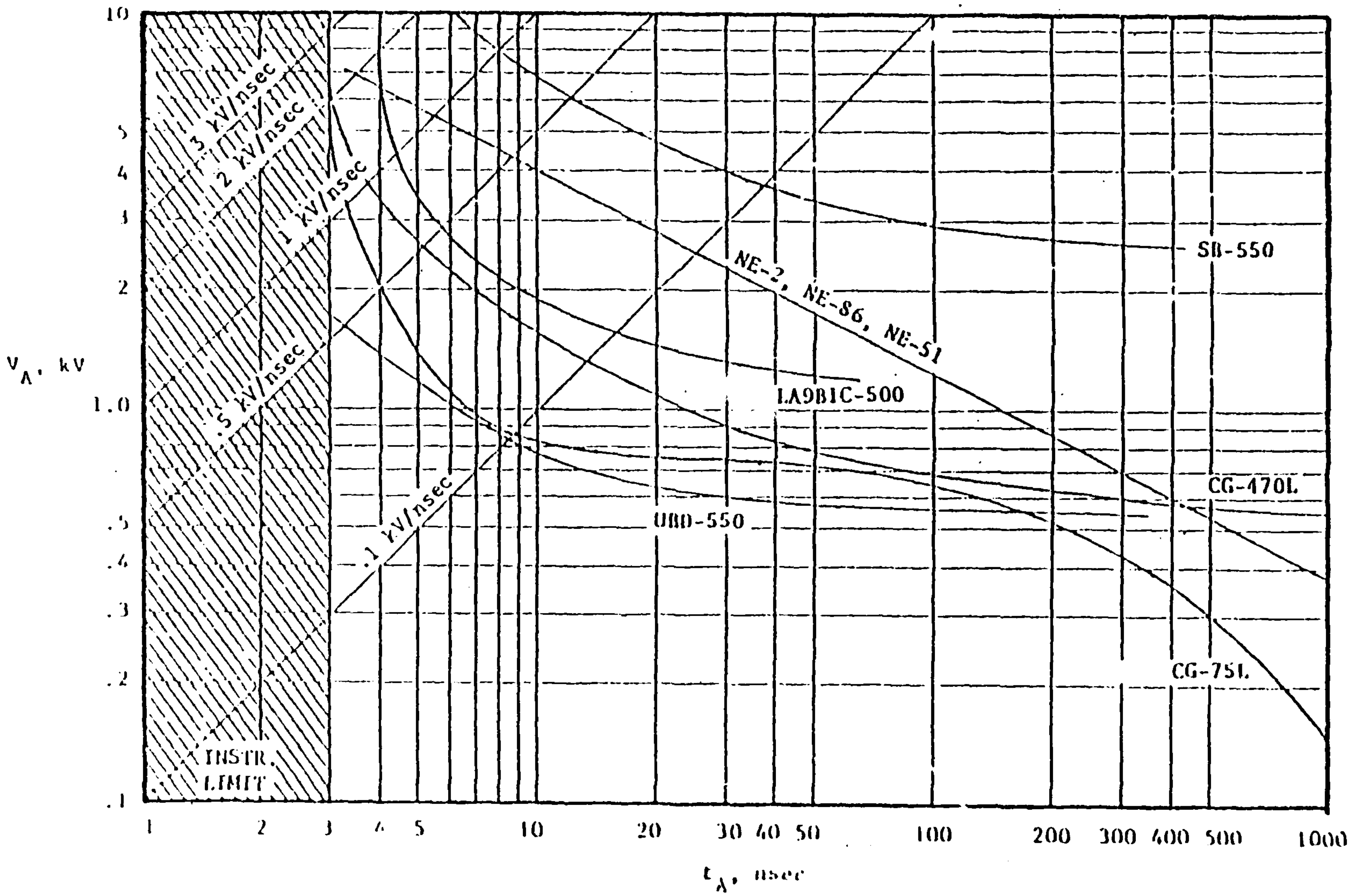


Table 6.31 Actuation Voltage Versus Time for Eight Different Types of Lower Voltage Dielectric TPDs [6.8]

Table 6.5 Spark Gap Parameter Matrix [6.8]

Device Family	Device Type	Speci-fied V_{BD} Volts	Average Measured V_{BD} Volts	Speci-fied P_{DISS} Watts	Maximum No-Fail Pulse Current, Amps	Maximum Pulser Output No-Fail Energy, Joules	V_A @ T_A= 10ns Volts	Voltage at 10 Amps Volts	Protec-tive Effici-ency α	F_{3dB} MHz
Uni-Imps	UBD-.55	550	555	-	880	162	.8 kV	23	4.1	2109
	UBD-1	1000	1125	-	890	162	1.1 kV	-	2.43	597
	UGT-4	4000	4450	-	880	162	4.5 kV	-	1.28	3975
Spark Gaps	CG-75L	75	78	-	880	162	.83kV	17	9.17	6115
	CG-470L	470	475	-	880	162	1.5 kV	22	2.26	9830
	CG-1000L	1000	1000	-	880	162	3.5 kV	-	1.38	11564
	SB-.55	550	557	-	880	162	7.0 kV	53	.05	10144
	SB-1	1000	1147	-	880	162	2.4 kV	-	1.08	4051
	SB-4	4000	4533	-	880	162	7.2 kV	-	.003	8379
Neon Lamps	NE-2	110	72	-	880	162	4.5 kV	-	.75	13060
	NE-86	55-90	70	-	880	162	4.2 kV	-	.35	9493
	NE-51	500	505	-	880	162	3.4 kV	-	.61	3457
Surge Arres-tors	LA9B1C-500	500	505	-	880	162	1.85kV	-	.38	1530
	LA9B1C-1000	1000	1127	-	880	162	1.9 kV	-	.5	1519
	LA9B1C-4000	4000	4400	-	880	162	5.8 kV	-	.07	1761

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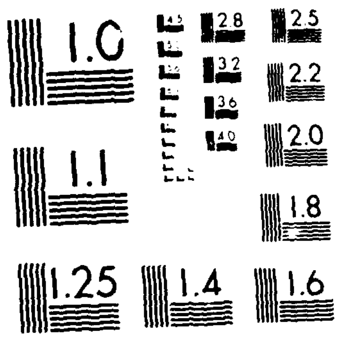

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NATIONAL BUREAU OF STANDARDS 1963-A

The protective efficiency is defined according to (6.7). F_{3db} is obtained for a 50 Ω source and load impedance, and C_T is obtained from (6.2).

Reference 6.10 and 6.11 present test data on several types of TPDs. A summary of the spark gaps tested in Reference 6.10 and some of the device characteristics are presented in Table 6.6. A summary of the spark gaps tested in Reference 6.4 is shown in Table 6.7.

The results of the tests summarized in Table 6.5 showed that the measured breakdown voltages of the dielectric breakdown devices was within 15% of the specified breakdown voltage except for the NE-2 neon lamp. Spark gaps demonstrated considerable current handling capabilities (880 A) without failure. In addition, spark gaps also demonstrated low insertion losses. In fact, all of the spark gaps tested had 3 dB insertion losses well over 100 MHz with most devices showing 3 dB insertion losses occurring over 1 GHz.

In the study reported in Reference 6.11, spark gaps were tested to determine insertion loss response time and pulse power handling capability. The results of spark gaps are summarized in Table 6.7.

In the initial round of tests the pulse width was 50 nsec and the amplitudes measured across a matched 50 Ω load with no TPD in place were 1, 3.8, 8.2, and 11 kV. When post-pulse tests indicated that a device had been damaged, no further pulses were applied to that device. A listing of the undamaged or surviving devices was completed after the tests.

The second series of tests (which was applied to the survivors of the first tests), the pulse width was increased to 500 nsec, and the amplitudes were 3.5, 7.5, and 11 kV. These additional tests were, of course, intended solely to study the energy dissipation capacities of the devices to a somewhat greater extent. All the spark gaps subjected to the pulse tests survived. All of the spark gaps tested in this program appear about equally effective for EMP protection. This does not mean that they are equivalent, merely that the test methods could not distinguish between them. The principal drawbacks to using spark gaps are the high DC breakdown voltage and the relatively high-energy leakage, especially with small overvoltages.

Of the devices that survived both pulse tests, only spark gaps have acceptably low-insertion loss over the frequency range from 0 to 100 MHz. Therefore, if wide-band and high power protection is needed at the upper end of or beyond the above range, it can at present be provided only by spark gaps.

Spark gaps frequently fire slowly and erratically at overvoltages of less than 2 or 3 times the DC breakdown voltage. For this reason, they often allow greater energy leakage for small overvoltages than for large overvoltages. Also, because of the arc formation time, spark gaps generally pass somewhat more energy - even when significantly overvolted - than do semiconductor devices, which respond rather rapidly.

The speed of response of each device depends strongly on the method of installation. In fact, the overall response is dominated by such things as lead inductance and the impedance mismatch offered by the test chamber. Other tests have shown that lead inductance is the more important. It is therefore of utmost importance to provide the shortest possible shunt paths for transient

Table 6.6 Spark Gap Characteristics [6.4]

Part Number	Vendor	Maximum Operating Voltage (Volts)	Maximum Breakdown Voltage (Volts)	Pulse Power/ Energy Rating	Weight	Approximate Dimensions Diameter (in.)	Approximate Dimensions Length (in.)	MIL Approved
2001-06*	Joslyn	115	730 at 10 kv/μsec	NS	0.05 oz	5/16	11/32	Yes MIL-Q-9858A Boeing D1-8000A
2001-07*	Joslyn	175	870 at 10 kv/μsec	NS	0.05 oz	5/16	11/32	
2001-08*	Joslyn	235	1030 at 10 kv/μsec	NS	0.05 oz	5/16	11/32	
2001-09	Joslyn	400	1390 at 10 kv/μsec	NS	0.05 oz	5/16	11/32	
2001-31	Joslyn	115	875 at 10 kv/μsec	NS	≈0.05 oz	5/16	11/32	
2001-28	Joslyn	375	< 2000 at 50 kv/μsec	NS	≈0.05 oz	5/16	11/32	Yes MIL-Q-9858A Boeing D1-8000A
2021-11	Joslyn	145	500 at 5 kv/μsec	NS	NS	0.312	0.248	No
2021-21	Joslyn	800	1500 at 8 kv/μsec	NS	NS	0.312	0.248	No
2301-13P	Joslyn	400	NS	NS	NS	NS	NS	No
UFT 1.6	Signalite	1600	1600 at 200 kv/μsec	NS	7.5 gm	0.620	0.875	No
UFT 0.8	Signalite	800	800 at 200 kv/μsec	NS	7.5 gm	0.620	0.875	No
UBD-0.8KV	Signalite	400	800 at 200 kv/μsec	NS	7.5 gm	0.620	0.875	NS
UBD-1.6KV	Signalite	1600	1600 at 200 kv/μsec	NS	7.5 gm	0.620	0.875	NS
CG-75	Signalite	40	1000 at 5 kv/μsec	NS	1.05 gm	0.300	0.265	Yes MIL-STD 202
CG-230	Signalite	115	1500 at 6 kv/μsec	NS	1.05 gm	0.300	0.265	Yes MIL-STD 202

*Data for these devices with leads is identical for the 2001-01, 2001-02, 2001-04 without leads.

NS = Not specified on data sheet

Table 6.7 Approximate Safe and Failure Pulse Voltage Levels for Each Commercial Device Tested. (Applied Pulse Widths were 50 and 100 nsec. A Dash Means that the Corresponding Level was not Determined [6.11]

Mfr	# Tested	Type	Description	V_B (V)	Safe Voltage at 50 nsec (V)	Failure Voltage at 50 nsec (V)	Safe Voltage at 500 nsec (V)	Failure Voltage at 500 nsec (V)
TII	1	300B	Gas-tube arrester	300-500	11000	-	"	-
"	1	300C	"	500-900	"	-	"	-
"	1	300A	"	150-300	"	-	"	-
SIEMENS	2	B2-B470	Spark gap	470	11000	-	11000	-
"	2	B2-H25	"	2500	"	-	"	-
"	2	B1-C90	"	90	"	-	"	-
"	2	KA6	"	6500-9500	"	-	"	-
"	2	B1-A350	"	350	"	-	"	-
"	2	B1-A230	"	230	"	-	"	-
"	2	B1-F90	"	90	"	-	"	-
"	2	B2-B800	"	800	11000	-	11000	-
"	2	B1-C145	"	145	"	-	"	-
"	1	B2-H10	"	1000	"	-	"	-
JOSLYN	2	2001-06	Miniature spark gap	230	11000	-	11000	-
"	2	2001-07	"	350	"	-	"	-
"	2	2001-08	"	470	"	-	"	-
"	2	2001-09	"	800	"	-	"	-
"	1	2001-31	"	230	"	-	"	-

cont'd

Table 6.7 (cont'd) Approximate Safe and Failure Pulse Voltage Levels for Each Commercial Device Tested. (Applied Pulse Widths were 50 and 500 nsec. A Dash Means that the Corresponding Level was not Determined).[6.11]

Mfr	# Tested	Type	Description	V_B (V)	Safe Voltage at 50 nsec (V)	Failure Voltage at 50 nsec (V)	Safe Voltage at 500 nsec (V)	Failure Voltage at 500 nsec (V)
DALE	2	LA9A1A/300V	Preionized spark gap	300	11000	-	11000	-
"	2	LA9A1A/400V	"	400	"	-	"	-
"	2	LA9A1A/500V	"	500	"	-	"	-
"	2	LA9A1A/750V	"	750	"	-	"	-
"	2	LA9A1A/1000V	"	1000	"	-	"	-
EG&G	1	GP-57-6	"	6000	11000	-	11000	-
"	1	GP-44L	"	12500	11000	-	11000	-
"	1	GP-64-4.9	"	4900	"	-	"	-

currents (except in the case of filters). This implies very small TPD packages with short or no leads.

Table 6.8 shows the response of the spark gaps tested. Figure 6.32 defines the parameters in Table 6.8. The test results show that, although a large voltage pulse bypasses the spark gap, the pulse width is narrow. Consequently, the amount of energy leaking past the spark gap is generally small ($\sim 1\%$).

Reference 6.12 discusses the developmental work being performed on a common chamber spark gap with multiple pins for use in systems where many signal lines need protection. This device is a simple, compact unit providing electromagnetic pulse (EMP) and lightning protection of systems in which many signal lines enter sensitive electronic equipment. Basically. because it takes one device to protect each wire entering a system, the efficient packaging of the multiple pin electronic surge arrester (Bulk ESA) provides a surge arrestor which has the advantages of space saving, low cost, and simplified assembly over the use of current protective devices which range from diodes to large spark gaps. The multiple-spark-gap (bulk ESA) protector developed is a sealed chamber containing 53 inline spark gaps. Each end of the chamber contains a standard 53-pin connector. The sealed chamber is filled with argon gas at 12-mm pressure, to which a trace of radioactive gas is added to stabilize the breakdown and enhance the fast-rise response.

The bulk ESA can be integrated with an EMI filter-pin connector which, in turn, can improve the performance of the bulk ESA. These two assemblies provide a method to help protect against EMP, lightning, EMI, and TEMPEST effects.

Although non-gaseous dielectric breakdown devices are not commerically available. they exhibit the same general characteristics as their spark gap counterparts. [6.13]. Figure 6.33 compares the Signalite Uni Imp Series UBD-550 which is a dielectric breakdown device. The Signalite spark gap has the following properties: 1) 550 Volt DC breakdown voltage, 2) shunt resistance of $1.5 \times 10^{12}\Omega$, 3) 9.5 pf shunt capacitance, and 4) pulse breakdown voltages of 4 kV at 5 kV/ns and 2 kV at 500 V/ns. The dielectric breakdown device has the following properties: 1) 600 Volts DC breakdown voltage, 2) shunt resistance of $4 \times 10^{13}\Omega$, 3) 9.5 pf shunt capacitance, and 4) pulse breakdown voltages of 1.6 kV at 5 kV/ns and 1.85 kV at 500 V/ns. They both have current handling capacities in excess of 1 kA. When subjected to two 100 ns pulse tests of 1) 10 kV peak voltage with a rise time of 5 kV/ns and 2) 5 kV peak voltage with a rise time of 500 V/ns, the devices did not fail and clamped the overvoltage transient (cf. Figure 6.33).

6.3.3 Semiconductor Junction Devices

Semiconductor junction devices are TPDs which include rectifiers and zener diodes. These devices provide EMP protection by "clipping" voltage transients to desired levels through either avalanche or zener breakdown of the semiconductor junction. The breakdown mechanisms are well understood and discussed in standard solid-state textbooks.

Semiconductor junction devices find most applications as low power transient suppressors. However, semiconductor junction devices that can handle large power surges are available or can be constructed by stacking many such devices

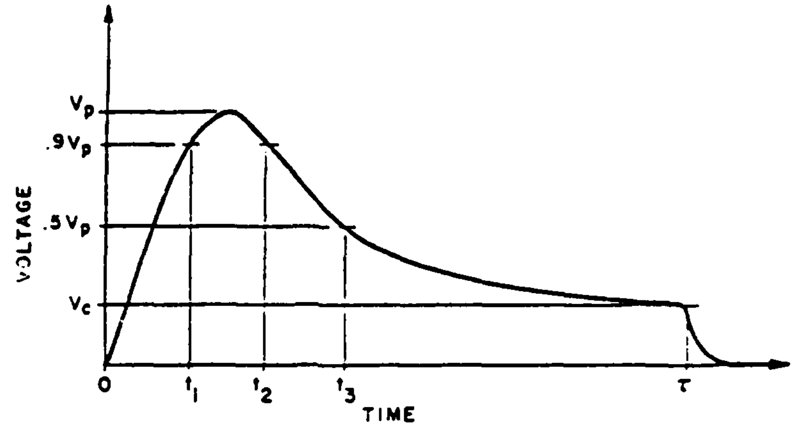
Table 6.8 Voltage Overshoot Parameters for Each Commercial Device That Survived all 50 nsec Pulse Tests. (Corresponding Energy Leakages into a 50 Ω Load are also Shown). [6.11]

Mfr	Type	Description	V_B	Peak Voltage (V)	Clamp Voltage (V)	Rise Time (nsec)	Dwell Time (nsec)	Width (nsec)	Energy Leakage (mJ)
TII	300B	Gas-tube arrester	300-500	3900	<300	1.5	1.0	4.1	0.87
"	300C	"	500-900	3900	<300	1.5	1.2	4.2	0.91
"	300A	"	150-300	5200	<300	1.5	1.2	4.2	1.55
SIEMENS	B2-B470	Spark gap	470	3565	<200	1.50	1.50	4.70	0.84
"	B2-H25	"	2500	3660	<200	1.50	1.45	5.15	0.96
"	B1-C90	"	90	2875	<100	1.50	1.45	4.55	0.51
"	KA6	"	6500-9500	10350	<1400	2.10	>23	>23	49.7
"	B1-A350	"	350	3140	<200	1.45	1.45	4.60	0.65
"	B1-A230	"	230	3025	<150	1.40	1.50	4.30	0.55
"	B1-F90	"	90	2820	<100	1.45	1.50	4.25	0.46
"	B2-B800	"	800	5895	<400	1.40	1.50	4.60	2.32
"	B1-C145	"	145	3385	<100	1.65	1.40	4.90	0.71
"	B2-H10	"	1000	3485	<200	1.50	1.50	5.40	0.91

cont'd

Table 6.8 (cont'd) Voltage Overshoot for Each Commercial Device that Survived all 50 nsec Pulse Tests. (Corresponding Energy Leakages into a 50 Ω Load are Also Shown). [6.11]

Mfr	Type	Description	V_B	Peak Voltage (V)	Clamp Voltage (V)	Rise Time (nsec)	Dwell Time (nsec)	Width (nsec)	Energy Leakage (mJ)
JOSLYN	2001-06	Miniature spark gap	230	3210	<200	1.30	1.10	3.85	0.58
"	2001-07	"	350	3025	<200	1.30	1.20	3.80	0.51
"	2001-08	"	470	3160	<200	1.40	1.20	4.20	0.61
"	2001-09	"	800	3270	<300	1.40	1.10	4.00	0.68
"	2001-31	"	230	4350	<200	1.40	1.20	3.30	0.90
DALE	LA9A1A/300V	Preionized spark gap	300	3590	<250	1.35	1.05	4.00	0.78
"	LA9A1A/400V	"	400	4150	<250	1.45	1.35	4.15	0.84
"	LA9A1A/500V	"	500	3380	<250	1.50	1.35	4.65	0.78
"	LA9A1A/750V	"	750	4305	<450	1.80	1.10	4.15	1.32
"	LA9A1A/1000V	"	1000	4665	<400	1.65	1.25	4.15	1.42
EG&G	GP-57-6	"	6000	10400	<750	3.80	>7.50	>14.5	18.8
"	GP-64-4.9	"	4900	8820	<500	3.80	>3.80	>10.8	11.4



RISE TIME $= t_1$

DWELL TIME $= t_2 - t_1$

WIDTH $= t_3$

PULSE DURATION $= \tau$

V_p = PEAK OVERSHOOT VOLTAGE

V_c = CLAMP VOLTAGE OR ARC VOLTAGE

Figure 6.32 Response Time and Overshoot Parameters for Terminal Protection Devices [6.11]

in series or parallel. These devices operating in a monopolar mode have exceptional junction response times (picosecond time regime). However, operating in the bipolar mode the response times are considerably less (greater than a nanosecond). In any case, the junction breakdown response time is not the response time of the clamping device. The actual clamping time is dominated by the internal inductance and lead inductance of device. The TPD response time can be considerably lengthened if the lead lengths are much greater than an inch.

The ability of semiconductor devices to handle large power surges requires large semiconductor junction surface areas. The large junction surface area gives the device an inherent capacitance which correlates to insertion losses in high frequency applications. High frequency insertion losses can be minimized by placing a low capacitance diode in series with the zener diode. However, the low capacitance diode must be able to handle the current that is expected to be shunted through the device.

Figure 6.34 shows the characteristic I-V curve for a single diode. B_{VR} is the reverse breakdown voltage, and the maximum forward voltage is on the order of 6 V. The I-V curve for two diodes in opposed series (Fig.6.35) shows that this configuration can utilize the reverse breakdown voltage of these diodes as a voltage limiter for a bipolar EMP signal. Zener diodes, which are specially designed to operate in the reverse breakdown mode, can be used effectively as

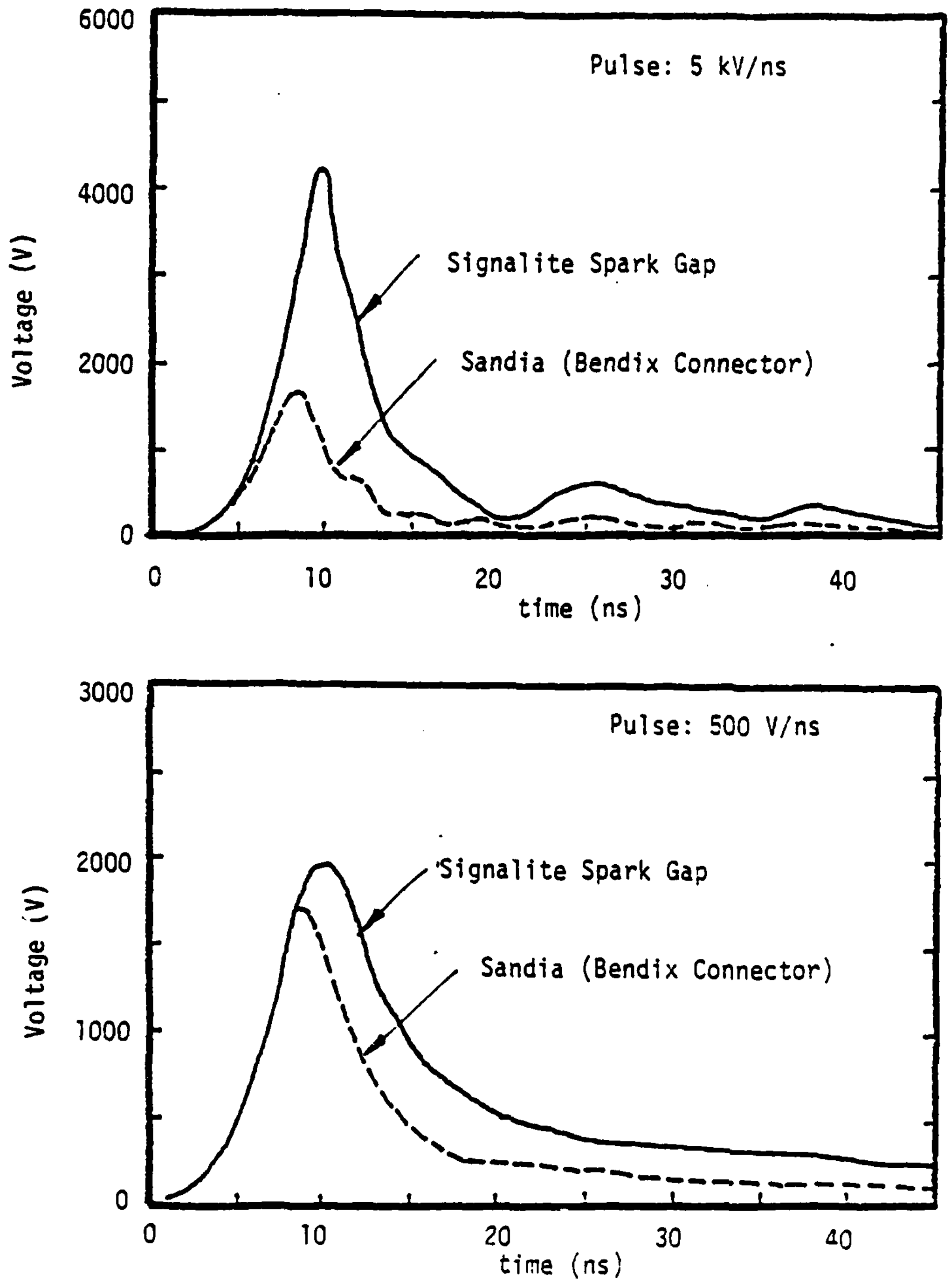


Figure 6.33 Comparison of Breakdown Properties for Dielectric Breakdown Device (Sandia) and Conventional Spark Gap (Signalite). [6.13]

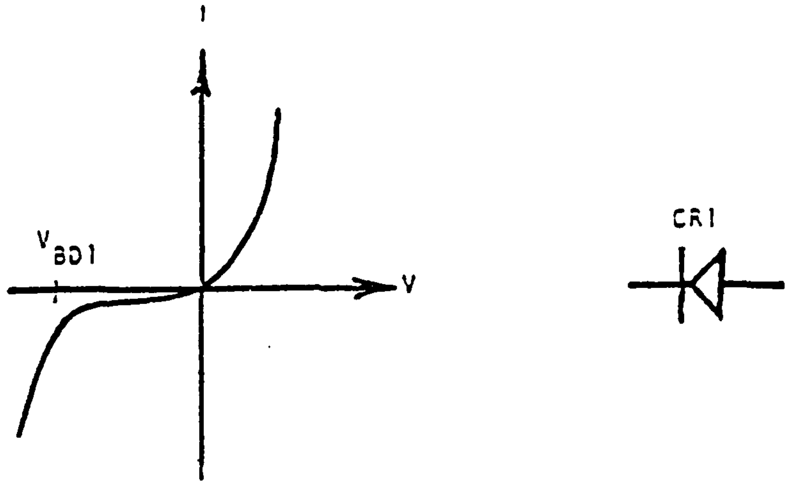


Figure 6.34 Single Diode V-I Characteristic Curve [6.8]

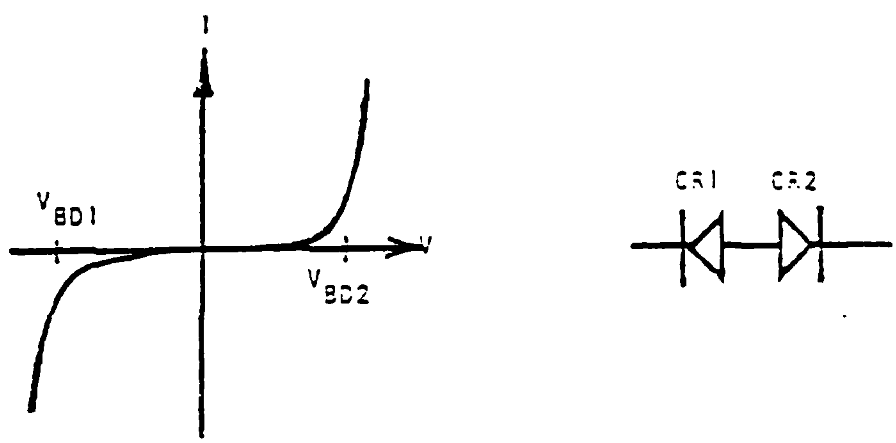


Figure 6.35 V-I Characteristics for Opposed Series Diodes [6.8]

TPDs. Figure 6.36 illustrates some of the TPD configurations involving diodes. Part (a) illustrates a low signal level TPD which limits the threat voltage to one diode drop. Part (b) shows a stacked opposed parallel pair; the forward characteristics of the diodes are the limiting factors. Parts (c) and (d) illustrate opposed series zener configurations. Configurations (a) and (b) will probably withstand more power dissipation than (c) and (d), because the former configuration utilizes the forward diode drop, which is less damage susceptible than the reverse bias mode. Configurations (b) and (d) have the advantage of reducing the TPD capacitance to less than that of one pn junction [6.8].

Diode pulse power vulnerability can be calculated with the aid of (5.1).

Reference 6.8 presents test data on several types of single junction semicc ductor devices. Twelve different types of zener diodes and one signal diod were evaluated. These devices covered breakdown potentials from 6 to 100 v and power ratings from .5 to 50 watts.

Nine types of TransZorbs* were also evaluated. The TransZorb is a specially packaged (hermetically sealed glass-to-metal) semiconductor breakdown device capable of handling large power surges which was developed by General Semiconductor Industries in conjunction with Harry Diamond Laboratory. Four series types of TransZorbs were tested. The 5500 and 5600 series TransZorbs are defined as silicon transient suppressors designed to protect voltage-sensitive components in airborne systems. The GHV series TransZorbs are much lower in shunt capacitance and, therefore, permit applications across analog and digital input circuitry with minimum insertion loss. The ICT-5 TransZorb is specially designed for protection of 5 volt IC logic circuits.

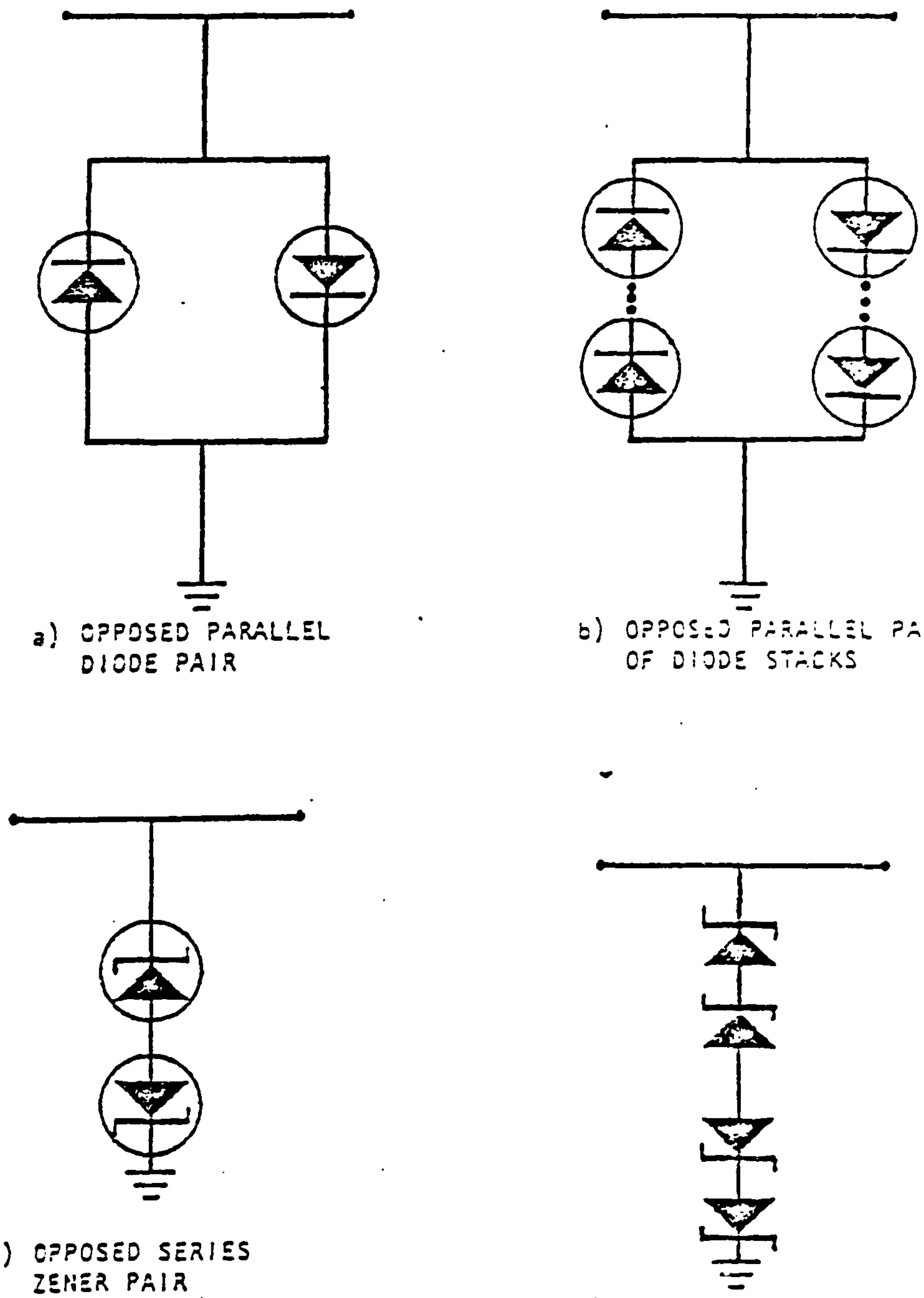
At least three samples of each diode type were evaluated during each parameter measurement.

Figure 6.37 gives the V-I characteristics for several of the diodes tested. Table 6.9 is a summary of the test results on the device parameters. Equation (6.2) can be used to obtain F_{3db} from C_T for any circuit configuration. The protective efficiency was measured according to (6.8). The pulse power columns, which refer to the pulse energy in the pulser, do not indicate the power dissipated in the TPD, because some power is reflected. As noted, some of the TPDs did not fail.

References 6.10 and 6.11 present test data on several semiconductor devices. The characteristics of the devices tested in Reference 6.10 are presented in Table 6.10. Tests of semiconductor devices [6.11] which clearly demonstrate that the theoretical junction response time advertised by manufacturers on the order of a picosecond for monopolar zeners is in fact much less than the response of the actual semiconductor device. Results are shown in Table 6.11.

Figure 6.38 shows several application areas of semiconductor breakdown devices. Note Figures 6.39(e) and (i) where a single monopolar TPD is used to protect a bipolar signal line. This is generally accomplished by use of the fast recovery diode bridge. Test results [6.15, 6.16] have demonstrated the EMP

*General Semiconductor Trade Name



a) OPPOSED PARALLEL DIODE PAIR

b) OPPOSED PARALLEL PAIR OF DIODE STACKS

c) OPPOSED SERIES ZENER PAIR

d) OPPOSED SERIES ZENER STACKS

Figure 6.36 Basic Diode TPD Configurations [6.8]

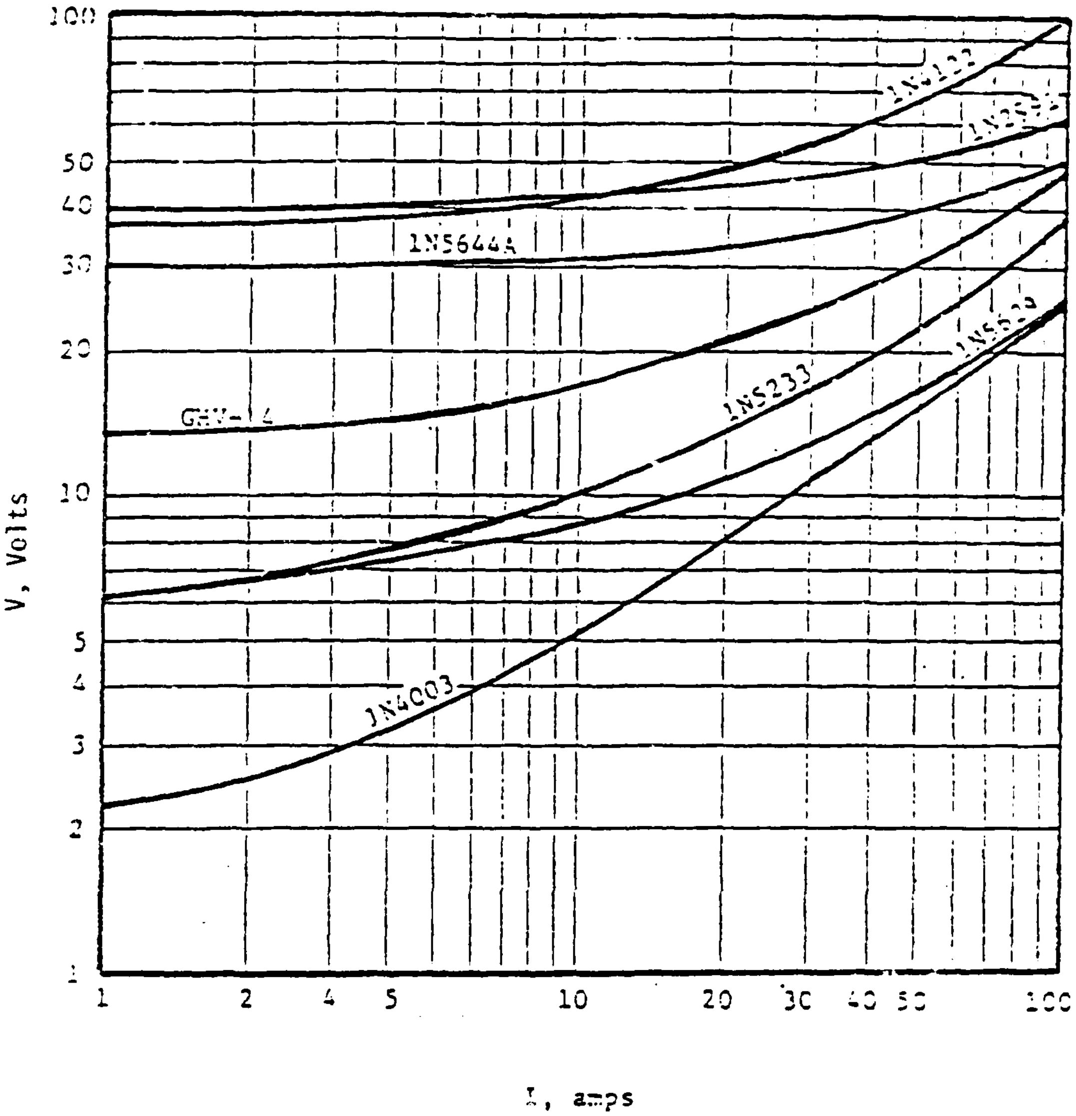


Figure 6.37 V-I Characteristic Curves for Some Zener Diodes, TransZorbs and a 1N4003 Rectifier [6.8]

Table 6.9 Semiconductor TPD Parameter Matrix [6.8]

Device Family	Device Type	Specified V_{BD} Volts	Average Measured V_{BD} Volts	Specified P_{DISS} Watts	Maximum No Fail Pulse Current, Amps	Maximum Pulser Output No Fail Energy Joules	Minimum Pulser Output Energy to Fail, Joules	Avg C_T, pF	Voltage at 10 Amps Volts	Protective Efficiency η
Transzorbs	1N5555	33	34	1	157	24.2	26.8	2154 pF	-	8.05
	1N5558	191	200	1	219	.07	.93	409 pF	-	3.15
	1N5629A	6.5-7.1	6.6	1	800	162	-	14892 pF	9	4.31
	1N5630A	7.1-7.9	7.7	1	800	162	-	9621 pF	-	6.1
	1N5644A	28.5-31.5	28.5	1	430	34.3	37.3	2460 pF	31	2.8
	1N5648A	40.9-45.2	43.4	1	235	11.9	13.3	1909 pF	-	8.68
	CT-5	6	6.6	1	680	162	-	15062 pF	-	9.1
	GHV-8	5.4	5.4	1	800	162	-	89 pF	-	3.48
	GHV-14	9.4	9.3	1	800	162	-	51 pF	17	3.59
Diodes	1N2042-2	6	5.6	10	400	29.5	30.9	5267 pF	-	105
	1N2828	100	98	50	56	.9	1.6	957 pF	-	3.42
	1N2980	16	15.5	10	355	25.9	26.8	2603 pF	-	22.6
	1N2991	36	36.5	10	205	9.3	11	1159 pF	43	13.9
	1N3321	24	22	50	507	52.1	55.7	3683 pF	-	7.3
	1N3794	16	15.6	1.5	130	3.6	4.9	960 pF	-	11.5
	1N3798	24	24.9	1.5	320	1.4	15.4	669 pF	-	6.13
	1N4122	36	37.5	.25	80	.14	.16	134 pF	42	3.64
	1N5233	6	5.7	.5	153	.39	.42	557 pF	10	19.7
	1N5359	24	23.3	5	105	2.3	3.2	640 pF	-	13.9
	1N5365	36	36.7	5	293	1.34	1.4	423 pF	-	12.8
	1N5378	100	89	5	147	.39	.42	216 pF	-	1.3
	1N4003 F/R	-	.4/563.4	-	680/2.3	91/.04	104/.05	53 pF	7	1060/-

Table 6.10 Semiconductor TPD Characteristics [6.8]

Part Number	Vendor	Maximum Operating Voltage (Volts)	Impulse Breakdown Voltage (Volts)	Pulse Power/ Energy Rating	Weight	Approximate Dimensions Diameter (In.)		Approximate Dimensions Length (In.)	MIL Approved
ICT-5	Gen. Semiconductor	5	8.5	>>100 kw	1.5 gm	0.220		0.350	No
1.5K36	Gen. Semiconductor	29	52	>>100 kw	1.5 gm	0.220		0.350	Yes, MIL-S-19500
1.5K150	Gen. Semiconductor	121	215	>>100 kw	1.5 gm	0.220		0.350	Yes, MIL-S-19500
1.5K200	Gen. Semiconductor	162	297	>>100 kw	1.5 gm	0.220		0.350	Yes, MIL-S-19500
						Width	Height	Length	
704-15K36	Gen. Semiconductor	31	51	>1 mw	NS	0.750	2.0	0.5	Yes, MIL-STD-7044
60KS200C	Gen. Semiconductor	180	335	>1 mw	NS	1.30	2.24	0.5	Yes, MIL-STD-1399
1.5K6.8	Gen. Semiconductor	5.5	10.8	>>100 kw	1.5 gm	0.220		0.350	Yes, MIL-S-19500
704-56A	Gen. Semiconductor	49	70	>>100 kw	NS	NS		NS	NS
UZ 5806	Unitrode	6.8	6.0	>>100 kw	NS	0.145		0.230	No
UZ 5212	Unitrode	120	120	>>100 kw	NS	0.145		0.230	No
UZ 5240	Unitrode	400	400	>>100 kw	NS	0.145		0.230	No
GA300A	Unitrode	60	60	>>100 kw	NS	0.225		0.705	No
GA301	Unitrode	100	100	>>100 kw	NS	0.437		1.097	No
S25.6	Shauer	5.6	5.6	NS	NS	0.160		0.44	No
S216.0	Shauer	16.0	16.0	NS	NS	0.160		0.44	No
.416.8	Sarkes Tarzian	6.8	6.8	1 w **	NS	0.105		0.300	No
.4133	Sarkes Tarzian	33	33	1 w **	NS	0.105		0.300	No
11A200	Sarkes Tarzian	200	200	1w **	NS	0.105		0.300	No
.41200	Sarkes Tarzian	200	200	1 w **	NS	0.105		0.300	No

NS = Not specified on data sheet

**Maximum steady state dissipation.

Table 6.11 Voltage Overshoot Parameters for Each Commercial Device that Survived All 50 nsec Pulse Tests. (Corresponding Energy Leakages into a 50 Ω Load are also Shown) [6.11]

Mfr	Type	Description	V_B	Peak Voltage (V)	Clamp Voltage (V)	Rise Time (nsec)	Dwell Time (nsec)	Width (nsec)	Energy Leakage (mJ)
DALE	LVP-6/6.2V	Avalanche diode	6.2	2355	<100	1.30	1.65	4.40	0.32
"	LVP-6/7.5V	"	7.5	2820	<100	1.40	1.50	4.40	0.47
"	LVP-6/9.1V	"	9.1	2050	<100	1.40	1.60	4.15	0.24
"	LVP-6/13V	"	13	2560	<100	1.65	1.20	3.90	0.37
GSI	1N5017	"	7.5	2615	<100	1.65	1.25	4.45	0.43
"	1N5020	"	10	2205	<100	1.50	1.45	4.50	0.30
"	1N5042	"	50	2565	<200	1.55	1.50	4.45	0.43
"	1N5344B	"	8.2	2155	<100	1.50	1.50	4.50	0.29
"	1N5369B	"	51	2155	<200	1.50	1.55	4.50	0.32
MOTOROLA	1N1518	"	3.9	2260	<150	1.55	1.30	4.60	0.35
"	1N1523	"	10	2025	<100	1.65	1.50	4.65	0.28
"	1N1802	"	200	2560	<200	1.75	1.90	5.45	0.51
"	1N1788	"	51	1995	<300	1.40	1.55	5.50	0.38
"	1N1785	"	39	2250	<250	1.50	1.60	4.80	0.38
UNITRODE	UZ8810	Avalanche diode	10	2805	<300	1.50	1.35	4.50	0.55

GSI stands for General Semiconductor Industries
See Figure 6.32 for Response Time Legend

TYPICAL TRANSZORB APPLICATIONS

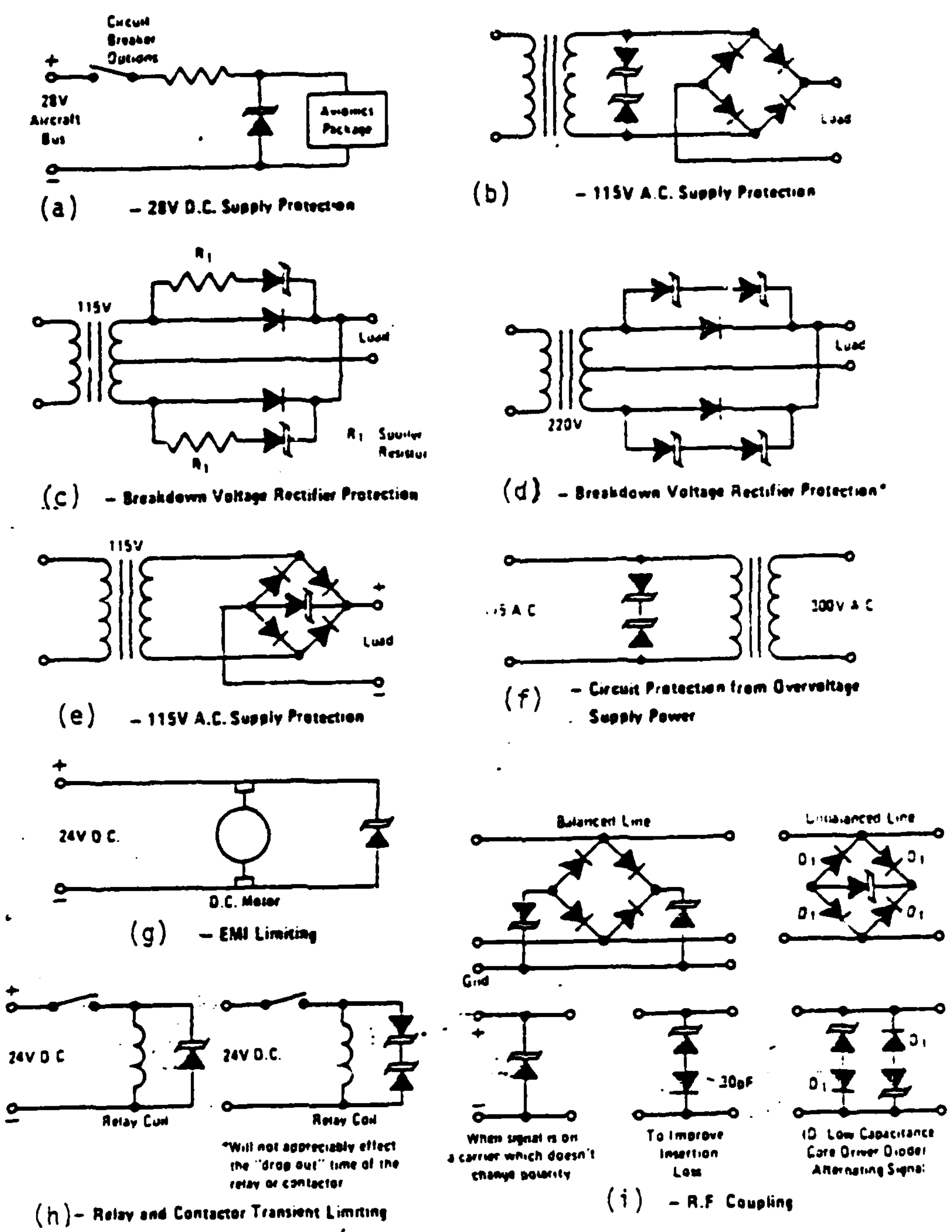


Figure 6.38 Application Areas of Semiconductor Breakdown Devices [6.14]

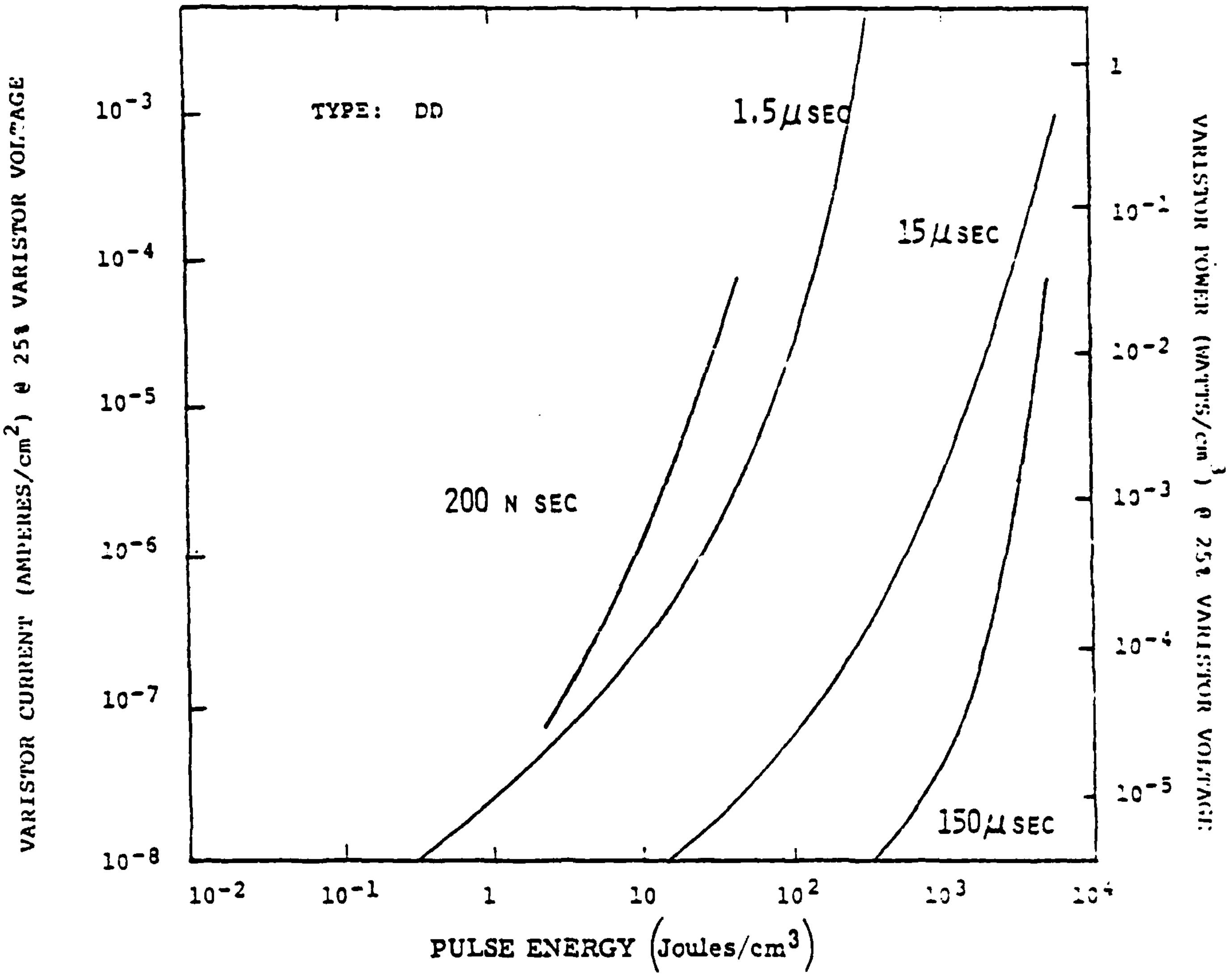


Figure 6.39 Typical Energy-Time Damage Characteristics of Type DD GE-MOV™ Varistor Material [6.18]

protection afforded by using this technique. An additional benefit of using this technique is that the TPD insertion loss can be reduced for application in protecting high frequency signal lines [6.15].

6.3.4 Nonlinear Resistors (Varistors)

Nonlinear resistors are devices that obey the current-voltage relationship

$$I = KV^N, \tag{6.7}$$

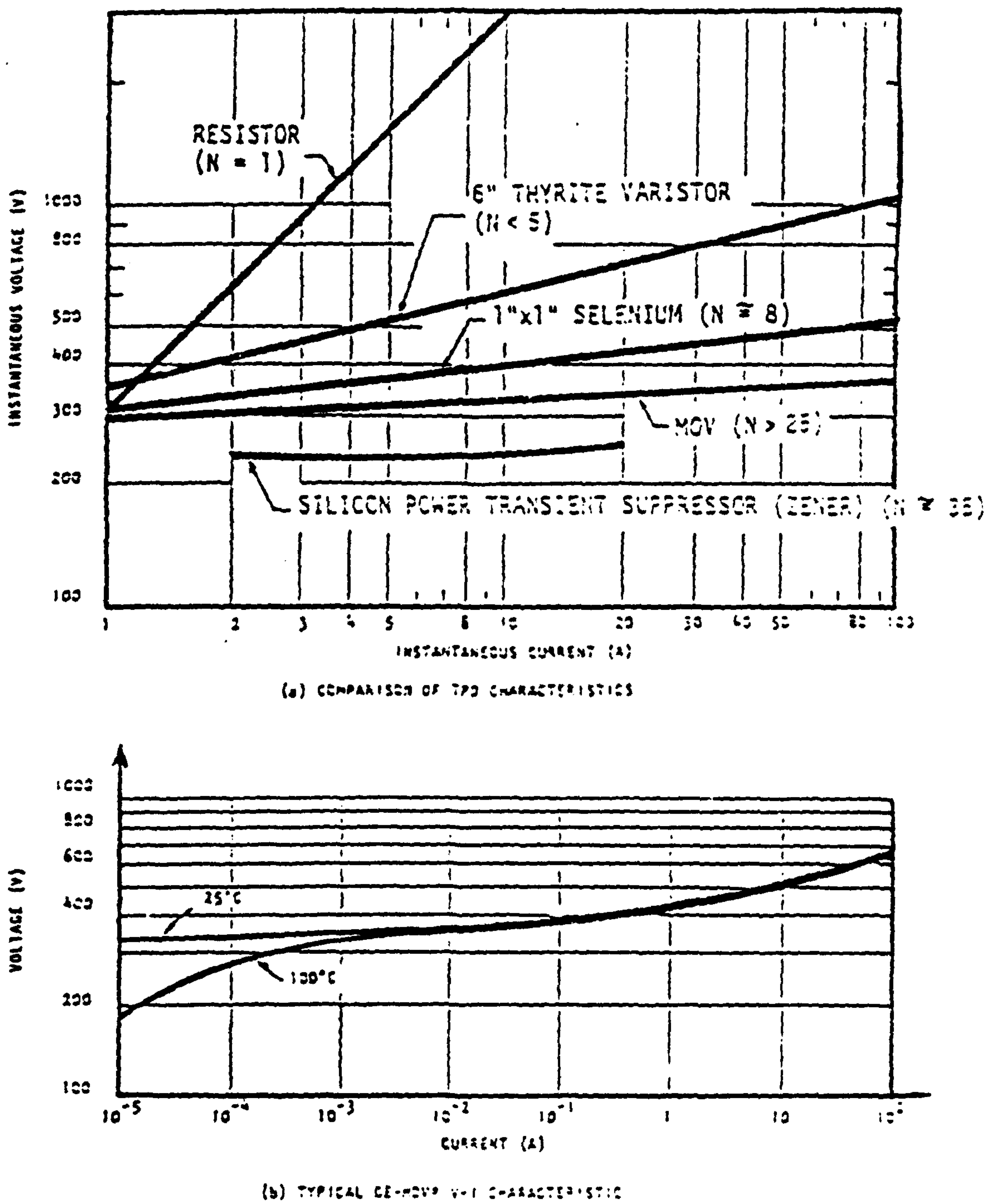
where N and K are device constants which depend on the varistor material. Varistors can be made out of many materials. "Thyrite" is a G.E. trade name for its silicon carbide type varistor. Selenium and certain metal oxides (mainly ZnO and Bi_2O_3) are also used. The G.E. trade name for its metal oxide varistor is MOV. For fast EMP transients, the MOVs are superior because of their fast response time. The others are slower, but have higher energy handling capabilities. These devices are bipolar.

The composition of metal oxide varistors consists of metal oxides which are sintered at high temperature to produce a polycrystalline ceramic body [6.17]. The structure of the body is a matrix of conductive metal oxide grains separated by a highly resistive intergranular boundary. It is the intergranular boundary that gives the metal oxide varistor its nonlinear behavior. These boundaries are distributed throughout the volume. This allows the varistor to uniformly dissipate energy making the varistor energy rating volume dependent. Thus, metal oxide varistors are capable of handling larger power surges.

The metal oxide varistor also exhibits an inherent capacitance due to intergranular boundary separation of the conductive grains. The capacitance of the device is typically greater than 1000 pf. Thus, the metal oxide varistor finds direct application in low frequency and DC circuit protection.

Excessive heating of the metal oxide varistor caused by prolonged or repeated power surges degrades the device [6.18]. The data in Figure 6.39 is an attempt to characterize the degradation of the type "DD" material as a function of pulse duration. Here is shown the typical increase in leakage current and standby power at a specific bias voltage as a function of input pulse energy for four different pulse widths. In this case, the bias voltage is again taken at 25% of the "varistor voltage". Here, the permanent damage tests were performed using high energy critically damped pulse waveshapes with pulse times of 30 nanoseconds, 3 microseconds and 30 microseconds to peak pulse output. As can be seen from Figure 6.39, the absorbed pulse energy density required for significant leakage current increase ranges from 10 to 1000 joules per cubic centimeter depending upon the pulse width. It should be noted from Figure 6.39 that the apparent degradation as a function of pulse width is generally what would be expected for a thermal damage mechanism, similar to that in semiconductor devices. For the GE-MOV™ varistor, however, the energy required for significant degradation is at least an order of magnitude higher than that to cause catastrophic damage in junction devices when compared on an equal area basis.

Figure 6.40 shows the V-I characteristics of several kinds of varistors [6.4]. Part (a) also shows a linear resistor ($N = 1$) and a reverse biased zener diode for comparison.



*TRADEMARK OF THE GENERAL ELECTRIC COMPANY

Figure 6.40 TPD V-I Characteristics [6.4]

Figures 6.41 and 6.42 illustrate varistor configurations. Here the material is used to isolate a center conductor from an outside conductor because of the high varistor resistance. If the voltage increases, the resistance would decrease and short the two conductors [6.2].

Figure 6.43 presents a comparison of the V-I curves of some varistor and dielectric breakdown devices.

Reference 6.8 gives some test data on five models of MOVs and Table 6.12 presents a summary of the test results. None of these devices failed. The pulser energy refers to the energy in the pulser and not that dissipated in the device. The protective efficiency is that defined in (6.6). F_{3db} can be found from (6.2) for a given set of source and load impedances.

Reference 6.10 presents test data on several varistors. A summary of the varistors tested in Reference 6.10 and some of the device characteristics are shown in Table 6.13.

6.3.5 Hybrid TPDs

Sometimes TPDs may be combined to give improved protection [6.4]. However, this results in a more complex, costly, and less reliable system which may be difficult to evaluate [6.19].

It is desirable to combine the individual TPDs so that the best features of each device are utilized. Figure 6.44(a) through (d) illustrates the use of dielectric breakdown devices to shunt the major portion of the EMP transients followed by semiconductor breakdown devices (or varistors) to clip the residual portion of the voltage transient. And as discussed earlier, low capacitance diodes can be used in conjunction with zener diodes (Figure 6.45(a)) to reduce their insertion loss.

Combinations of linear and nonlinear TPDs are also useful in circuit protection. An example is the use of filters to reflect or dissipate the bulk of the EMP transient outside the normal operating frequency band followed by a low power nonlinear device to clip the residual voltage transient. Or, a high power nonlinear device can be used to shunt the bulk of the transient energy to ground followed by filters to "clean up" the residual transient.

As can be seen from the discussion above, the combinations are numerous and detailed and it is not within the scope of this handbook to discuss all the possible combinations in detail. Rather, the purpose of this subsection is to point out some of the design considerations to be taken into account when constructing hybrid TPDs and their possible limitations.

The use of dielectric breakdown devices (spark gaps) in a hybrid TPD has associated with it uncertainties in the amount of energy leakage. This residual energy can cause the secondary TPDs to fail. Another aspect of using dielectric breakdown devices in hybrid TPDs is that it is desirable to have the spark gap which can handle large power surges fire first thus preventing most of the transient energy from reaching secondary TPD elements which may not handle as much power. It is then necessary to add either delay lines (Figure 6.46(a)) or a series inductor (Figure 6.46(b) and (c)) to provide this isolation. Resistors can also be used in place of inductors to provide isolation [6.22].

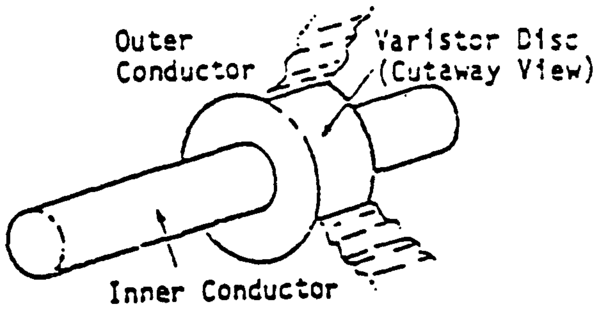


Figure 6.41 Varistor Protective Device
[6.2]

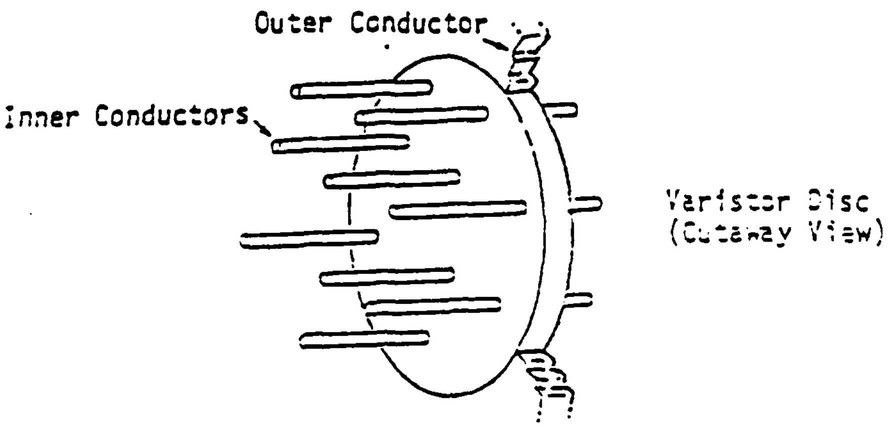


Figure 6.42 Alternate Geometry for Varistor Protection
[6.2]

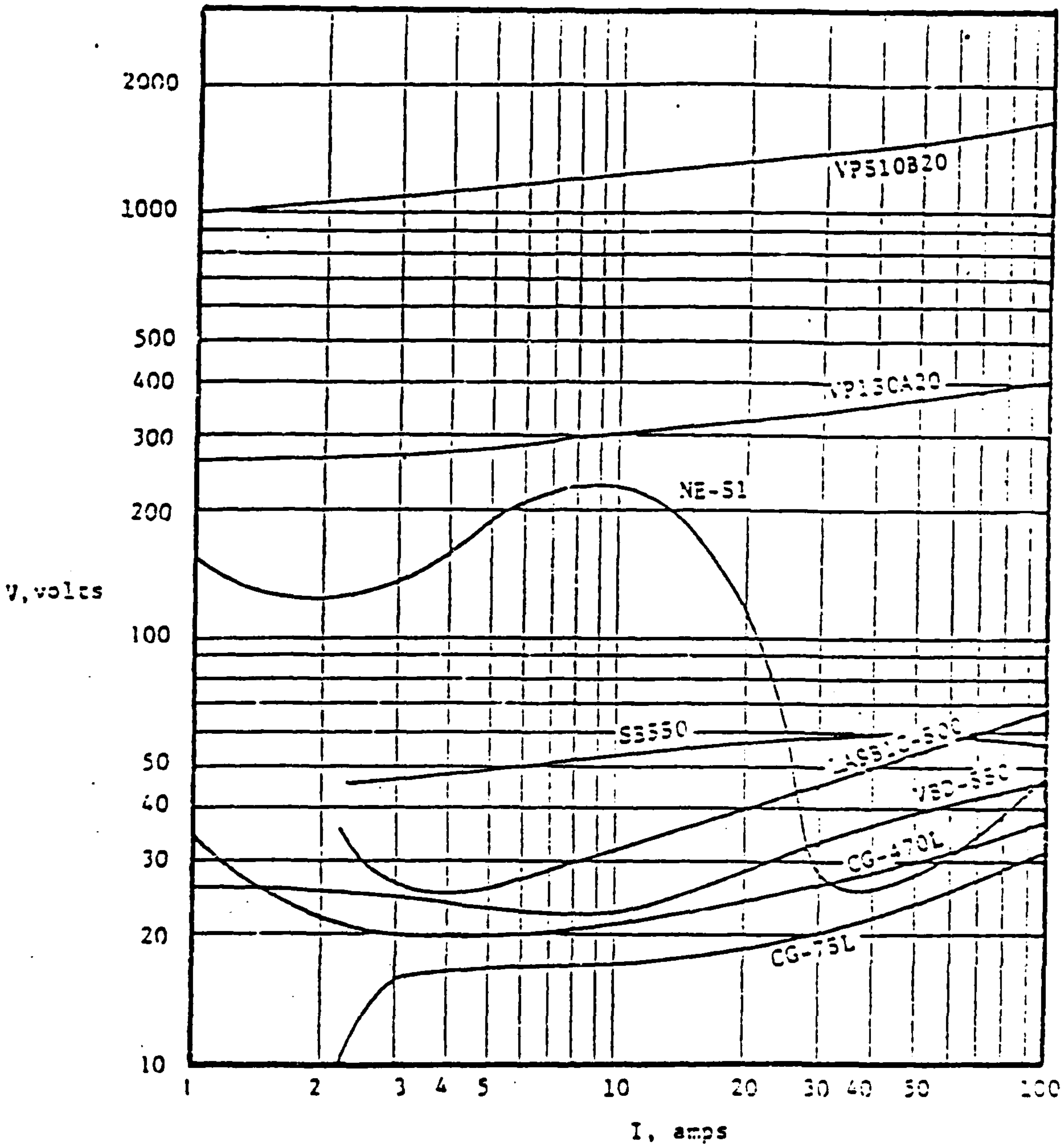


Figure 6.43 V-I Characteristic Curves for Some MOVs
Dielectric Breakdown TPDs [6.8]

Table 6.12 Varistor Parameter Matrix [6.8]

Device Family	Device Type	Specified V_{BD} Volts	Average Measured V_{BD} Volts	Specified P_{DISS} Watts	Maximum No Fail Pulse Current, Amps	Maximum Pulser Output Energy To Fail, Joules	Minimum Pulser Output Energy To Fail, Joules	Avg C_T, pF or V_A @ T_A = 10 ns	Voltage at 10 Amps Volts	Protective Efficiency
MOV'S	VP130A20	185	202	.05	827	162	-	1403 pF	300	.26
	VP150A20	211	225	.05	847	162	-	1191 pF	-	.31
	VP510B20	720	825	.7	647	162	-	167 pF	1250	.02
	VP510B40	720	837	.7	680	162	-	157 pF	-	.02
	VP1000B160	1410	1400	1.3	570	162	-	189 pF	-	.006

Table 6.13 Varistor Characteristics [6.10]

Part Number	Vendor	Maximum Operating Voltage (Volts)	Impulse Breakdown Voltage (Volts)	Pulse Power/ Energy Rating (Joules)	Weight	Approximate Dimensions Diameter (In.)	Approximate Dimensions Length (In.)	MIL Approved
VP510B40	General Electric	510	721	40	NS	0.760	0.75	No
VP1[illegible]A10	General Electric	130	184	10	NS	0.760	0.25	No
VP420B40	General Electric	420	595	40	NS	1.032	0.75	No
VP250A40	General Electric	250	354	40	NS	1.032	0.30	No
VP150A10	General Electric	150	212	10	NS	0.760	0.25	No
6[illegible]R2100	National Lead	1000	NS	NS	NS	0.28	1.12	No
6[illegible]2100	National Lead	540	NS	NS	NS	.0.28	1.12	No
7[illegible]R[illegible]0	National Lead	275	NS	NS	NS	0.28	1.12	No

NS - not specified on data sheet

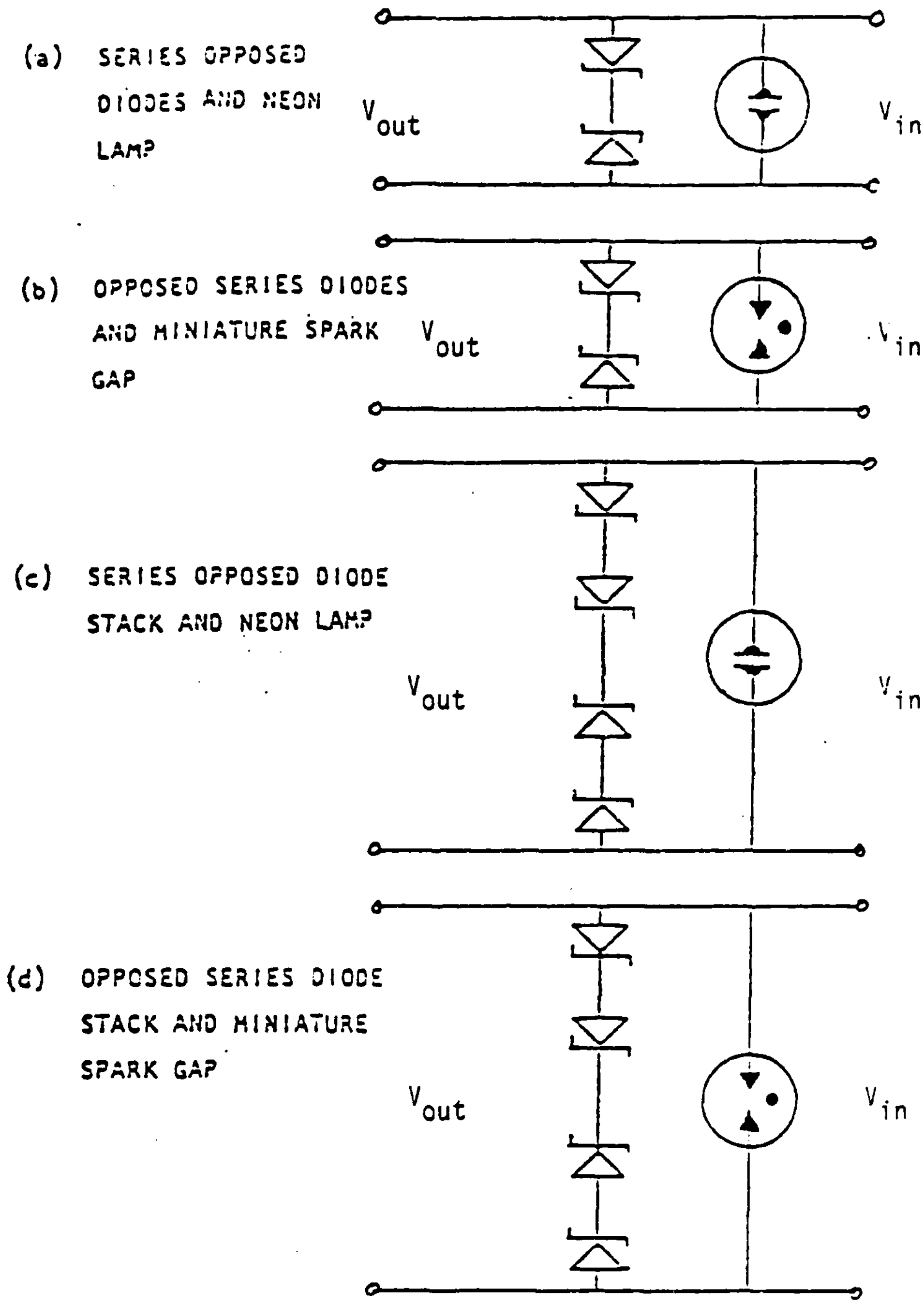


Figure 6.44 Terminal Protection Networks [6.19]

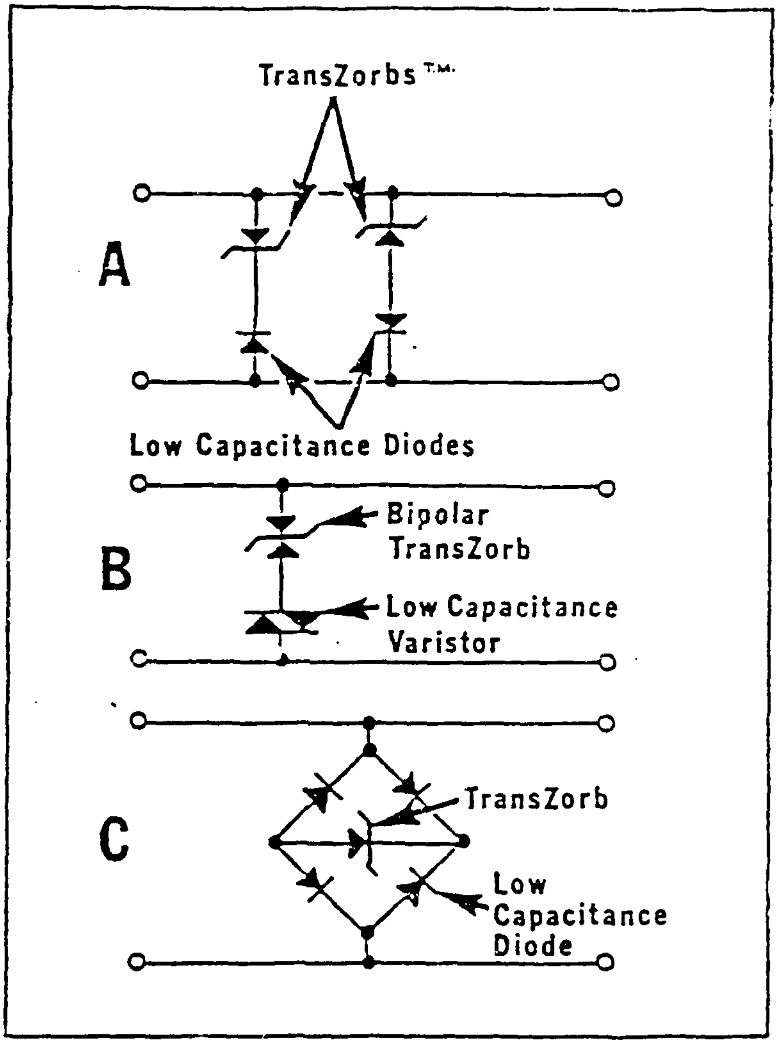
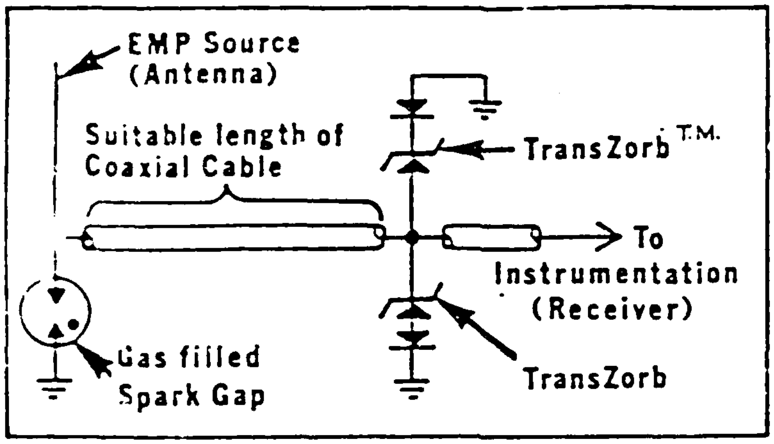
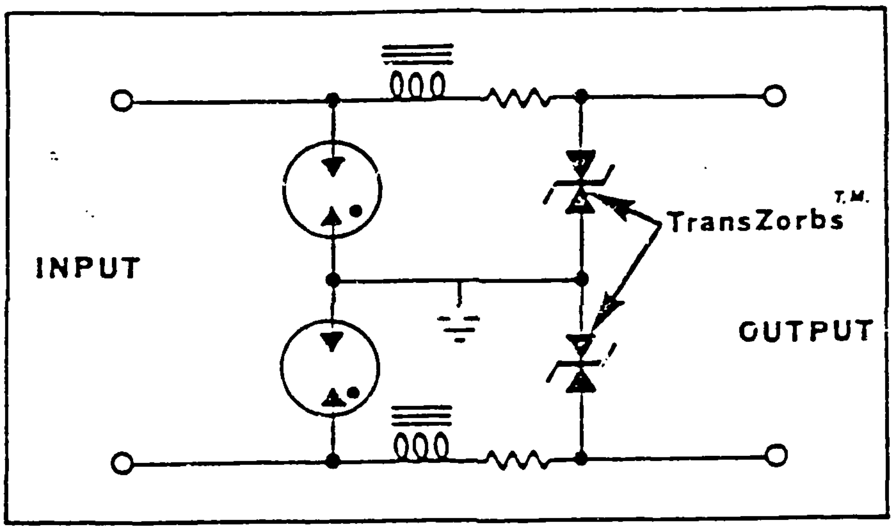


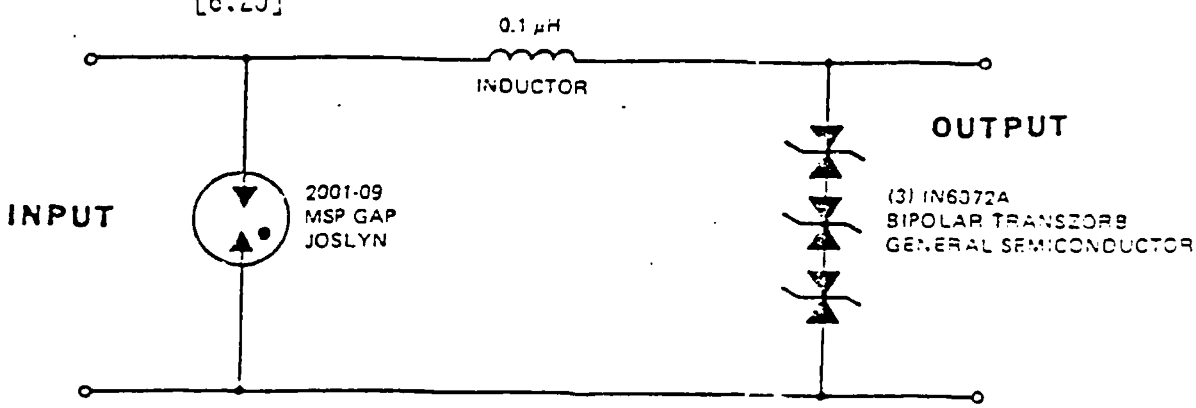
Figure 6.45 Capacitance Reduction Circuits [6.20]



(a) Cable Isolation Protection Circuit [6.20]



(b) Inductor Isolation Protection Circuit (Pat.#3, 934, 175)
[6.20]



(c) Inductor Isolation [6.21]

Figure 6.46 Use of Delay Lines and Inductors to Isolate Hybrid TPD Elements

When constructing hybrid TPDs it is always important to keep the lead lengths of the TPD as short as possible [6.23].

6.3.6 Other TPDs

Other transient suppression devices available are diode AC switches (DIACs), crowbars, biased suppressors, silicon-controlled rectifiers (SCRs), thyristors, and PIN diodes. Most are of limited use for varying reasons [6.11]. For example, some cannot handle the power of typical EMP transients, some require gate control (see Table 6.1), and some do not respond fast enough to EMP transients.

6.3.7 TPD Summary

All of the devices mentioned here have potential use in EMP hardening schemes. Reference 6.10 lists several TPD disadvantages, which are summarized in the following paragraphs.

All TPDs reflect a large percentage of incident energy and thus could increase system threat at other locations. If TPDs are used on both terminals of a wire, the reflections may cause the transient to last much longer than normal. The nonlinear devices will significantly alter the threat frequency spectrum in a rather unpredictable manner. If nonlinear devices are used extensively, system modeling becomes complex, CW data cannot be used, and low-level tests would be invalid. In that TPDs are tied directly across lines, the semiconductor types that fail by short circuiting may decrease system reliability.

TPDs should be used after a thorough analysis of impact on system performance. It is less desirable to use TPDs in locations internal to a system because of the reflection and nonlinear properties discussed above. The most desirable application of TPDs is at external locations, such as receiver antennas and external cabling, where reflection of incident energy does not present a large problem.

Table 6.14 is a summary TPD functional selection matrix, which should aid in the selection of a TPD device for a specific application [6.4].

6.3.8 General Installation Practices of TPDs

Several examples of preferred TPD installation practices are found in Reference 6.1. A basic overview of the installation guidelines follows.

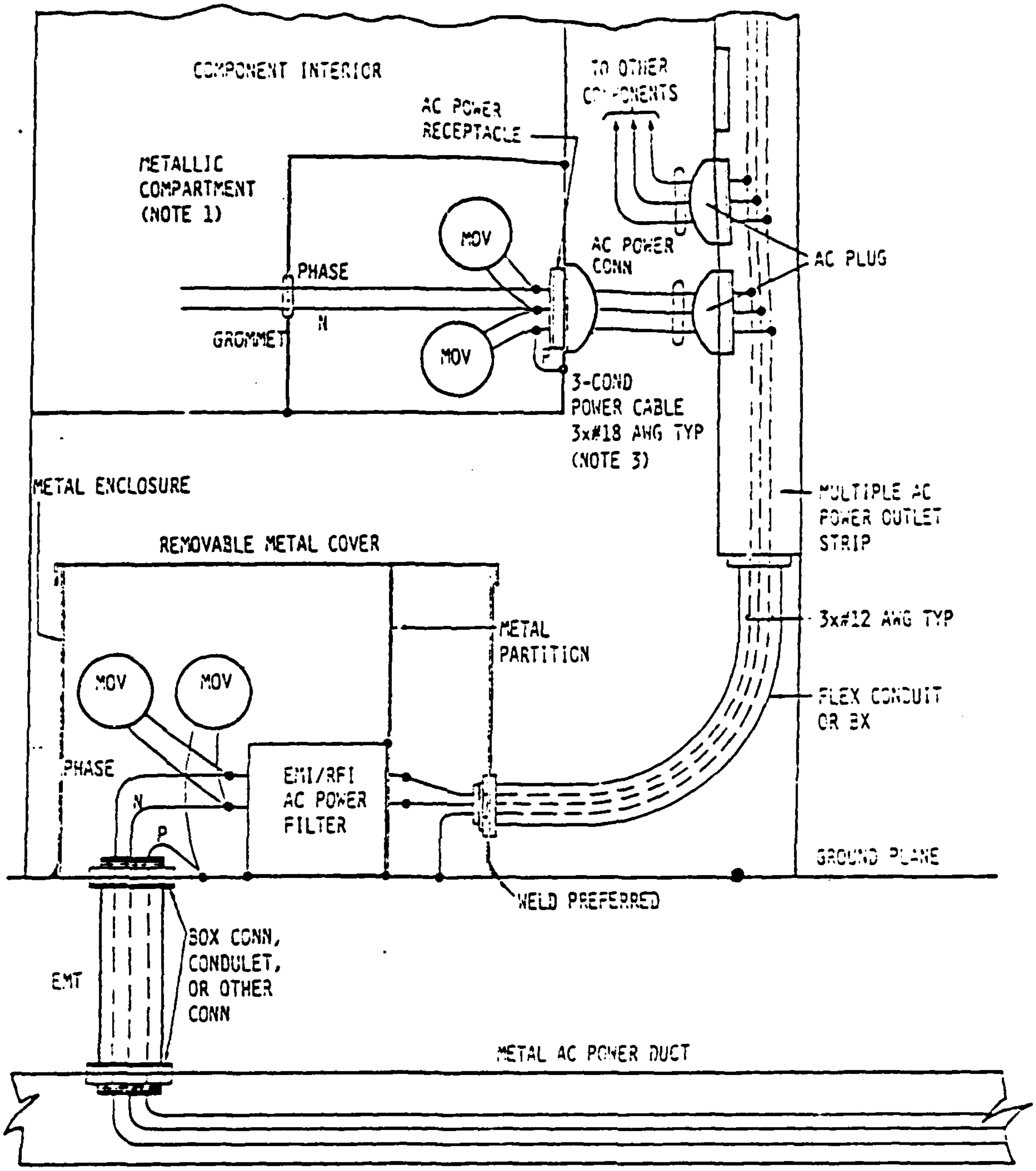
1) TPDs should be installed such that the shunt currents do not flow into the shielded volume. This is usually accomplished through the use of an entry vault (metal enclosure) which houses the TPDs (Figure 6.47). Thus, currents shunted from unhardened exterior cables will flow through the TPD and out on the exterior of the shielded volume (i.e. equipment rack or hardened cable). By allowing the currents to flow on the exterior of the protected volumes, further coupling of the EMP transients to sensitive equipment is minimized.

2) To reduce the coupling between cables in the entry vault, it is recommended that the power lines be separated or shielded from the signal lines. This would also reduce EMI (electromagnetic interference) during normal operation of the equipment.

Table 6.14 TPD Functional Selection Matrix [6.4]

Voltage Range (Volts)	Energy Throughput Load (mJ) 1 50 ohm	Maximum Frequency for 1 dB Insertion Loss (MHz) 1 10 100 1000	Time to Device Turn on (tB)
0.1 to 1.0	0.01–0.1 0.1–1.0 1.0–10.0	OPD OPP	2–4 ns. 4–40 ns.
1.0 to 6.0	0.01–0.1 0.1–1.0 1.0–10.0	OPDS	6–10 ns.
6.0 to 43	0.01–0.1 0.1–1.0	OSD SPEC OSD OSDS	2–6 ns. 2–6 ns.
43 to 90	0.01–0.1 0.1–1.0 1.0–10.0	SPEC COMB	2–3 ns. 2–6 ns.
90 to 1000	0.01–0.1 0.1–1.0 1.0–10.0	MSG NEL MOV	2–3 ns. 3–10 ns. 3–6 ns.

NOTE: OPD – Opposed Parallel Diodes
OPP – Opposed Parallel PIN Diodes
OPDS – Opposed Parallel Diode Stacks
OSD – Opposed Series Diodes
MSG – Miniature Spark Gaps
SPEC – Special Terminal Protection Devices
COMB – Combinations
MOV – Metal Oxide Varistors
NEL – Neon Lamps
OSDS – Opposed Series Diode Stacks
– – – – New Areas of Protection



NOTES:

1. THE COMPARTMENT CAN ALSO BE FASTENED TO THE OUTSIDE OF THE COMPONENT ENCLOSURE.
2. ROUTE AC POWER CABLES AWAY FROM SIGNAL, CONTROL, AND DC POWER CABLES.
3. SHIELDED CABLES ARE REQUIRED IF THE SITE HOUSING PROVIDES LITTLE OR NO ATTENUATION.

Figure 6.47 Example of Equipment AC (and DC) Power Hardening Method [6.1]

3) The lead lengths on TPDs should be as short as possible. If possible, leadless TPDs should be used. This makes the TPDs more effective.

6.4 Use of Protective Devices at Non-Antenna Interfaces

6.4.1 Introduction

Because of the variety of circuitry associated with interface pins, it is nearly impossible to address each possible protection measure for all circuits. It is more appropriate to give examples of generic circuits that have been hardened to illustrate the TPD selection technique. Thus in the subsections to follow, the use of TPDs to protect the following circuits is presented:

1) Signal Lines (subsection 6.4.2),
2) Digital Logic Circuits (subsections 6.4.3), and
3) Power Lines (subsection 6.4.4).

The examples should aid the design engineer in choosing satisfactory TPDs for protecting non-antenna interfaces. These examples should serve as a guide but they should not be considered the only protection measures available.

The TPD chosen to protect the non-antenna interface should adequately perform the following functions:

1) Protect the circuit from the current/voltage transients specified in Section 2.4.3.2,

2) The protection measure should not interfere with the normal operation of the equipment in the absence of an EMP event, and

3) The TPD should not fail during repeated pulses thus allowing the interface hardening method to be tested according to Section 9.3.2.1.

The TPD that satisfactorily conforms to these criteria will harden sensitive circuitry in an EMP environment according to Section 2.4.

Figures 6.48 and 6.49 show the decision process for determining the need and selection criteria for TPDs. The exact TPD selected is principally determined by the power handling capability, turn on time, and insertion loss. Table 6.14 can be used as a guide in TPD selection.

6.4.2 Signal Line Protection

Signal lines consist of control, command, and communications (C^3) links between rooms on the ship. The routing of cables between these rooms is then subject to the environments specified in Section 2.4.

An example of the TPD use and selection criteria are illustrated in References 6.21 and 6.24, where the susceptible inter-equipment signal cables on the AN/SRC-16 system are analyzed for the following peak threat conditions which occur over the frequency range from about 0.5 MHz to 10 MHz:

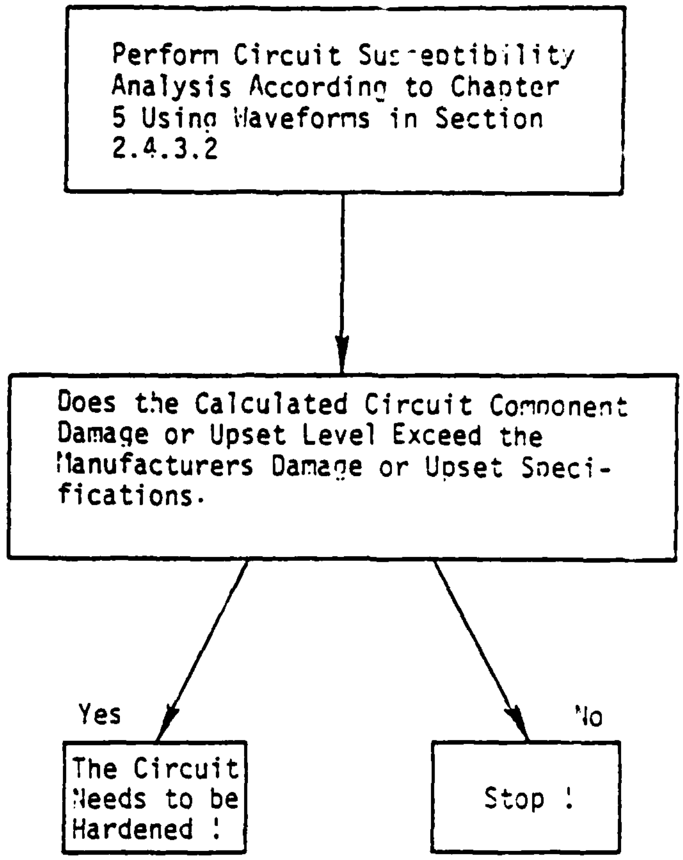


Figure 6.43 Flowchart to Determine if the Circuit Needs to be Hardened

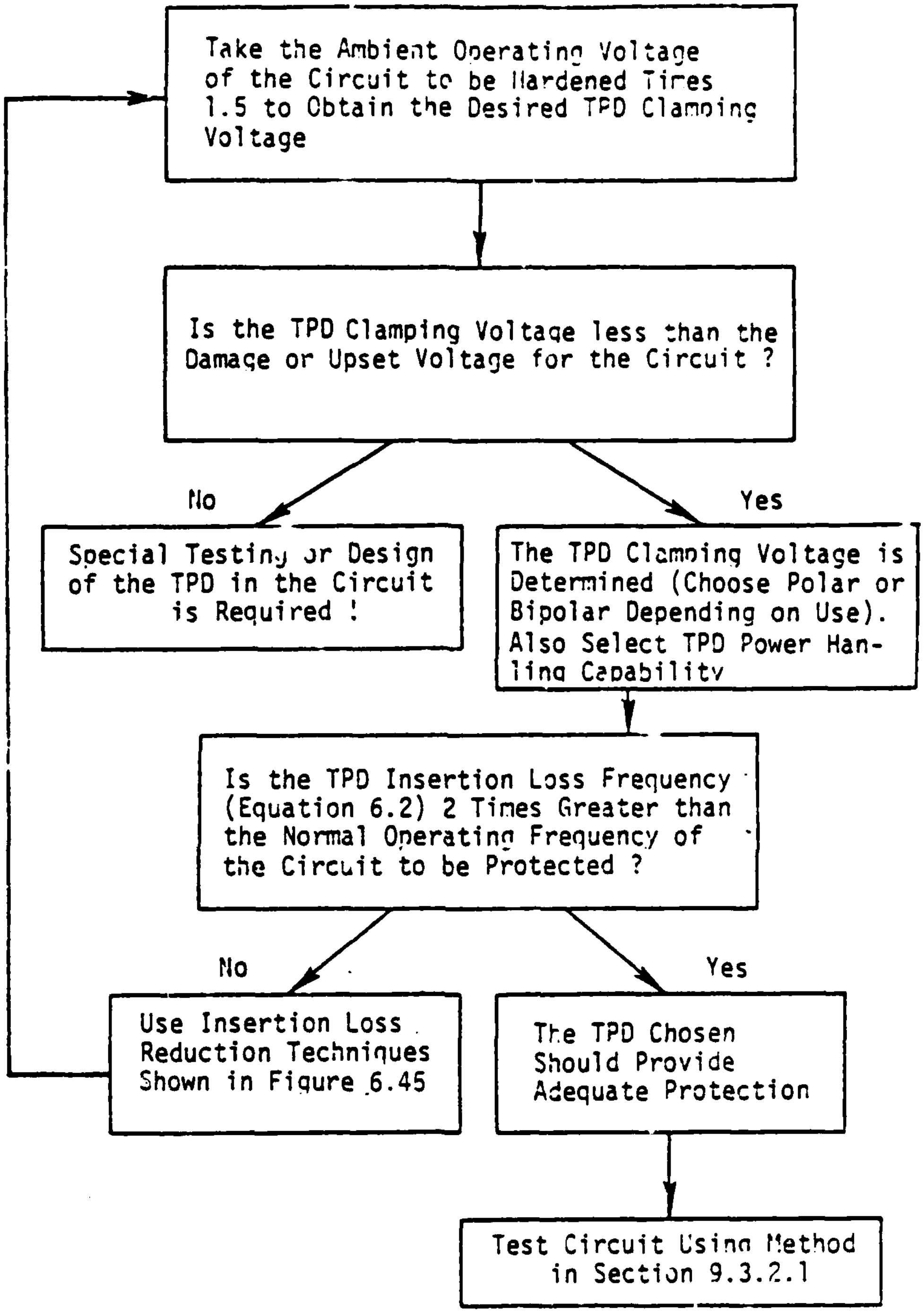


Figure 6.49 Flowchart to Determine the TPD to be Used in the Susceptible Circuit

$V_{P\ max}$	1000 V
$I_{P\ max}$	10 A
$P_{P\ max}$	10 kW.

The only equipment which is vulnerable to the EMP interface pin threat is the Receiver Overload Protector (ROP) subassemblies, (Figure 6.50). Capacitors C1, C2, C4 and C7 have 500 volt ratings and diode CR1-1N3070 has a peak inverse voltage rating of 200 V. The ROP is designed such that 10 volts of rf signal will turn on transistors Q1 and Q2, and turn off Q3. Relay K1 then becomes de-energized, grounding the receiver fault line and opening the signal line to the receiver; thereby protecting the components within the ROP as well as the receiver. In the event that the ROP did not respond in time to limit the EMP transient, the diode CR1-3070 could be overstressed by exceeding the peak inverse voltage of 200 volts. EMP protection should therefore be provided for the ROP in addition to the built-in over voltage circuit. Although the capacitors have a 500 volt rating, parts procured to a military specification are normally tested to 200% of the maximum voltage rating. The capacitors should not be damaged by the 1000 volt pulse.

The TPD designed for use with the ROP subassemblies should meet the following general requirements:

- The TPD should not significantly degrade the signal lines.
- It must sufficiently suppress EMP transients to prevent damage or malfunction of the ROP.
- It must be capable of withstanding multiple transients without degradation.

The TPD must also be capable of meeting the electrical requirements given in Table 6.15 to insure normal operation of the circuit.

A TPD was designed for protecting the ROP to comply with the requirements given in Table 6.15. The device is designated as TPD-Model 3. A schematic diagram of the device is shown in Figure 6.51.

Two important characteristics of TPDs installed in a signal line are the stand-by mode and the protection mode characteristics. In the standby mode the breakdown voltage, V_{BD}, the shunt capacitance, C_T, and the 3 dB cutoff frequency, f_{3dB}, are important parameters.

In the protection mode the DC breakdown voltage, V_{BD-DC}, impulse breakdown voltage, V_{BD-IMP}, holdover voltage, V_{HO}, and the surge current rating, I_{SURGE}, are important. Parametric values for these characteristics are given in Table 6.16. In the standby mode the V_{BD} is 50 volts which is well above the circuit operating voltage of 7 volts. The capacitance C_T largely controls the f_{3dB} point, the frequency at which the signal falls off about 50 .

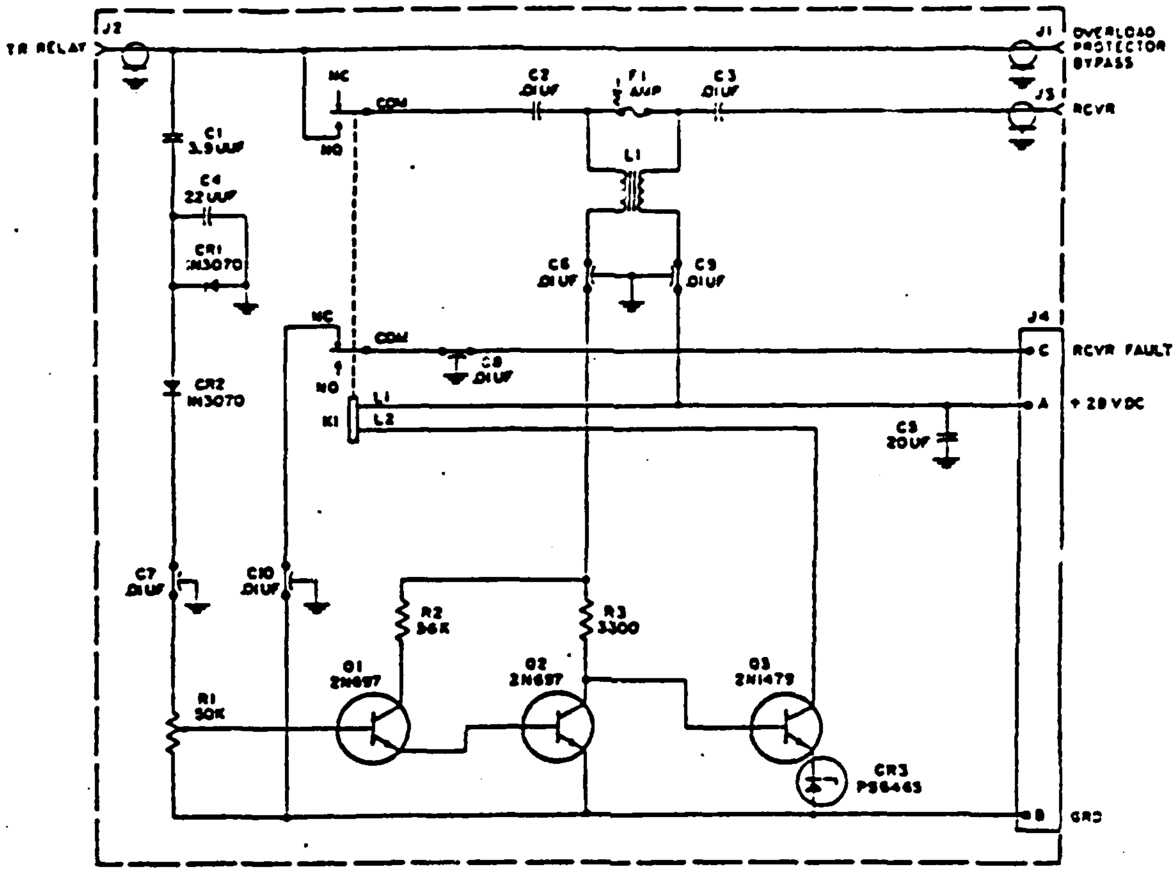
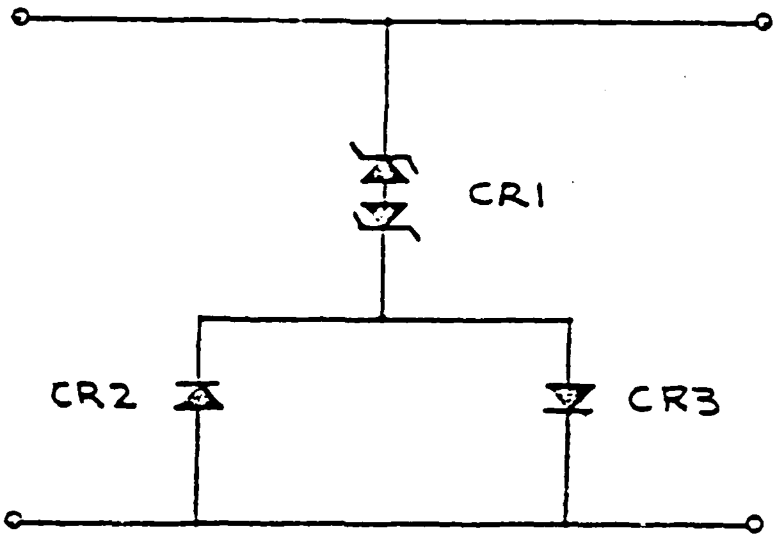


Figure 6.50 Receiver Overload Protector Subassemblies A1A3 and A1A4, Schematic Diagram [6.21]

Table 6.15 TPD Electrical Requirements for the ROP [6.21]

P_p max	10 kW for 1 µsec
I_p max	10 A
$V_{BREAKDOWN}$	50 to 60 volts
Frequency Range	2 to 30 MHz
Capacitance (at standoff voltage)	80 pF max
Resistance (below breakdown)	1 megohm



CR1 - 1N6160 Bipolar Silicon Transient Suppressor, Semtech

CR2, CR3 - FF05 Fast Recovery Diode, Semtech

Figure 6.51 TPD Model 3, Schematic Diagram [6.21]

Because the maximum signal frequency is 30 MHz, a f_{3dB} of 265 MHz would not deteriorate the signal. The f_{3dB} was calculated from (6.2), where R_s and R_L are the source and load impedances, which are taken as 50 Ohms each for this determination. In the protection mode the breakdown, or limiting voltage of 50 volts will provide adequate protection for the ROP. The I_{SURGE} of 18.6 A provides adequate protection from the EMP threat level of 10 A.

The response time for the 1N-6160 devices is stated by the manufacturer to be less than 1×10^{-12} seconds, although in the bipolar mode is typically less than 5×10^{-9} seconds which affords good protection for the fast EMP transients.

The TPD model 3 for the ROP cable will be installed in the aluminum box and encapsulated with a silicone rubber compound in accordance with HAC SPEC. HP 16-61, Type I. The unit will be installed in the cable line between the ROP and the SIM/DUP and T/R relay.

Table 6.16 TPD - Model 3 Mode and Protection Mode Characteristics [6.16]

Characteristic	Parameter	Value
Standby mode		
	V_{BD}	50 volts
	C_T	24 pF
	f_{3dB}	265 MHz
Protection mode		
	V_{BD-DC}	50 volts
	V_{BD-IMP}	50 volts
	V_{HO}	50 volts
	I_{SURGE}	18.6 A, 1 msec

6.4.3 Digital Logic Circuit Protection

Digital logic circuits are a special class of signal lines that merit separate analysis. This is largely because of the low level signals common to the logic circuit. In addition, some digital circuitry now being used in operating near 1 gigabyte per second which requires special high frequency TPD. That is, TPDs with low insertion losses at high frequencies.

An example of TPDs being used to protect digital circuitry is given in References 6.16 and 6.24. Pictorial diagrams of two types of AN/UYQ-21 systems are shown in Figures 6.52 and 6.53. The Small Scale Tactical Display Subsystem consists of a Central Equipment Group, two Display consoles, a Remote Key Set, and data links to the Sensors and Computers. Included in the Central Equipment Group are:

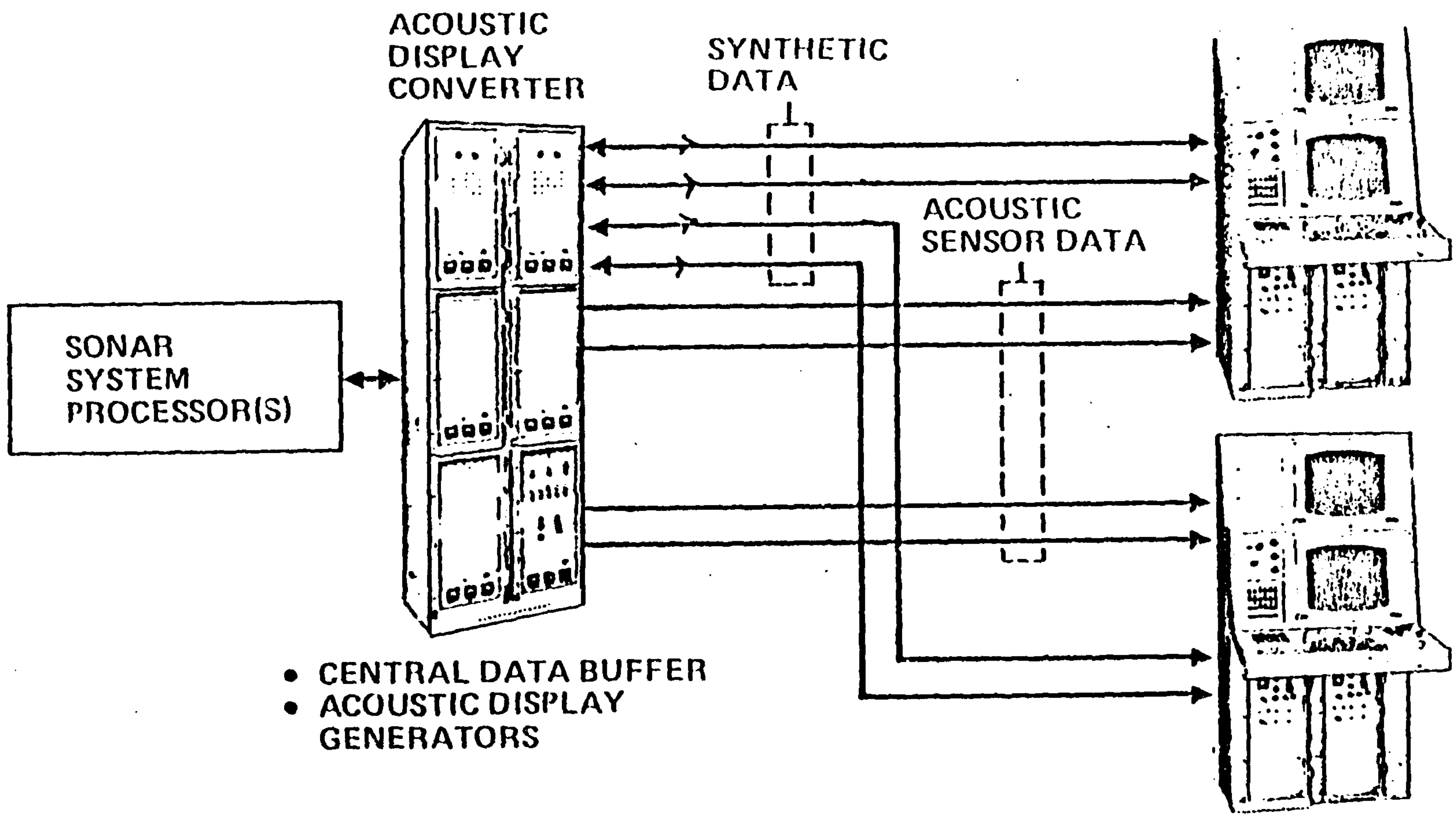


Figure 6.52 Acoustic Display Subsystem AN/UYQ-21, Pictorial Diagram [6.24]

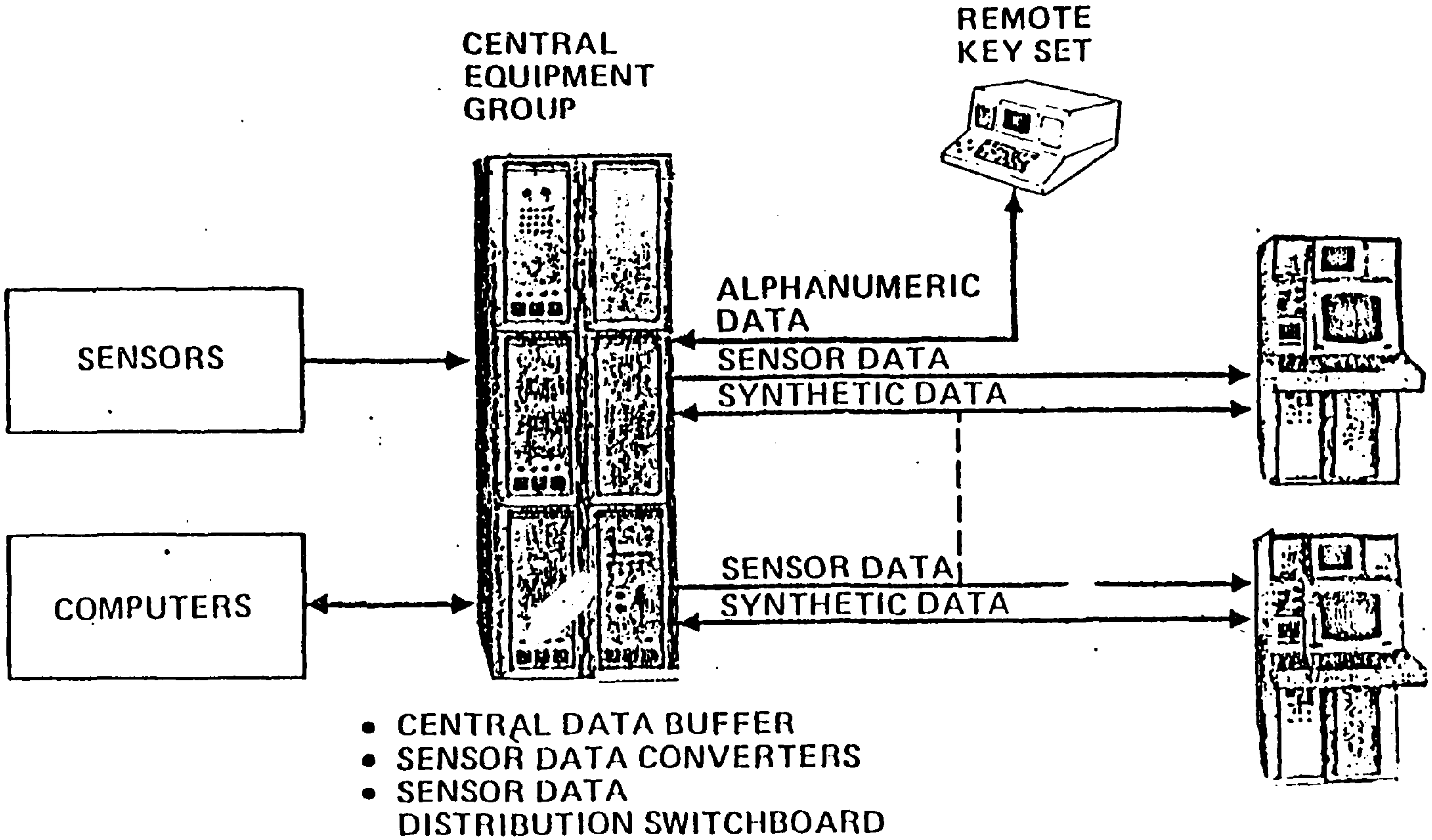


Figure 6.53 Tactical Display Subsystem AN/UYQ-21, Pictorial Diagram [6.24]

- Central Data Buffer
- Sensor Data Converters
- Sensor Data Distribution Switchboard.

Sensor data and synthetic or simulated data lines connect the Central Equipment Group and the Consoles.

The Acoustic Display Subsystem consists of an Acoustic Display Converter, two Display Consoles, and the Sonar System Processors. The Acoustic Display Converter includes the Central Data Buffer, and the Acoustic Display Generators. Sensor Data and synthetic data lines connect the consoles and the Display Converter.

The Data Display Group uses a total of 57 analog and 24 digital signals throughout the system. Part of the analog and digital data lines carry high speed signals.

The AN/UYQ-21 equipment performs a similar function to that of the AN-UYA-4 previously described. Descriptive information on the AN/UYQ-21 is limited since the equipment is in the development phase. Also, much of the signal information is classified and therefore cannot be discussed in this report.

The results of the damped sinusoidal pulse, Section 2.4.3.2, direct injection tests into the UYQ-21 simulated loads are shown in Figures 6.55 and 6.56. The tests were conducted at 1 MHz, 10 MHz, and 50 MHz without and with TPDs across the load.

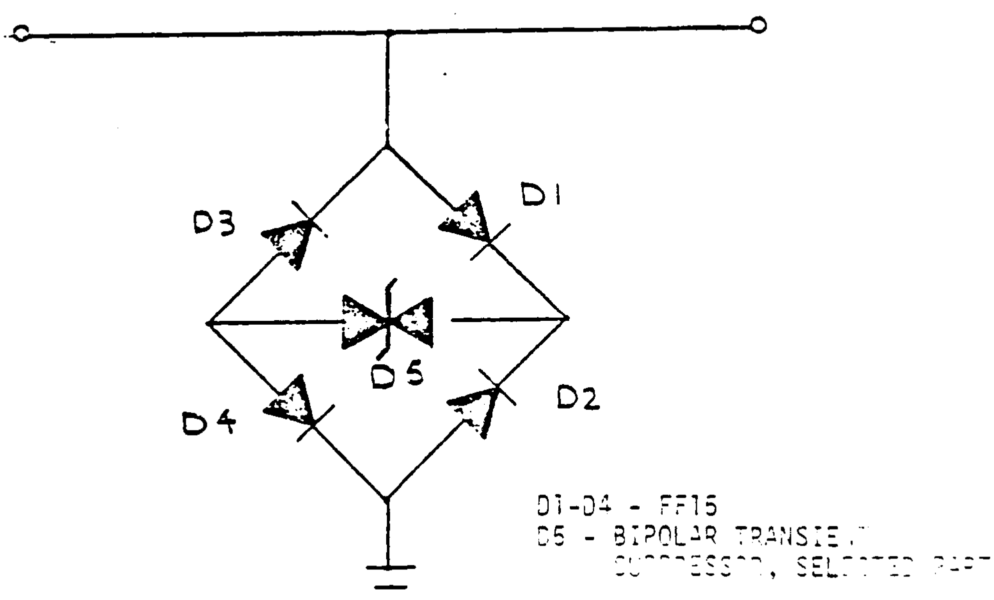


Figure 6.54 Schematic Diagram, TPD Diode Bridge for Use on UYQ-21 [6.16]

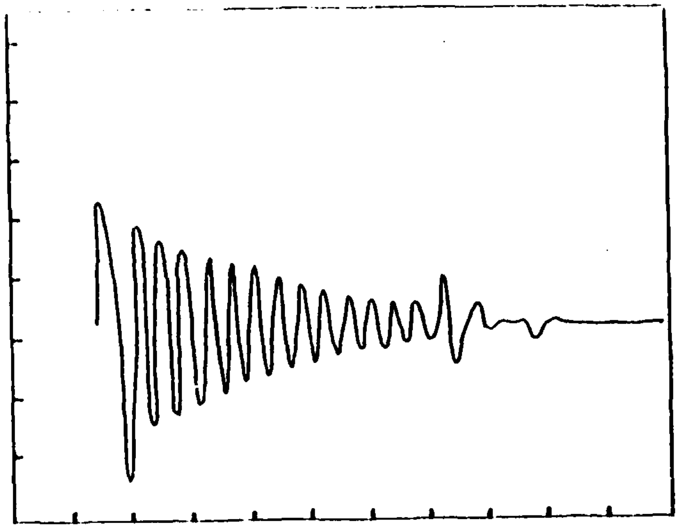


Figure 6.55a Load Current; 5A/DIV, 2μS/DIV.

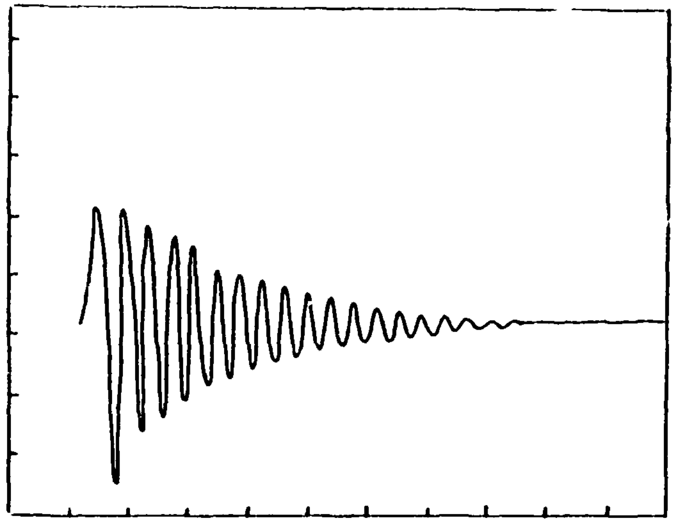


Figure 6.55b Load Voltage; 500 V/DIV, 2μS/DIV.

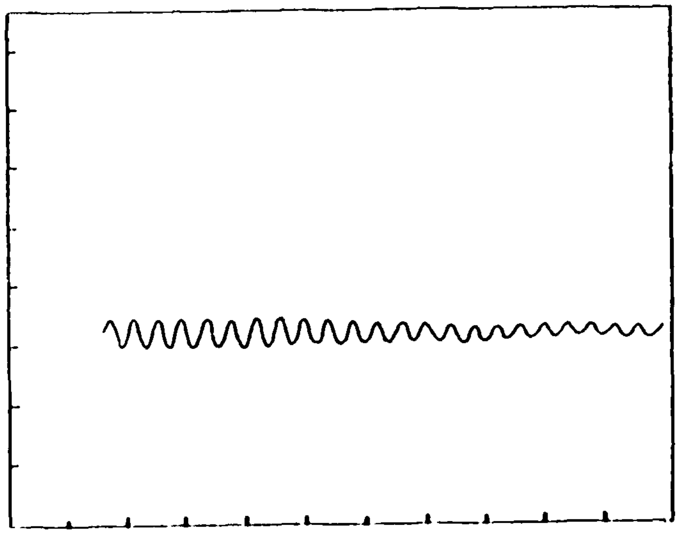


Figure 6.55c Load Current with L10A Diode Bridge; 5A/DIV, 2μS/DIV.

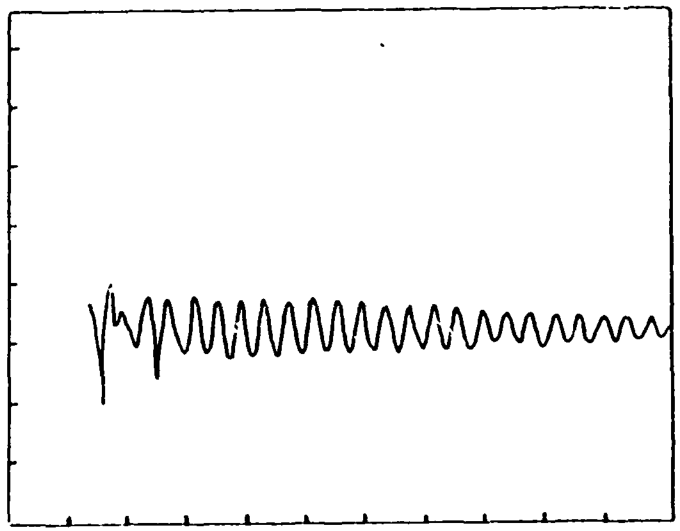


Figure 6.55d Load Voltage With L10A Diode Bridge; 200V/DIV, 2μS/DIV.

Figure 6.55a-d 1 MHz Damped Sinusoid Pulse (DSP) Directly Injected Across 100 Ohm Load [C.1?]

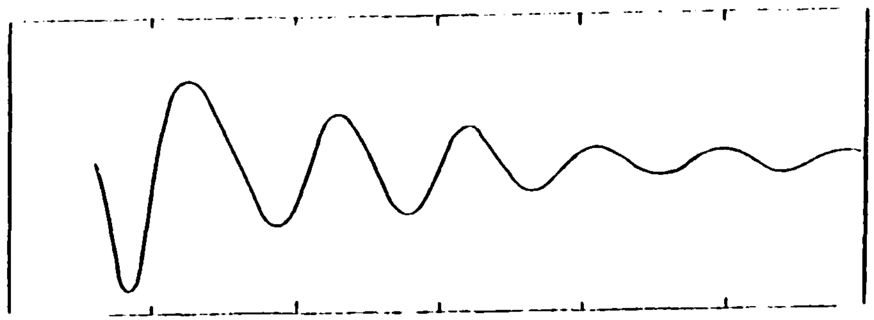


Figure 6.56a Load Voltage Across 100 Ohms; 1000 V/DIV, 100 NS/DIV.

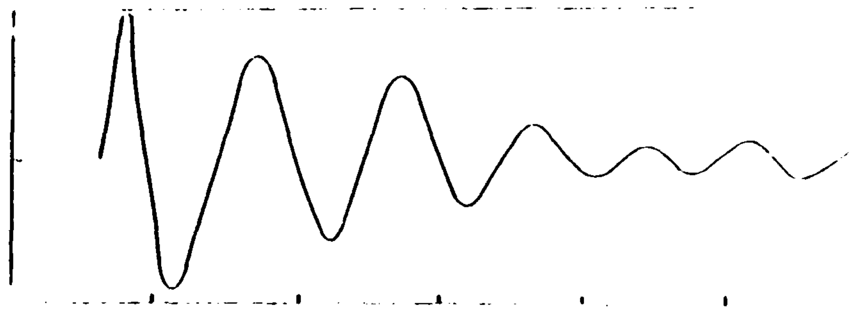


Figure 6.56b Load Current Into 100 Ohms; 10A/DIV, 100 NS/DIV.

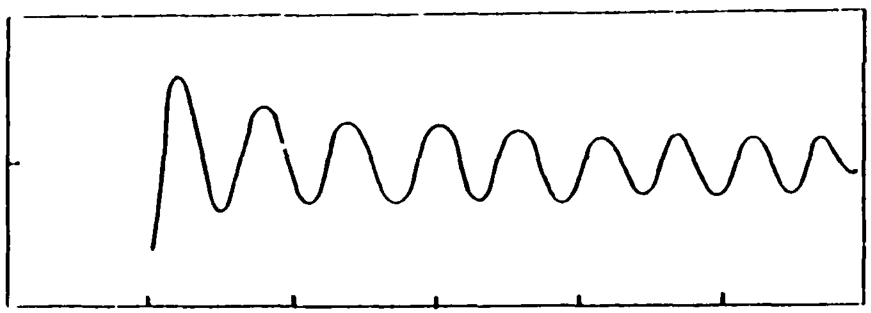


Figure 6.56c Load Voltage with L10A Diode Bridge; 100 V/DIV, 200 NS/DIV.

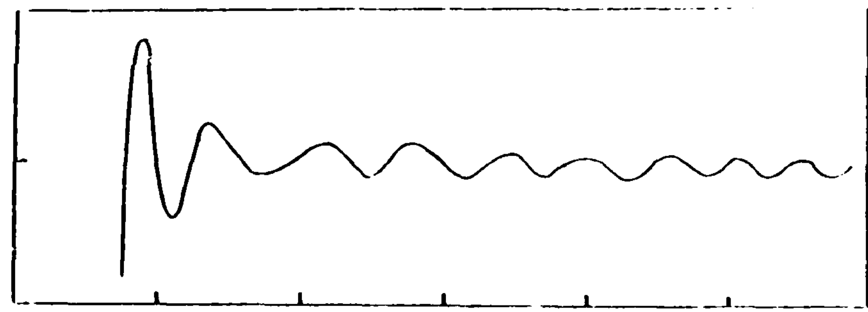


Figure 6.56d Load Current with L10A Diode Bridge; 2A/DIV, 100 NS/DIV.

Figure 6.56 10 MHz Damped Sinusoid Pulse (DSP) Directly Injected Across 100 Ohm Load

The direct injection tests for the UYQ-21 were set up by connecting the simulated load across the output of the damped sinusoid pulser. The load voltage and current were then monitored without and with the appropriate TPD connected across the load.

In conducting the cable coupling tests, each of the cables was installed on the test bed and connected to the source and the load termination boxes. The source impedance was simulated with a 1K resistor. The simulated load impedance was 100 ohms for the UYQ-21. The current injection transformer and the CT-5 current probe (Table 6.17) for monitoring the overall cable currents were clamped around the cable near the midsection. The voltage and current probes for monitoring the load response were installed in the load terminating box. The load transfer waveforms were then monitored and photographed on the oscilloscope.

The TPD designated for use on the UYQ-21 is given in Table 6.18. The fast recovery diode bridge (Figure 6.54) was used in conjunction with the bipolar transient suppressors for the UYQ-21 system to reduce the capacitance on the high speed data lines.

Figures 6.55a-b show the voltage and current response across a 100 ohm load to a 1 MHz, 10 A, damped sinusoidal current directly injected into the load. Figure 6.55c-d show the response with a L10A diode bridge across the load. The load current is reduced to about 1 A and the voltage to 40 V.

Figures 6.56 a and b show the voltage and current response across a 100 ohm load without a TPD at 10 MHz. With a L10A diode bridge across the load, the load voltage is reduced from 1000 volts to about 30 volts (Figure 6.56c) and the load current is reduced from 10 A to about 0.5 A, except for the initial peak of 1.5 A which is attributed in part to lead inductance in the setup. The test measurements at 50 MHz are not shown because some stray circuit elements may have obscured the true measurement values.

6.4.4 Power Line Protection

Power lines operate at low frequencies ($\leq$ 400 Hz) whereas EMP has a high frequency spectral content. This allows filters and nonlinear TPDs with high insertion losses at high frequencies to be used. For example, Figure 6.47 shows the installation of metal oxide varistors (MOVs) to protect AC (and DC) power lines. Consequently, the numerous methods of power supply hardening are now shown in further detail.

6.5 Use of Protective Devices at Antenna Interfaces

6.5.1 Introduction

Generally, in shipboard operation, a transmitter or receiver is not connected to an antenna directly [6.25]. A ship requires that receivers be protected from ship's transmitted energy and that, when possible, antennas be shared. Multicouplers provide both these functions by allowing simultaneous use of an antenna by several transmitting and/or receiving equipments while providing isolation between them and from extraneous signal sources. Transmitting multicouplers, because they must provide both efficient matching to the antenna and isolation between channels with low insertion loss, require a broadband antenna having a Voltage Standing Wave Ratio (VSWR), on 50 ohms, of 3:1 or less.

Table 6.17 Voltage and Current Probes [6.16]

PARAMETER	CURRENT PROBE	VOLTAGE PROBE
Pulser Output		TEK P6015
Cable Bulk and Core Currents	*TEK CT-5	
Load Parameters	TEK P6022	TEK P6008
*TEK CT-1 used at 50 MHz (TEK = Tektronix)		

Table 6.18 TPD Designated for UYQ-21 [6.16]

SYSTEM	TPD	BREAKDOWN VOLTAGE (VOLTS)
UYQ-21	L10A, FF15 Diode Bridge	10
	L20A FF15 Diode Bridge	20
	L60A FF15 Diode Bridge	60

Antenna and multicoupler are normally limited to 3:1 frequency range. Greater loss can be tolerated in receiver circuits because atmospheric noise normally determines receive sensitivity and limitation on permissible antenna VSWR is not as important. Greater loss is also allowed in the receiver multicoupler in order to increase off-frequency rejection. Often a single antenna suffices to cover the HF spectrum.

Upon these complex systems will be incident the Electromagnetic Pulse (EMP) engendered by an exoatmospheric nuclear burst. The EMP planewave pulse incident upon the antenna is that specified in Section 2.4.5. This specification is not used in this section explicitly. The amount of EMP energy coupled to the antenna is dependent upon the antenna geometry. The larger antennas (HF) allow more EMP energy to be received by the antenna structure than the smaller antennas (VHF/UHF). The amount of coupling to the antenna is explicitly specified in Section 2.4.3.3 or 2.4.3.4 depending upon whether the antenna is unhardened or hardened, respectively.

The purpose of this subsection is to identify the problem areas encountered in protecting antennas with TPDs and the solutions. The problem areas associated with applying TPDs at antenna interfaces are:

1) System loading

2) Spurious-frequency generation of third-harmonic or inter-modulation products

3) System noise level effects

4) Extinguishing characteristics after TPD gap firings.

These problem areas can be isolated and corrected using time-domain reflectometry (TDR) techniques and by lowering the VSWR.

Even under normal conditions, shipboard topside harmonic and intermodulation levels from nonlinear devices and objects greatly affect receivability and/or compatibility. Because protective devices could introduce nonlinear elements at critical points, for example in a multi-frequency transmitting antenna, the very real intermodulation problem may be exacerbated [6.26].

Intermodulation aboard ship is a major cause of interference to receiving systems and is greatly aggravated by the use of many simultaneous transmissions. When seven or more transmitters are used simultaneously, the probability of interference on any receiving frequency is very great. For example, ten transmitters can produce 100,000 products up through the 7th order. The most serious cause of intermodulation is in the receivers if they are unprotected by narrow bandpass filters. Use of good two-section filters will practically eleminate the receivers as significant sources of intermodulation.

In this section examples of protective devices designed to protect HF and VHF/UHF antenna interfaces from the transients specified in Sections 2.4.3.3 and 2.4.3.4 are presented. Also discussed is the compatibility of each protective device on system performance.

6.5.2 Protection at HF Antenna Interfaces

Protection of equipment connected to HF antennas is complicated by the fact that the EMP spectrum (0.1-10 MHz) and the HF antenna operating spectrum (3-30 MHz) overlap. This voids the general application of filters to suppress the EMP threat. Hence, the EMP transient suppression at HF antenna interfaces is generally accomplished through the use of nonlinear TPDs. These TPDs must have a low insertion loss to limit system loading.

An example of the protection measures used to harden the HF antenna interface is illustrated in References 6.21 and 6.25. The example presented is applicable for hardened and unhardened HF antenna interfaces. The major difference is that the hardened antenna will have a primary voltage limiter near the antenna and the isolation element such as inductor or resistor will most likely not be required, because there is probably physical isolation (a delay line) between the primary voltage limiter and the secondary voltage limiters.

6.5.2.1 TPD Selection

The selection and preliminary compatibility evaluation of the HF antenna transient suppressor is from Reference 6.21. The example presented here is the attempted hardening of a 31 foot trussed whip antenna interface. The high voltage capable of being coupled into a 31 foot trussed whip antenna system from an EMP event requires adequate surge protection to preclude catastrophic electronic component failures. Some of the problems in protecting this system result from the very fast pulse rise times and the high energy levels to be dissipated.

In general, the TPD must not significantly degrade any circuit when in the standby mode, it must provide sufficient transient suppression, and must be capable of withstanding multiple EMP transients without degradation. Specific TPD criteria selected for this system, which are derived in the latter part of this section, are:

1. Limit the peak voltage transient at the antenna coupler input to 5 kV maximum, and the principal pulse voltage to 1 kV maximum.

2. The TPD shall not trigger below 500 volts.

3. The 3 dB cutoff frequency imposed by the TPD shall be greater than 36 MHz.

The TPD designed for this system, designated TPD Model 2, is shown schematically in Figure 6.57. The TPD is a hybrid type consisting of a gas filled spark gap in parallel with a series string of bipolar transzorb transient suppressors. A 0.1 μH inductor separates the spark gap and transzorb string. Following an EMP event, the transzorbs will respond within about 1 nanosecond to clip the fast rise time edge of the pulse.

The induced voltage buildup across the inductor will assist the breakdown of the gap. After firing, the gap will operate in the arc region, diverting the majority of the EMP energy through the gap. The gap will extinguish as the transient pulse voltage and current decay below the threshold levels.

The 500 volt minimum voltage criteria for the TPD was derived from the system operating levels. The maximum peak envelop power rating, P_{pep}, specified for the

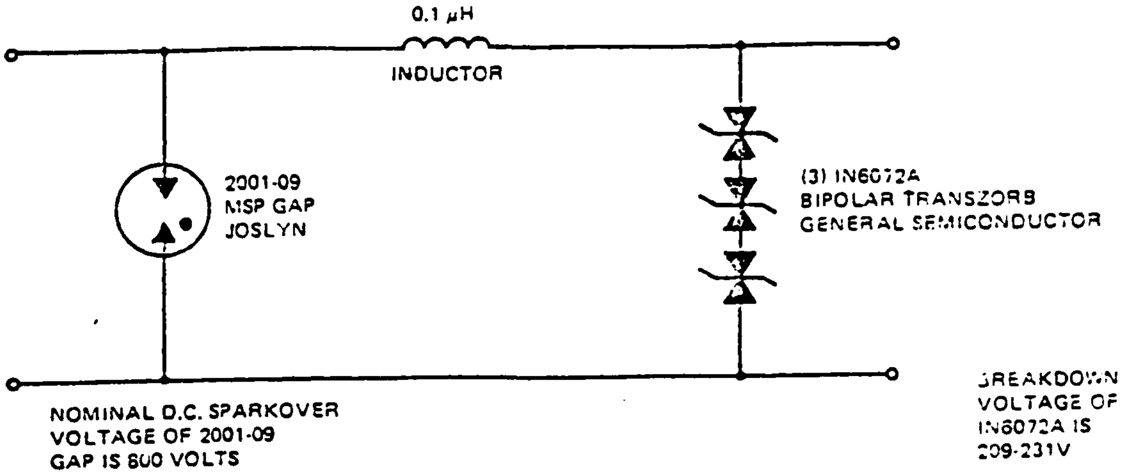


Figure 6.57 Transient Protective Device Model 2, Schematic Diagram [6.21]

antenna coupler, CU-1170/SRC-16 is 1200 W, giving a peak voltage of 245 volts for a 50 ohm load. Given a safety factor of 2 to account for a mismatch in load impedance, the maximum signal voltage is 490 V.

The 3 dB cutoff frequency, f_{3dB}, is controlled largely by the TPD shunt capacitance, C_T. The maximum value of C_T permitted can be determined from (6.1). If f_{3dB} is assumed to be 36 MHz (twice maximum signal frequency), and R_S = 163 ohms and R_L = 50 ohms, then C_T = 115 pF maximum.

The standby characteristics for the TPD Model 2 hybrid shown schematically in Figure 6.57 are given in Table 6.19.

Table 6.19 TPD Model 2 Standby Characteristics [6.21]

Device	Part Type	V_{BD} Volts	C_T pF	f_{3dB} MHz
Transzorb	1N6072A	220	250	
Transzorb	(3 in series)	660	83	50
Spark Gap	2001-09	800	<1	4150
Hybrid Assembly	--	660-800	84	50

The TPD hybrid assembly has a V_{BD} of 660 to 800 V, and an f_{3dB} cutoff frequency of 50 MHz, which is well above the minimum levels determined above.

The TPD Model 2 protection mode characteristics are given in Table 6.20. In the protection mode the turn-on and conduction characteristics of each device are of primary importance. The estimated turn-on time, taken from the manufacturer's data sheets, is 1 to 5×10^{-9} sec for the 1N6072A transzorb, and 5 to 10×10^{-9} sec for the 2001-9 spark gap.

Table 6.20 TPD Model 2 Protection Model Characteristics [6.21]

Parameter	Transzorb String (3) 1N6072A	MSP Gap 2001-C9
DC Breakdown Voltage	660 V	800 V
Impulse Breakdown Voltage (5 kV/ns - estimate)	660 V	5 kV
Holdover Voltage	660 V	400 V
Surge Current Rating	4.6A (10 x 1000 µs)*	10 kA (10 x 20 µs)*

* 1st number in parentheses is the rise time in microseconds from zero to peak value. 2nd number gives rise time interval from zero to the $\frac{1}{e}$ point past the peak.

The turn-on time response parameter is not well defined for fast rise times associated with EMP type signals. Tests should be made on each device type to provide quantitative data.

The transzorb string has sufficient surge capability to clamp the fast rise time pulse for 10×10^{-9} second. During this time, the spark gap will break down, turning off the transzorbs. Although no data is available on the peak current rating of the 1N6072A for a 10×10^{-9} second surge, extrapolation ratings indicate it could go two orders of magnitude above the surge current rating given in Table 6.20 without damage.

The surge current rating of the spark gap is sufficient to handle the bulk of the pulse energy.

6.5.2.2 High Frequency TPD Tests

The testing procedure for evaluating the compatibility of the TPD with the HF antenna system is from Reference 6.25. Testing determined that the TPD was not well suited for protecting the HF antenna due to the large amount of intermodulation introduced into the system. The TPD testing procedure is presented here in detail to illustrate the numerous problems which must be overcome in finding a TPD which is capable of protecting the HF antenna.

A preliminary measurement of the TPD in an rf environment indicated a need for extra shielding to prevent extraneous pickup from the source. A copper box was constructed and the device mounted inside with input and output access provided through UHF-N type connectors.

The following measurements were then made on the TPD Model 2:

1. Resistance, capacitance, inductance
2. TDR measurements
3. Impedance and phase angle
4. Insertion loss, bandwidth
5. Power handling capability, reflected power
6. Nonlinearity-harmonic generation
7. Receiver noise figure.

Resistance, capacitance and inductance measurements on the TPD were made as follows:

(a) Resistance: shunt resistance R_S of the TPD was measured with a General Radio Type 1864 Megohmmeter. Results of the measurements as a function of applied DC voltage are shown in Figure 6.58. No difference was noted whether looking to "input" or "output" ports.

(b) Capacitance: shunt capacitance C_S of the TPD was measured with a Tektronix Type 130 L-C meter. This was found to be C_S = 77 pF. No difference was noted between input and output ports.

(c) Series inductance of the TPD was measured on a Tektronix Type 130 L-C meter. Bare bus wire was connected from the meter to the "input" port, through the TPD, and from the "output" port to the meter. Inductance was found to be L = 0.25 μH. To confirm the reliability of this procedure, an inductor with the same dimensions as indicated on the TPD drawings was constructed and measured on the same meter. This turned out to be L = 0.1 μH - the same value as indicated on the drawing. Low frequency inductance formulas also give L = 0.1 μH for these dimensions. Again no difference was noted when the input/output leads were reversed.

(d) Figure 6.57 is the schematic of the Model 2 TPD furnished by the manufacturer. The nominal DC sparkover voltage of the Joslyn msp (miniature surge protector) 2001-09 is 300 volts. The breakdown voltage of each of the General-Semiconductor Transzorbs, type 1N6072A, is 209-231 volts; these are essentially back-to-back Zener diodes.

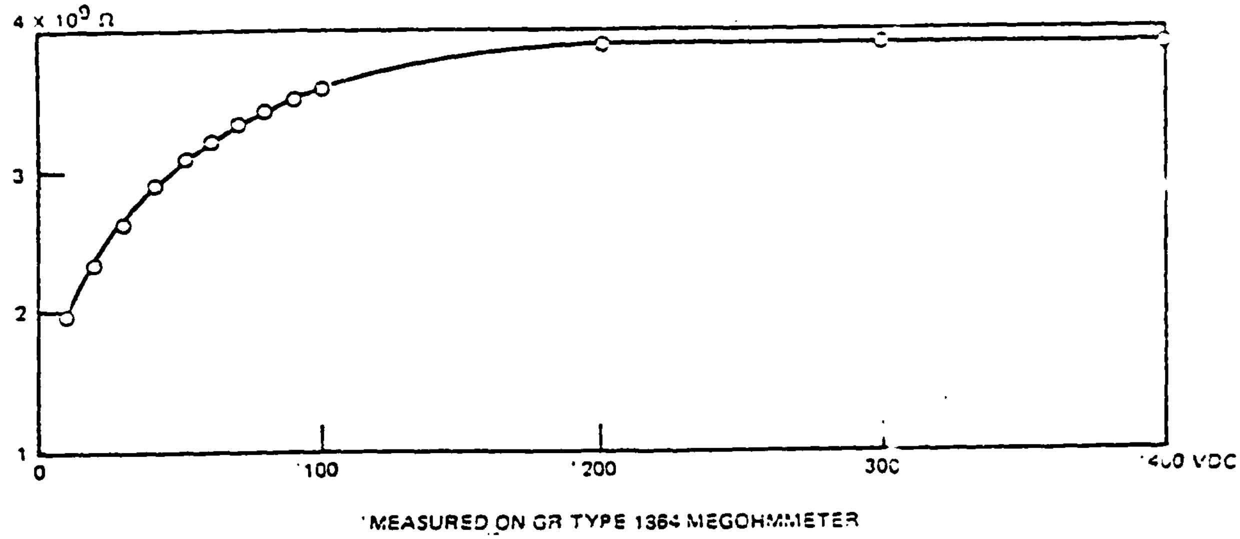


Figure 6.58 HF TPD Resistance versus Applied DC Voltages [6.23]

6.5.2.3 Time Domain Reflectometer Test (TDR)

TDR tests were made with a Tektronix type TDR 1502 Reflectometer. Results of these tests are shown in Figure 6.59. The TDR test with and without the TPD are shown. With just the 50 ohm load a small hump can be noted due to a connector. With the TPD installed the reflection coefficient is 0.58 maximum. Some "ringing" is noted before the system returns to the 50 ohm level. The third oscillogram is referred to later.

The reflectometer, although desired primarily for measurements on cables and transmission lines, does give useful data on components and discrete elements. It functions by periodically generating a step-waveform (period of 60 micro-seconds) with an amplitude of 225 millivolts, duration of 10 microseconds, and a rise time of 110 picoseconds. The display - either cathode-ray-tube or a chart from a sampling readout - consists of the reflected signal superimposed on the incident signal. A reflection coefficient ρ (= $E_{reflected}/E_{incident}$) is measured in general for a 50 ohm reference impedance, Z_{ref}. Thus a cable or component impedance is defined as $Z = Z_{ref} \times [(1+\rho)/(1-\rho)]$ and an open-circuit or increased Z in a cable or a series inductor causes a rise or increase in the reflected signal display, that is, a positive ρ. A cable short or decreased Z or a shunt capacitance gives a negative ρ.

The TPD test shows clearly the rise in impedance at what is the rear connection on the type N connector followed by the capacitance of the spark gap. The increased ρ from the inductor is quite evident and then follows the shunt-capacity effect of the shunting diodes.

6.5.2.4 Impedance, Insertion Loss, and VSWR

Measurements of the HF TPD were made on a Hewlett-Packard Model 4815A Radio Frequency Vector Impedance Meter. These data are shown as a function of frequency in Figure 6.60. VSWR values are found on this Smith Chart by projecting a circle with center at 1.0 and radius to the point at a particular frequency

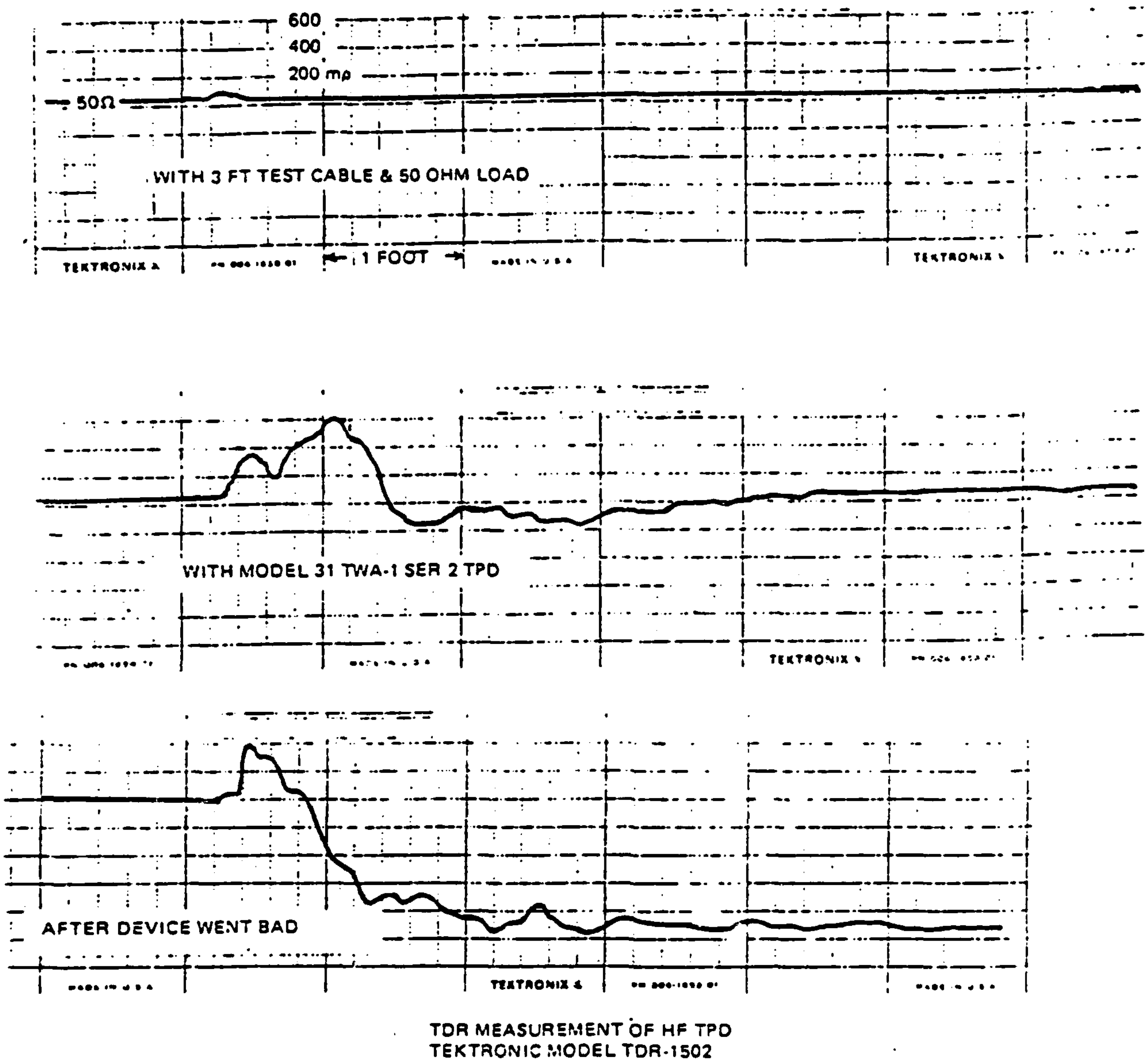


Figure 6.59 Time-Domain-Reflectometry of HUAC TPD [6.25]

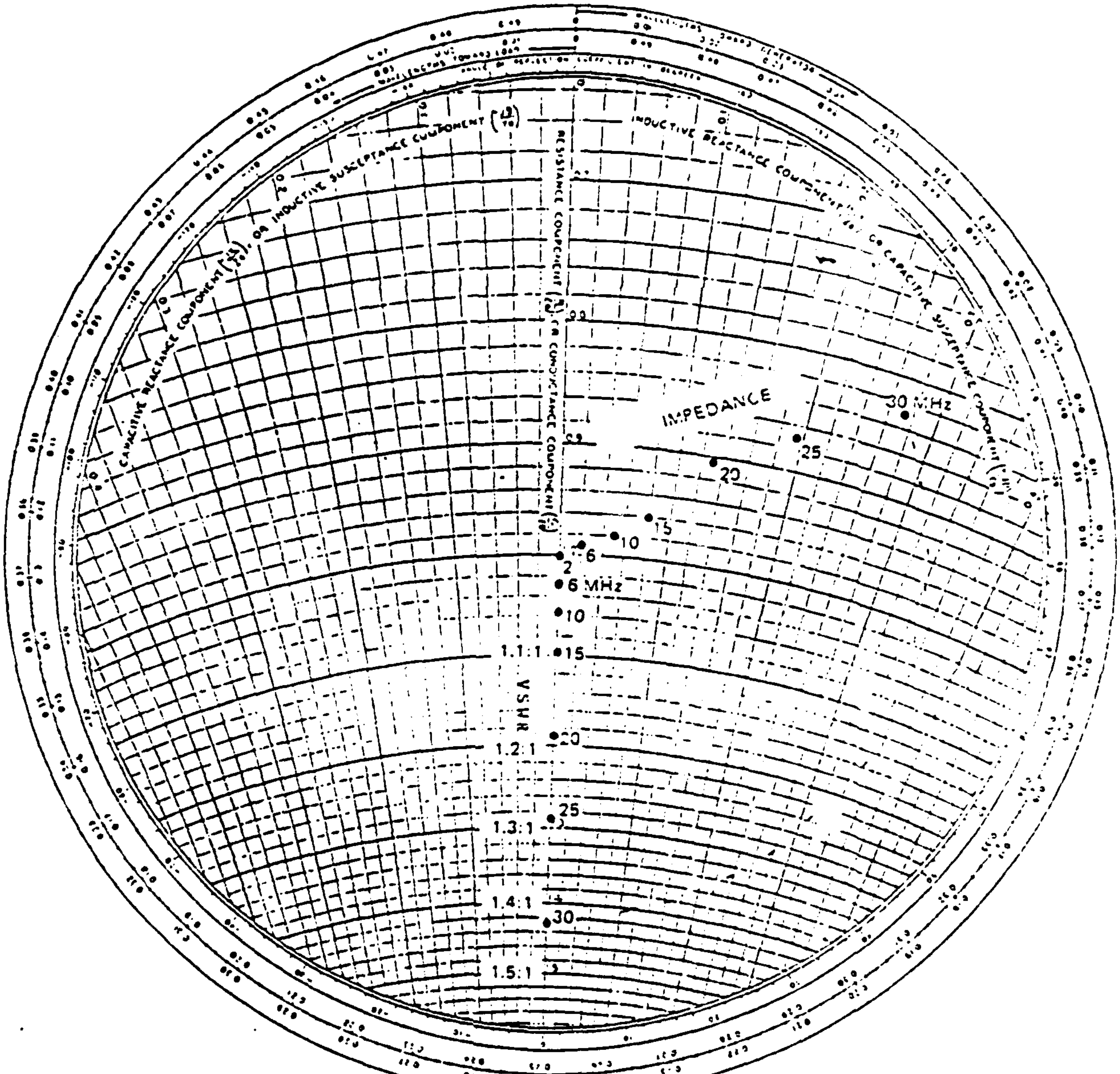


Figure 6.60 Impedance and VSWR versus Frequency for HUAC TPD [6.25]

onto the vertical scale. As can be seen, the TPD appears inductive at all frequencies with VSWR ranging from 1.0 at 2 MHz to 1.43 at 30 MHz.

Insertion loss and bandwidth of the HF TPD were measured on a Hewlett-Packard Model 1411T Mainframe-Display/8553B RF Section/8552B IF Section/8443A Tracking Generator-Counter. Results of these measurements are shown with insertion loss as a function of frequency in Figure 6.61. This shows a maximum 0.4 dB loss below 30 MHz and a 3 dB cutoff at 55 MHz.

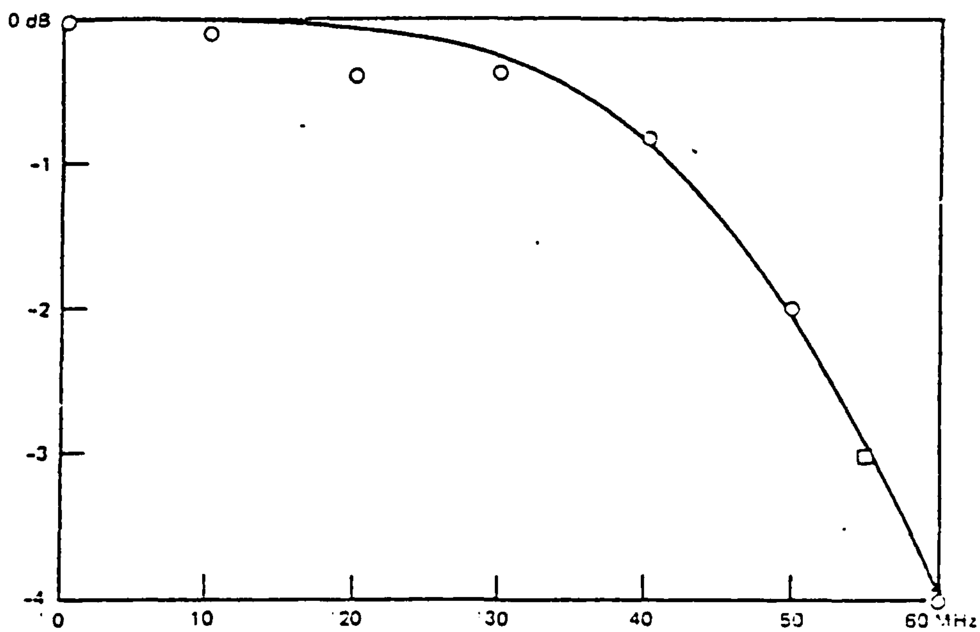


Figure 6.61 Insertion Loss Versus Frequency for HUAC TPD [6.25]

Initial power applied to the TPD was held below 800 watts with most measurements made at 600 watts. The AN/URT-23 one kilowatt transmitter used for these tests appeared less stable above 800 watts. Also, it seemed reasonable to hold the power applied to the TPD to a lower level until all of its parameters were determined. Figure 6.62 shows the VSWR as a function of frequency as determined from the forward and reflected power values. Also on this figure are plotted VSWR values from the Smith Chart of Figure 6.60 and similar data taken with a Hewlett Packard 8407A Network Analyzer System; both of these agree at low level. At high power levels, the VSWR is quite different, although reasonable in magnitude. Table 6.21 lists the forward and reflected powers as measured with the Bird Wattmeter and a 50 ohm dummy load.

6.5.2.5 Nonlinearity and HF Harmonic Generation

Two different systems were devised to measure harmonic generation. The first was for a "quick" look for third and higher harmonics and the second for a more precise measurement of third harmonic generation, especially as a function of power level applied to the TPD.

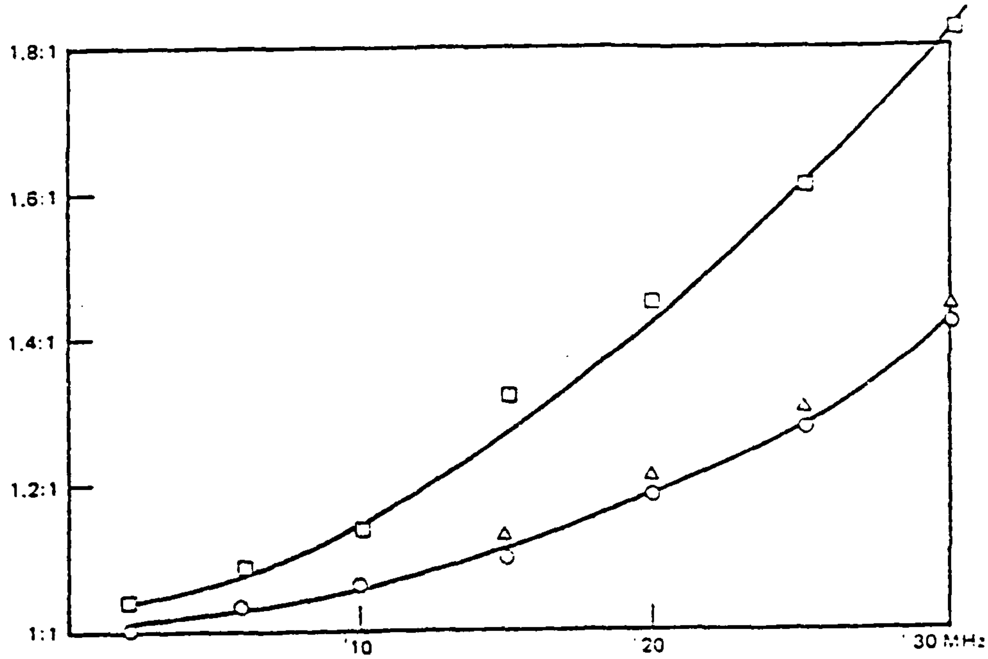


Figure 6.62 VSWR versus Frequency of HUAC TPD by Bird Wattmeter at 600 Watt Level (□), HP Network Analyzer ( ), and Smith Chart Data (0) of Figure 6.60 [6.25]

Table 6.21 Forward and Reflected Power by Bird Wattmeter [6.25]

	WITHOUT TPD		WITH TPD	
2 MHz	600 watts	0.1 watt	600 watts	0.1 watt
4	600	0.1	600	0.1
6	600	0.3	600	1.1
10	600	1.3	600	2.6
15	600	1.4	600	11.2
20	600	1.2	600	19.8
25	600	2.2	600	33.0
30	600	2.9	600	52.0

Figure 6.63 is a block diagram of the first system in which a 20 MHz high pass filter is employed to greatly attenuate the fundamental of 4.0440 MHz with power level nominally of 600 watts or 57.8 dBm as measured with the Bird 43 Power Meter. Figure 6.64 is the attenuation plot for the low-pass filter used to improve spectral purity of the URT-23 power source. The high-pass filter following the TPD and the 30 dB fixed attenuator greatly attenuates the fundamental and some of the generated harmonics. Consequently, a correction to the data has to be applied. Figure 6.65 shows two oscillograms of the filter response at 2 and 5 MHz/division as taken with the 8553-B Spectrum Analyzer. The wide bandwidth scan shows high frequency detail but the fundamental data is lost in KTB noise; the 2 MHz/division scan clearly shows 75-76 dB of attenuation at 4 MHz. The first peak in Figure 6.65 is at 16.495 MHz.

Figure 6.66 shows oscillograms from the Spectrum Analyzer with and without TPD. To these data are applied corrections to obtain the actual levels at the TPD. These corrections are the sum of 30 dB and the appropriate frequency. These data are tabulated in Table 6.22 and the spectrum is presented in somewhat of a "bar-chart" form in Figure 6.67.

A second system was devised to give an even "cleaner" system with respect to the third harmonic. This is especially desirable in making measurements at reduced power levels. Figure 6.68 is the block diagram of this system in which the low pass filter is that previously described. The two filter-traps further attenuate the third harmonic; the second of these is in effect a short circuit at this frequency and in conjunction with the $\lambda/4$ line segment presents a high impedance to any third harmonic coming from the TPD, routing it to the spectrum analyzer. The HP 355C/D attenuator is nominally at zero attenuation. The tunable band-pass filter attenuates 2.8 dB at the tuned frequency and as shown in Figure 6.69, reduces the 57.8 dBm fundamental to a level of -60 dBm at the analyzer. From this figure it is seen that the level of the third harmonic is -12 dBm at the analyzer or -6.2 dBm at the TPD.

A total correction of 5.8 dB is applied because of the 2.8 dB of the filter plus an additional 3 dB as the TPD is, in this circuit, loaded by two 50 ohm loads in parallel, that of the analyzer plus the 50 ohm, 500 watt termination required to absorb the fundamental power. Figure 6.70 shows oscillograms at 100, 10 and 1 watt driving levels; in all of these except the no-TPD of Figure 6.68 the log reference (top of screen) is -10 dBm and the scan width is 2 MHz/division. Table 6.23 lists third harmonic levels for various driving levels of the fundamental as measured with this system.

Figure 6.71 is a graph of most of these data and it is seen that there is almost a linear relationship with the driving and third harmonic levels. The above datum of -6.2 dBm at 600 watts differs from the -5 dBm of the first system by only 1.2 dB, a reasonable experimental and reading error.

6.5.2.6 HF Receiver Noise Figure

Receiver noise figure measurements were made on the TPD to determine if there is any receiver degradation from the TPD when installed on a standard, R-1051/URR, shipboard-high-frequency receiver. Table 6.24 lists the results of this test over a 2 to 30 MHz frequency range. Figure 6.72 is a block diagram of this test.

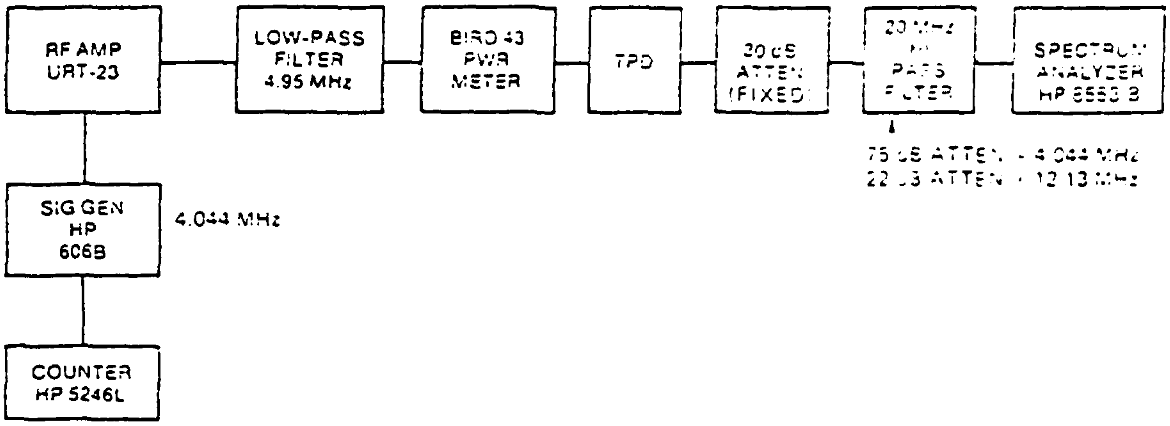


Figure 6.63 Block Diagram of First System for Harmonic Measurements [6.25]

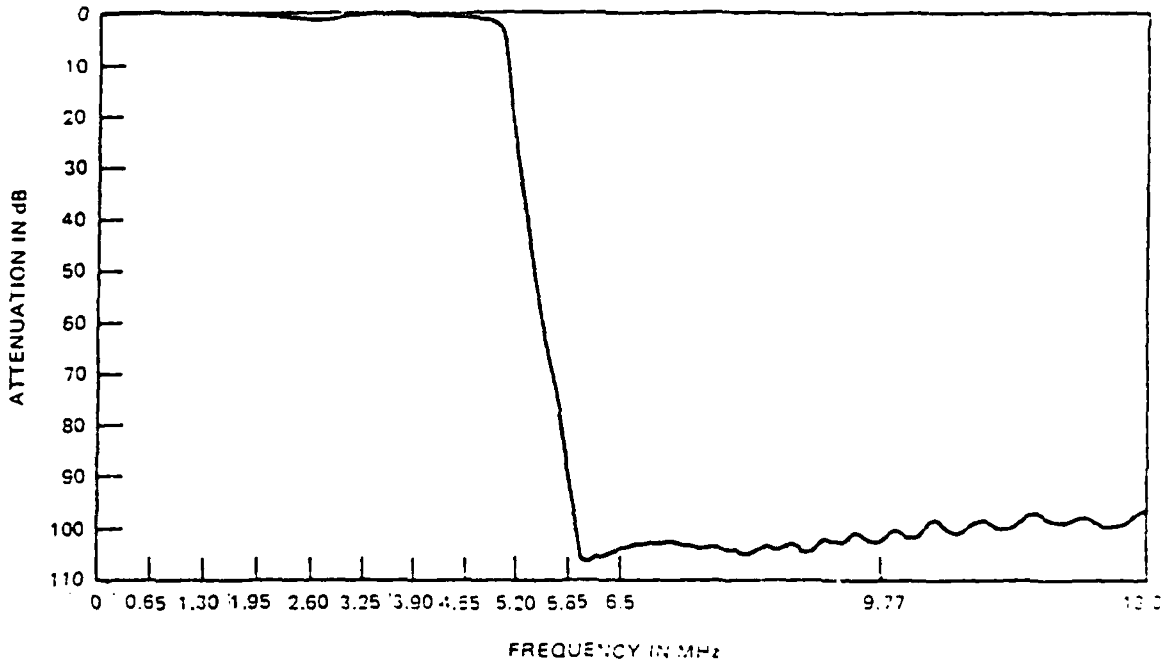


Figure 6.64 Insertion Loss of Low Pass Filter [6.25]

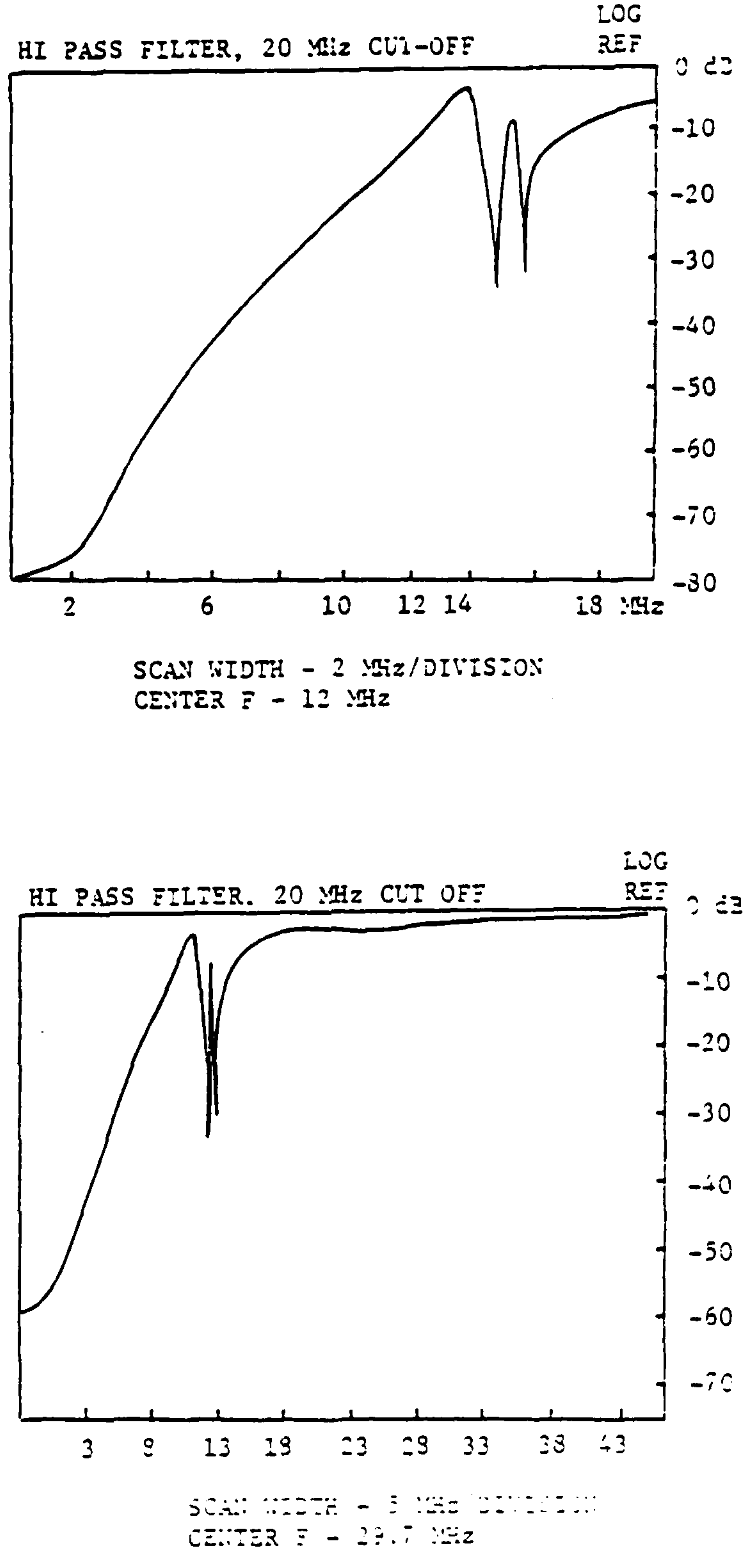
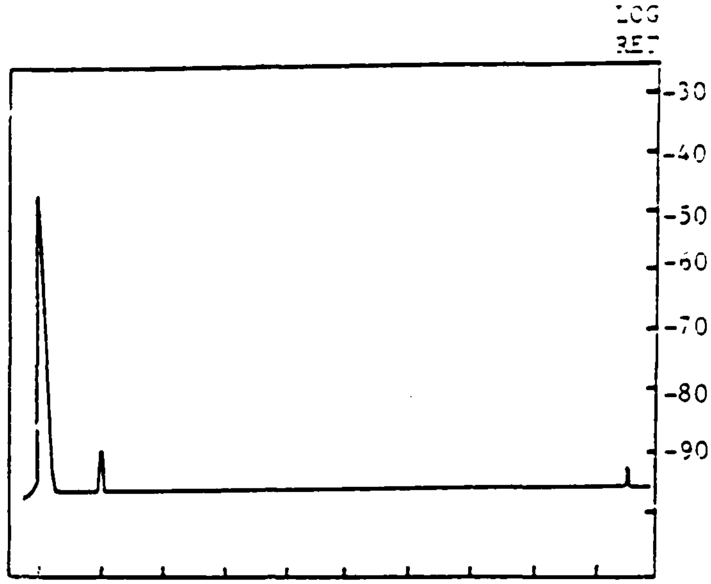
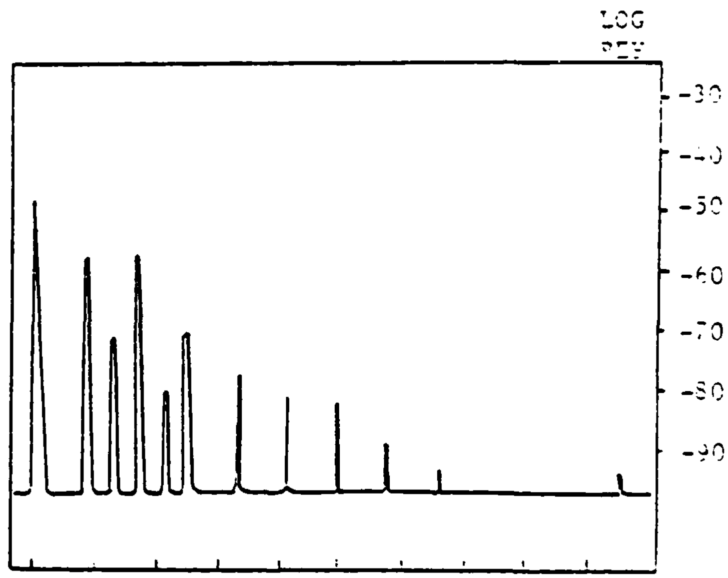


Figure 6.65 Insertion Loss of High Pass Filter [6.25]



WITHOUT TPD - A "CLEAN" SYSTEM
FUNDAMENTAL WITH TRACE OF 3F



WITH TPD AND HARMONICS SHOWING
10 MHz/DIVISION

Figure 6.66 Oscillograms from Spectrum Analyzer of Fundamental and Harmonics to Number 17 [6.25]

Table 6.22 Harmonic Energy Levels [6.25]

Frequency MHz	Harmonic Number	Filter Insertion Loss in dB	Level by Oscillograph Trace, dBm	Corrected Level at TPD in dBm
4.0440	(1) Fund.	75	-48 (600W)	+57.8
12.132	3	22	-57	-5.0
16.176	4	4	-73	-39
20.220	5	8	-56	-18
24.264	6	4	-83	-49
28.308	7	5	-70	-35
36.396	9	3	-76	-43
44.484	11	2	-76	-44
52.572	13	0.5	-82	-51
60.660	15	1.2	-88	-57
68.748	17	1.5	-96	-65

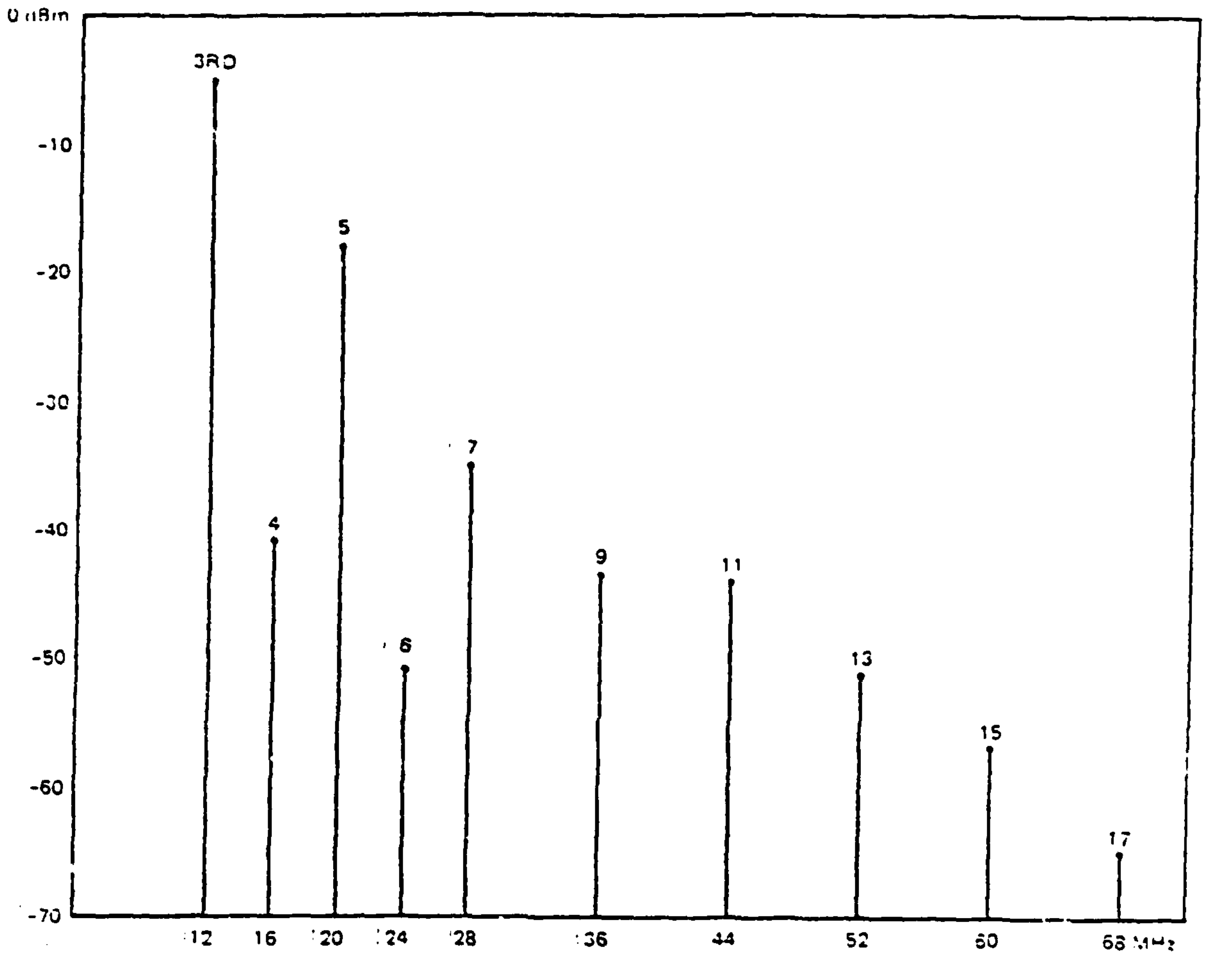


Figure 6.67 Spectral or "Bar Chart" Form of Harmonic Number and Level in dBm for HUAC TPD at 600 Watt Fundamental [6.25]

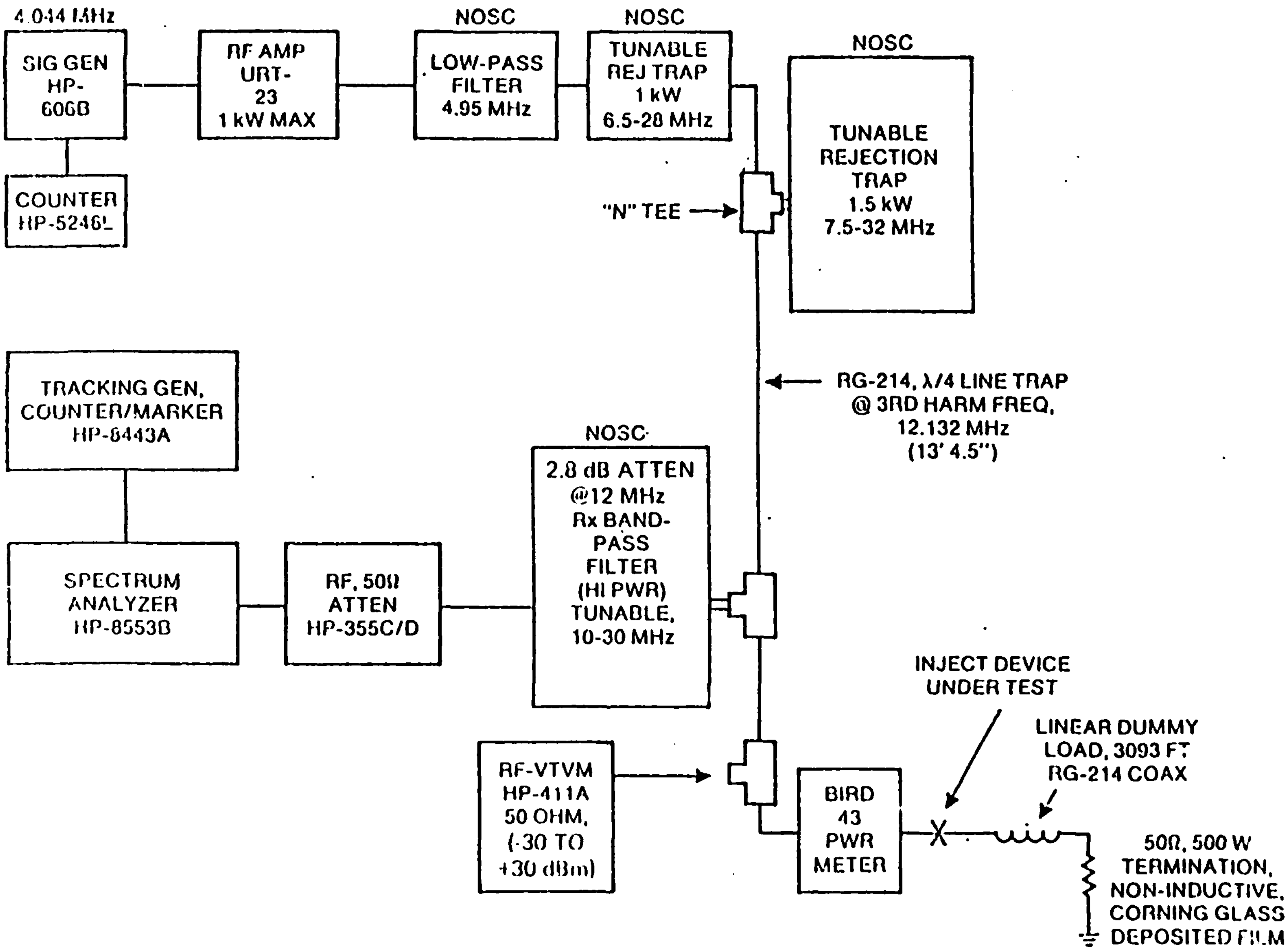


Figure 6.68 Block Diagram of Second System for Third-Harmonic Measurement [6.25]

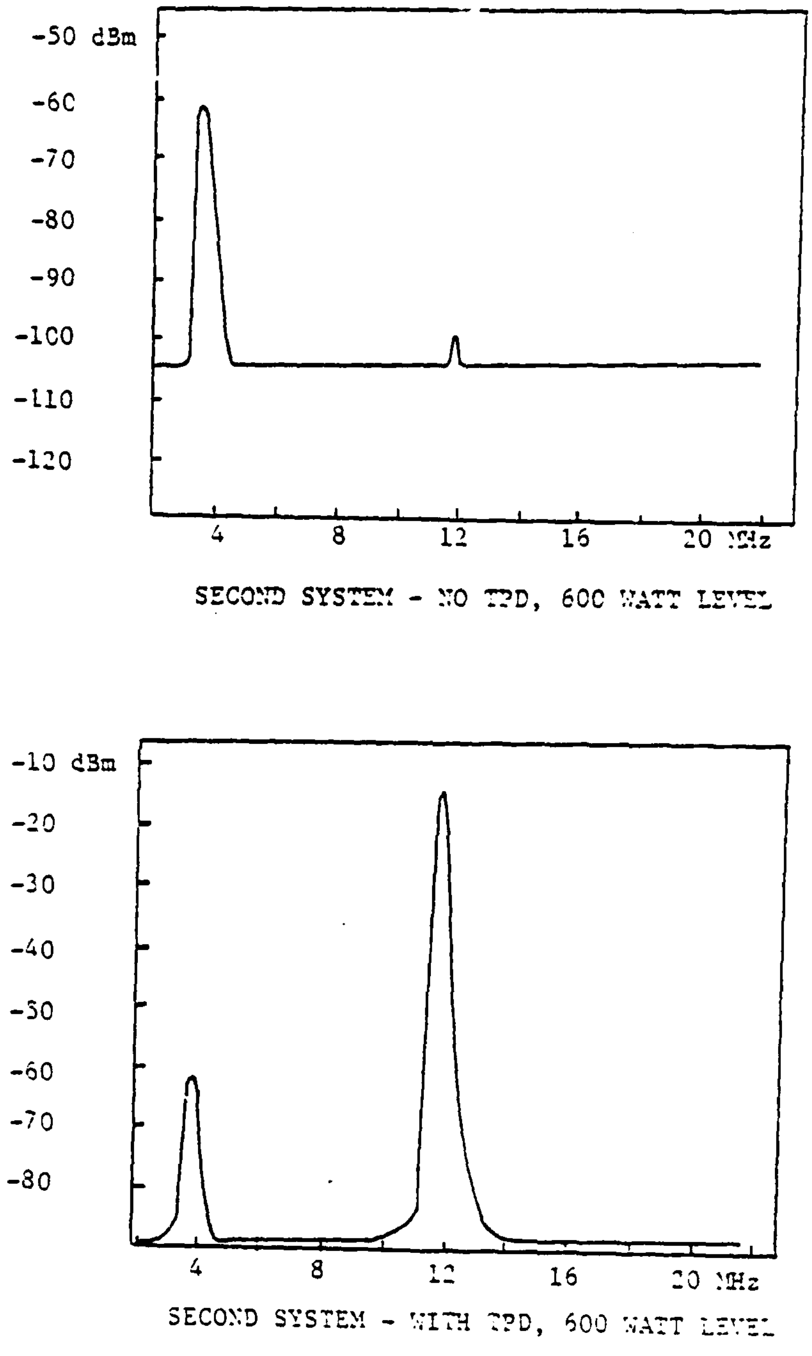


Figure 6.69 Oscillograms from Spectrum Analyzer of Second System, 600 Watt Fundamental. With and Without TPD [6.25]

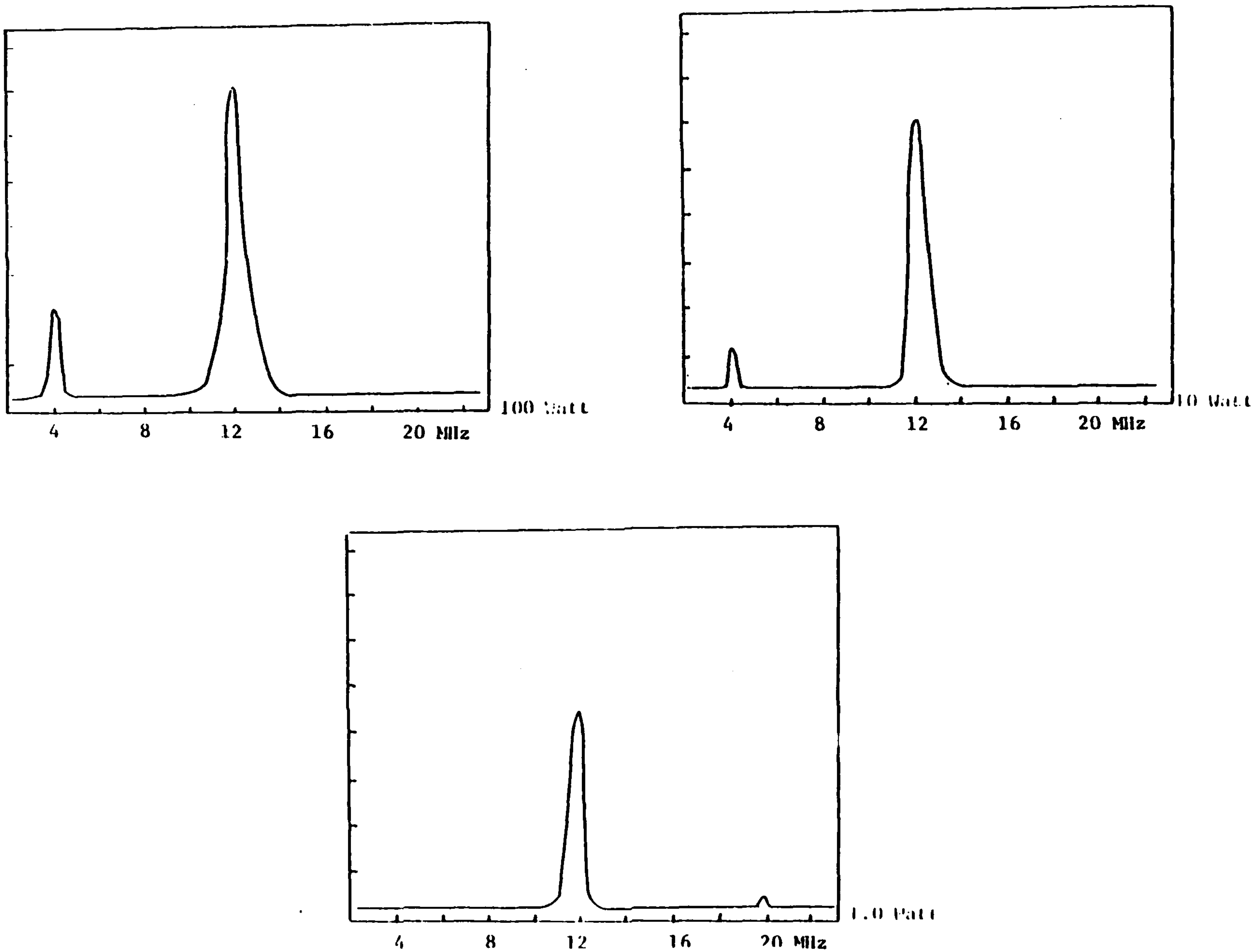


Figure 6.70 Same as 6.69, but at Power Levels of 100, 10 and 1 Watt [6.25]

Table 6.23 Third Harmonic Levels Versus Driving Levels [6.25]

Driving level watts	dBm	Level at analyzer dBm	Corrected level at TPD dBm
600	57.8	-12	-6.2
300	54.8	-15.5	-9.7
100	50.0	-20.0	-14.2
10	40.0	-30.5	-24.7
5	37.0	-33.5	-27.7
2	33.0	-40.5	-34.7
1	30.0	-45.0	-39.2
0.5	27.0	-50.5	-44.7
0.1	20.0	-65.0	-59.2

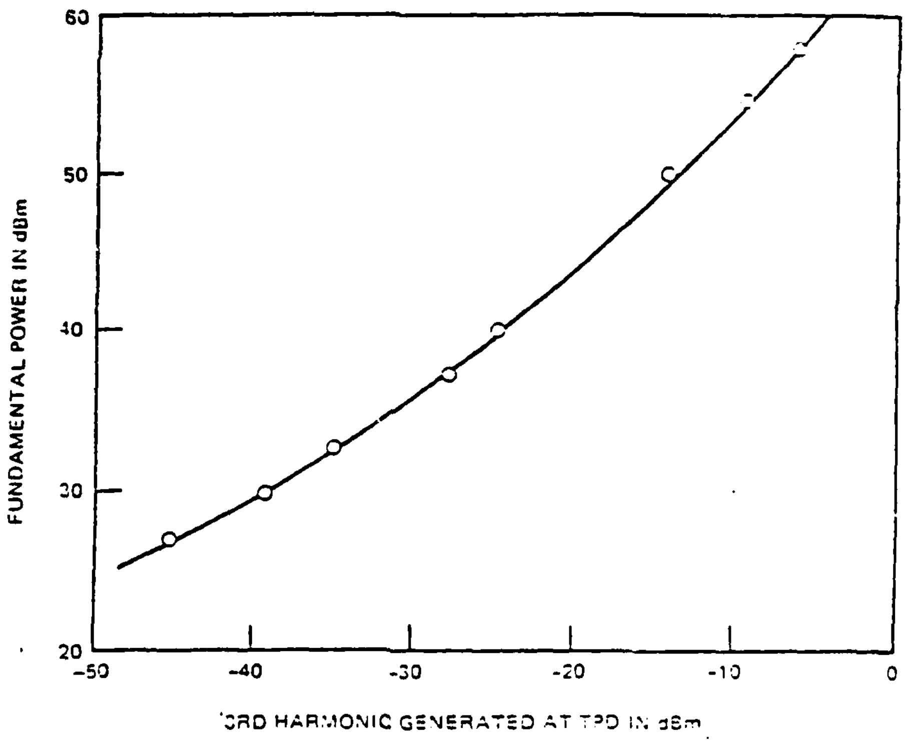


Figure 6.71 Third Harmonic Level Generated at HF TPD as a Function of Driving Power [6.25]

Table 6.24 Noise Figure [6.25]

Frequency	N.F. w/o TPD--dB	N.F. with TPD--dB
2.1 MHz	12.0	12.0
5.1	11.8	11.8
10.1	10.8	10.8
15.1	12.0	12.0
20.1	13.0	13.0
25.1	14.0	14.0
29.9	15.5	15.5

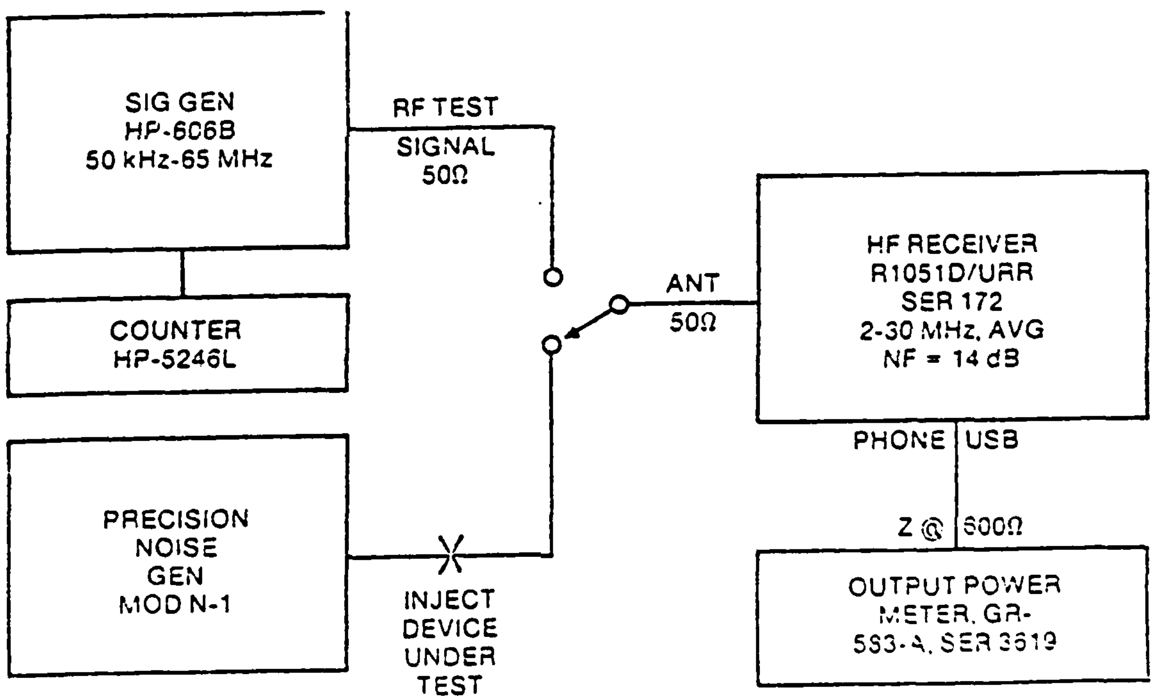


Figure 6.72 Block Diagram of HF Noise-Figure Measuring Experiment [6.25]

A 0.14 μV signal was then fed into the R-1051D/URR at 20.1 and 29.1 MHz. No difference was noted on the signal level indicated on the output meter.

6.5.2.7 HF Antenna TPD Discussion

The resistance, capacitance, and inductance measurements were made to establish a baseline reference and to give some indication of what to expect prior to installation of the TPD in any system. It can also provide a reference comparison for other TPDs of the same type. The equivalent circuit of the TPD in a 50 ohm system would be a 0.1 μH inductor in series with a paralleled 77 pF capacitor and 50 ohm resistor.

This would give:

$$\text{at 10 MHz } Z_{in} = 47.24 - j5.13$$

$$\text{at 30 MHz } Z_{in} = 32.75 - j4.92$$

Taking the 0.25 μH as measured on the L-C bridge would give

$$\text{at 10 MHz } Z_{in} = 47.24 + j4.37$$

$$\text{at 30 MHz } Z_{in} = 32.75 + j23.35.$$

The latter set of calculations agrees with the bridge and network analyzer measurements which show inductive reactance throughout the frequency range.

The increase in VSWR caused by insertion of a TPD of this type would have to be viewed on a system by system basis. High frequency Navy antenna systems are generally restricted to a maximum VSWR of 3:1. Installation of any VSWR would require other compensation. This might be possible for a single frequency or narrow band of frequencies but probably not for the whole frequency range of the antenna system. (Typical frequency ranges of Navy high frequency antennas are 2-6 MHz, 6 to 15 MHz or 10 to 30 MHz).

A question that has arisen with respect to VSWR is shown in Figure 6.67. This shows that the VSWR of the device when installed in a medium power installation is considerably different than is measured in a low-power bridge or network analyzer system. In trying to reconcile this inconsistency the device was installed in a higher power setup. Unfortunately in the process of trying to apply a 1000 watt power level to the TPD from a Collins 208-10, 2-30 MHz amplifier, a malfunction caused irreversible damage to the TPD and the destruction of the transmitter loading cell. This question of whether there was a transmitter malfunction or whether the VSWR of the TPD did indeed increase at this high power level was not resolved. The destructive effect is shown in the last oscillogram of Figure 6.59, showing TDR measurements "before and after".

As can be seen in Figure 6.66, harmonics are generated and easily observed up to the 17th harmonic. The following points should be considered:

(a) Specifications on most Navy transmitting systems show all harmonics generated to be at least 80 dB below the fundamental. This HF TPD generates a 3rd harmonic approximately 67 dB below fundamental - a degradation of 13 dB.

(b) Probably the most critical effect of this TPD, however, is that excessive harmonic generation is present and detectable even at very low power levels. Thus if the device were installed in a receive system, any nearby rf source and/or combination of the system without the TPD of Figure 6.68 used in these tests was approximately 160 dB below the 600 watt fundamental power level. Higher order harmonics were undetectable.

(c) A typical shipboard installation could be a transmitting system and a receive system on the same ship decoupled by 15 dB (a typical value on a CG). If transmitter power is 1000 watts this would mean 30 watts available at the receive antenna. It appears that harmonics generated throughout the HF spectrum would be well above receiver sensitivity (typically better than 107 dBm (1 μV @ 50 Ω).

If further analysis is deemed feasible, there are two points for consideration and clarification. One is resolution of the VSWR vs. power question and the other is to determine any change in the intermodulation products from two medium to high power sources.

Intermodulation is a serious problem when TPDs are installed in a broad band antenna system. There are few hybrid devices using both spark gaps and secondary voltage limiters that can adequately harden the antenna interface. In order to use the hybrid device TPD similar to the TPD model 2 for hardening HF antenna interfaces, the use of series inductors as isolation elements is not a good design practice because of the operation of the antenna at high frequencies. A delay line or series resistor would be more appropriate although probably not practical. In addition, the shunt capacitance of the TPD at 30 MHz or above generally restricts use of nonlinear TPDs (except spark gaps) at antenna interfaces.

6.5.3 Protection at VHF/UHF Antenna Interfaces

The application of TPDs to protect VHF/UHF (30 MHz - 3 GHz) antenna interfaces is presented in this subsection. As can be seen from Figure 2.6, the EMP frequency spectrum does not greatly overlap the VHF/UHF operating spectrum of the antenna. Thus filters could provide a large measure of protection for the VHF/UHF antenna interface. However, large voltages (< 4000 V) are still expected to couple to the VHF/UHF equipment.

References 6.21 and 6.25 present an example of the protective measures used to protect a VHF/UHF antenna. The actual antenna analyzed is the AS-1013/URC antenna. TPDs similar to the TPD analyzed to protect the AS-1018/URC antenna are then tested for compatibility with VHF/UHF antennas in general.

6.5.3.1 VHF/UHF TPD Selection

Transient surge protection is required to protect the receiver input from high voltage pulses coupled in through the antenna. The transient protective device (TPD) must be capable of suppressing the EMP induced transient specified in Figure 2.6.

The general requirements for a TPD are:

- The TPD must not significantly degrade the signal line or circuitry when in the standby mode.

- It must provide adequate transient suppression to preclude circuit damage or malfunction when operating in the protection mode.

- It must be capable of withstanding m[illegible]iple EMP transients without degradation.

Specific TPD criteria for protecting the AS-1018/URC antenna system are:

- Limit the peak voltage transient at the antenna coupler to approximately 1500 to 2000 volts.

- The TPD shall not trigger below 145 volts DC.

- The 3 dB upper cutoff frequency imposed by the TPD shall be greater than twice the highest operating frequency or 800 MHz.

The 1500 to 2000 peak voltage transient limit was determined from the maximum component stress levels.

The 145 volt minimum breakdown voltage criteria for the TPD was derived from the system operating level. The maximum power output of the Radio Set AN/SRC-20 is 100 watts, giving a line voltage maximum of 70.7 volts. Given a safety factor of 2 to account for a mismatch in load impedance, the maximum signal voltage is 141 volts.

The 3 dB upper cutoff frequency, f_{3dB}, is controlled largely by the TPD shunt capacitance, C_T. The maximum value of C_T can be determined from (6.2). If f_{3dB} is taken as 800 MHz, R_S and R_L are 150 ohms and 50 ohms respectively, and C_T = 5.3 pF maximum.

One of the few types of TPDs to meet the capacitance requirement is the spark gap. For this application an MSP series spark gap, Part No. 2021-11 manufactured by Joslyn was selected. The electrical characteristics of the 2021-11 spark gap are given in Table 6.25.

Items 1, 2, 5, and 6 of Table 6.25 are important parameters for the TPD when in the standy or passive mode. Each parameter in this mode satisfies the general and specific TPD criteria previously defined. Items 2, 3 and 4 relate to the protection mode or active parameters. The EMP transient risetime would approximate an impulse of less than 5 kV/nsec, item 2, given an impulse sparkover voltage of less than 1300 volts. This would adequately limit the peak voltage transient. The maximum surge current or short circuit current for the system was calculated to be 300 A. Therefore. the 5 kA surge discharge current value, item 3, is well in excess of requirements.

The TPD package design for the AS-1018/URC antenna cable is shown in Figure 6.73. The spark gap was fitted into a coax tee fitting, UG/28 A/U, to facilitate installation in the antenna cable line between the UHF transceiver and the antenna coupler, Figure 6.74. The compact size minimizes stray capacitance and lead inductance effects.

6.5.3.2 VHF/UHF TPD Tests

The insertion of a TPD at the VHF/UHF antenna interface requires testing in the system to determine system degradation. The tests performed on the TPD illustrate

Table 6.25 Electrical Characteristics - 2021-11 Spark Gap [6.21]

Item	Electrical Parameter	Value
1	DC sparkover voltage (SOV)	145 volts
2	Nominal impulse SOV at	
	5 kV/μsec rise time	580 volts
	5 kV/nsec rise time (extrapolated)	1300 volts
3	Surge discharge current on	
	10 x 20 μsec* waveshape	5 kA
4	Maximum holdover voltage at 1 A	100 volts
5	Insulation resistance at 100 Vdc	>10^9 ohms
6	Capacitance	<1.0 pF

* This defines a waveshape having a 10 μsec risetime and a period from to $\frac{1}{e}$ point past the peak of 20 μsec.

the test procedure (and example results) for determining any degradation of system performance after hardening the antenna interface.

Seven devices were made available for possible testing as UHF TPDs; three especially fabricated ones from Hughes Aircraft (HUAC), devices 96 and 98 being received later in the tests, and four commercially available from Fischer Custom Communications. All incorporate type N connector bodies, principally as Ts and some kind of gas-gap, sparkover surge-protector. Figure 6.75 shows typical devices.

All of the TPDs had a shunt resistance of greater than 10^{11} ohms at 100 volts, direct current as measured with a General Radio type 1864 megohmeter. Shunt capacitance was measured with a Tektronix type 130 L-C meter operating at about 130 kHz. The results are as follows:

Hughes no.	99	6.5 pF
	98	6.3
	96	6.1
Fischer	250 A-1500-N	6.4
	250 A-800-N	7.4
	350 A-1500-N	7.6
	250 A-1000-N	6.[illegible]

TPD Mounting Fixture

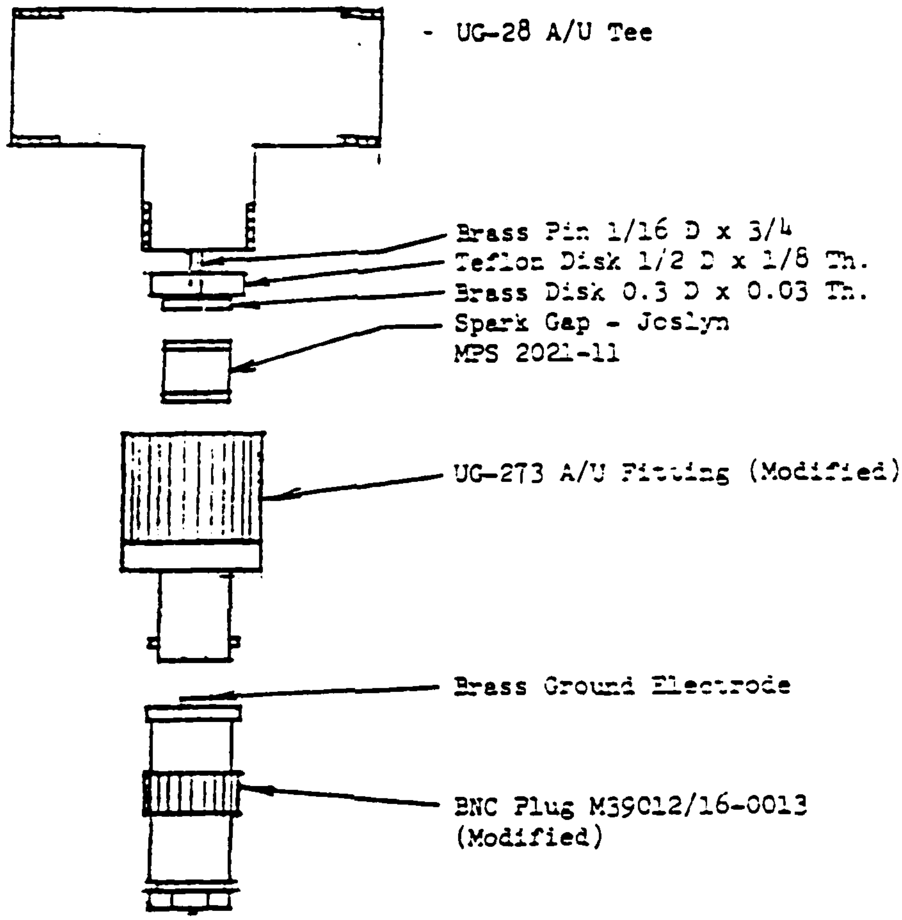


Figure 6.73 TPD Model 1 [6.21]

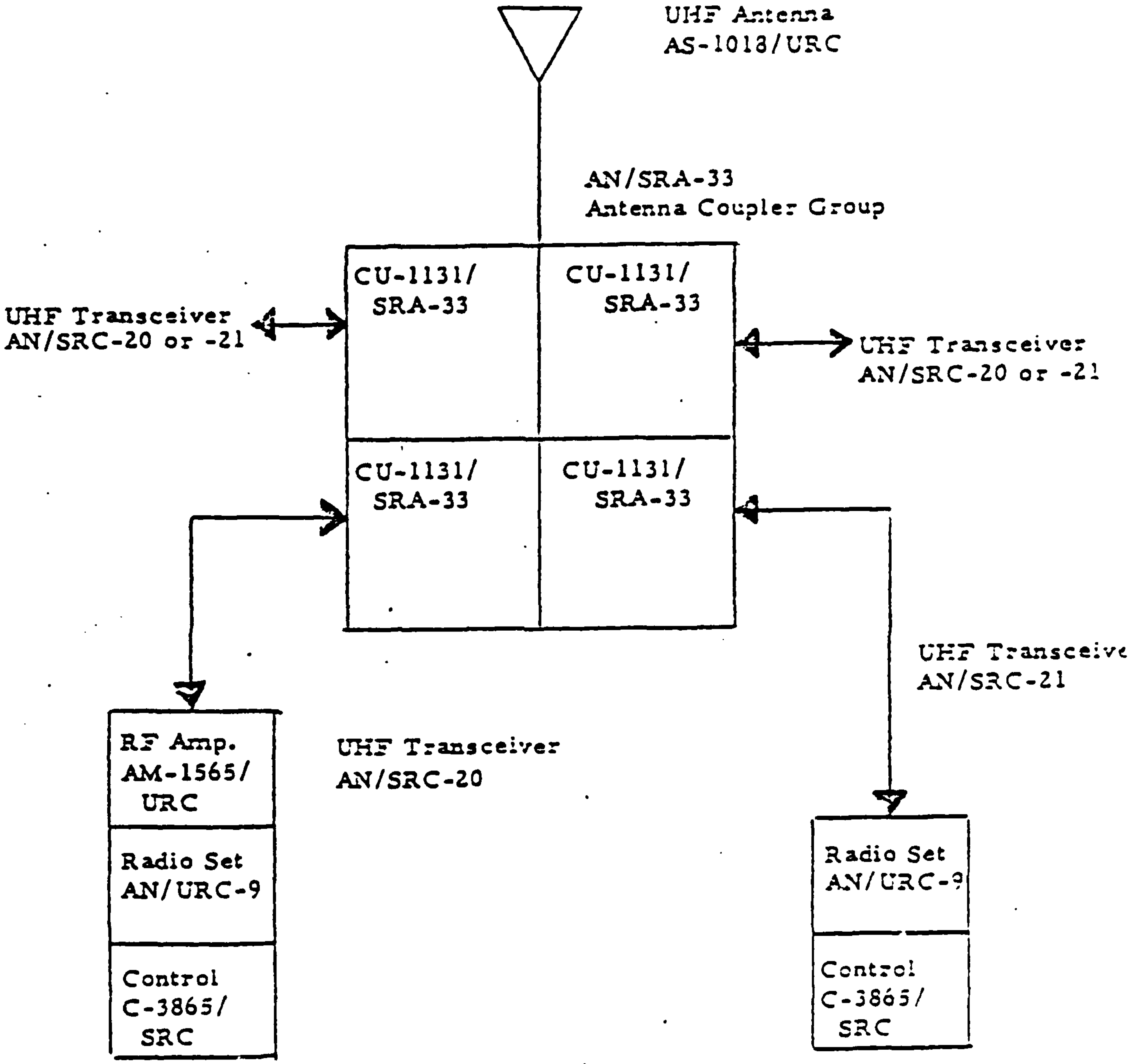


Figure 6.74 Block Diagram, UHF Antenna System [6.21]

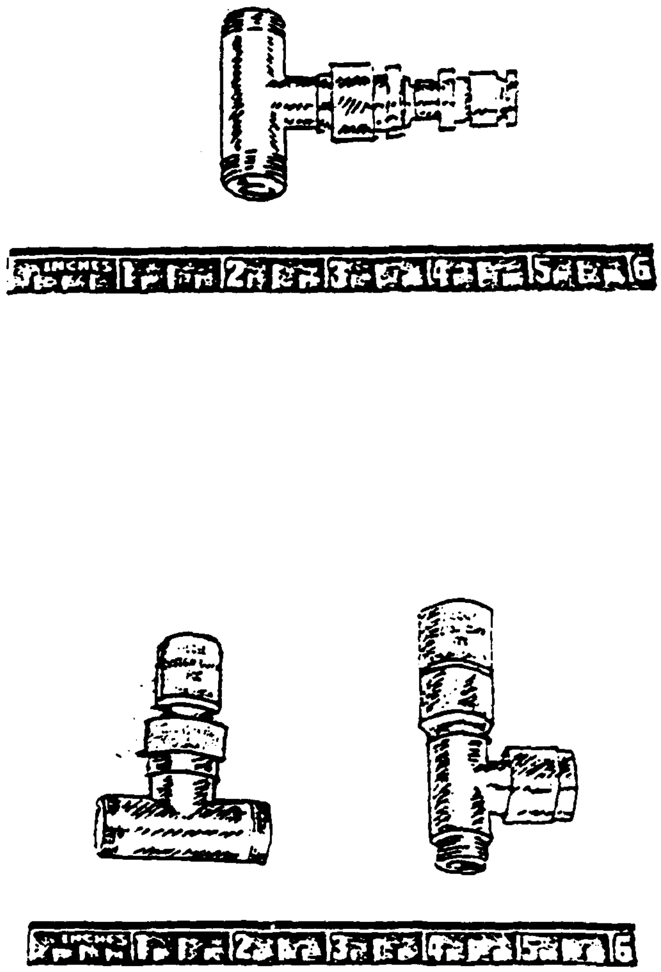


Figure 6.75 HUAC and Fischer UHF Protective Devices [6.75]

Time-Domain-Reflectometer measurements were made with the same experimental arrangement as used on the HF TPDs. These are shown in Figure 6.76. The shunt-capacitance effect from the gas-gap is readily apparent and is followed by a small increase in reflection coefficient from a small series-inductance effect.

Figure 6.77 is a block diagram of the UHF impedance measuring system. The HP 803A VHF/UHF Impedance Bridge operates over the frequency range of 50 MHz to 500 MHz and is a Byrne Bridge. Table 6.26 presents those data from measurements on the Hughes Device number 99 and the Fischer devices. With a few exceptions at the higher frequencies, all appear slightly capacitive as one would expect them to be.

Figure 6.78 is a block diamgram of the system for measuring the UHF insertion losses of the same previous devices. Losses are rather insignificant throughout the band, as shown in Table 6.27.

The power-handling capabilities of devices such as these are determined mainly by the Voltage-Standing-Wave-Ratio (VSWR) that they introduce into a system. Figure 6.79 is a block diagram of the system used to make these measurements. The standing-wave indicator is a type 219 from Polytechnic Research and Development Co. (PRD) and provides simultaneous direct indications of angle-of-voltage reflection-coefficient (for use with a Smith chart in Z determinations) and VSWR on an auxiliary VSWR amplifier - the HP 415 E. This is a tuned amplifier-voltmeter for detecting the one KHz, square-wave modulation of the RF source, and is calibrated such as to read-out directly in VSWR. Measurements were at a power-level of 1/4 watt (one watt attenuated six dB) with both a resistive load and an AS-390/SRC UHF antenna as a sink. Table 6.28 summarizes the resistive-load data for the devices tested.

The HUAC devices were then tested in this system feeding a real antenna, the AS-390/SRC, through 23.5 feet of RG-214. This antenna is a broadband coaxial stub antenna with a radial bent-rod counterpoise. The lower antenna section encloses a feed line and a tuning stub which can be rotated and locked in position during manufacture to provide the optimum input impedance. The design coverage is 220-400 MHz, but the antenna can be used over a wider frequency range with some decrease in performance. The antenna structure is sixteen inches high and the eight ground radials extend to a diameter of twenty-three inches. Table 6.29 presents these data with various configurations of the HUAC devices and this antenna.

In only one case of the above did the VSWR even approach the limiting ratio of three.

6.5.3.3 Harmonic and Intermodulation Generation

All seven of the UHF devices considered here were first tested in the HF system previously described and in no case were any third harmonics detectable with 85 watts at 4.044 MHz driving the resistive load. A harmonic level of -90 dBm was detectable at 600 watts and -96 dBm at 400 watts.

Two AN/WSC-3 UHF transmitters were combined with a CU-691/U antenna coupler for the system shown in Figure 6.80.

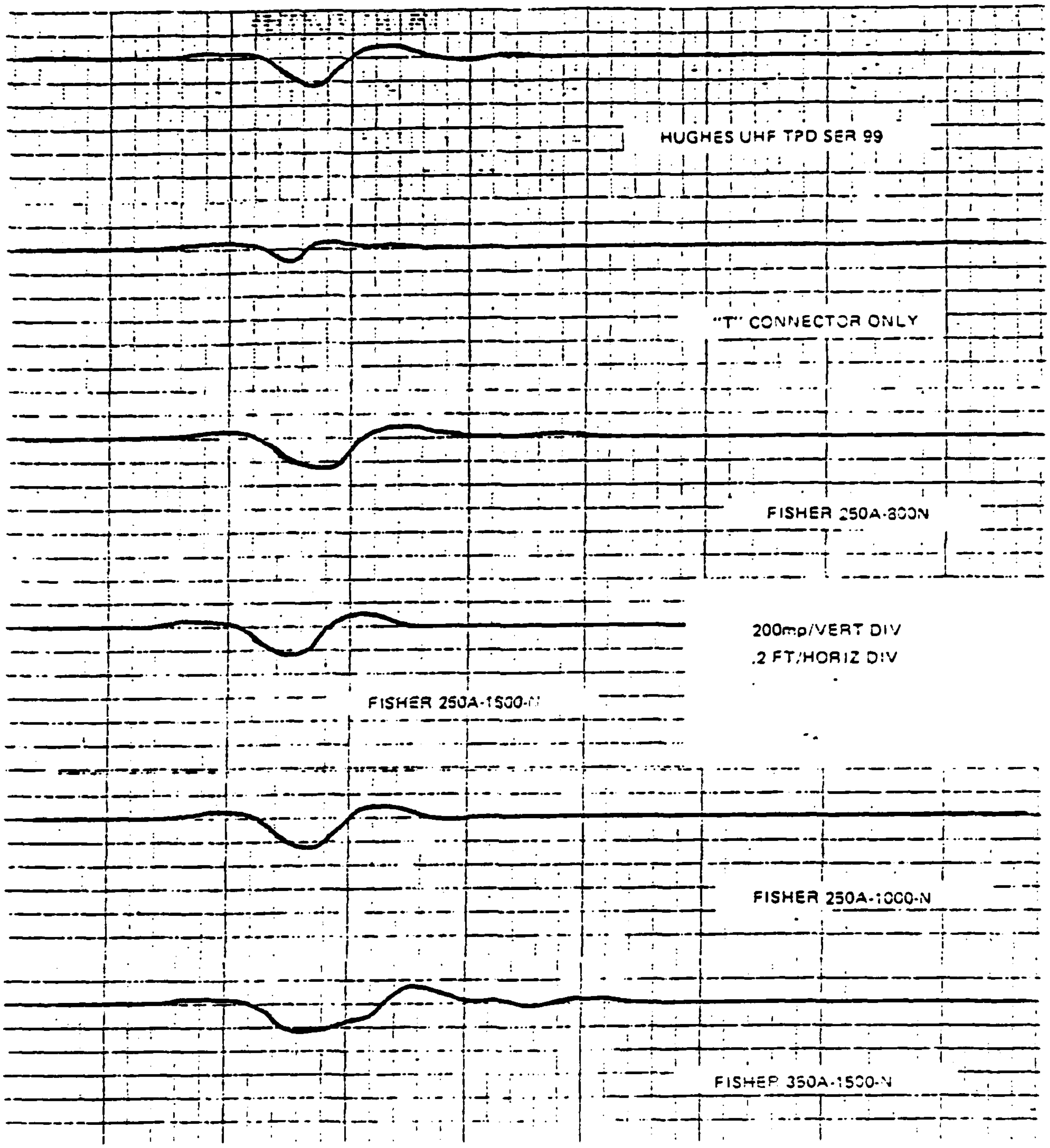


Figure 6.76 Time-Domain Reflectometer Oscillograms from UHF TPDs [6.25]

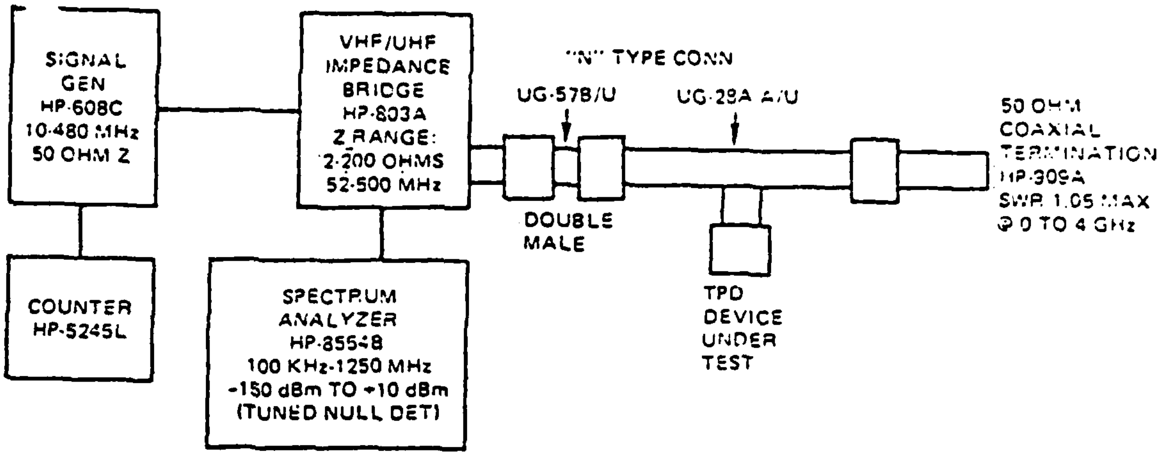


Figure 6.77 Impedance Measuring System for UHF TPDs [6.25]

Table 6.26 UHF TPD Impedance Measurement [6.25]

Frequency (MHz)	TPD	Z (ohms)	Phase Angle (deg.)
225	50 Ω load	50.0	0.0
	HUAC 99	39.0	-4.0
	250 A-1000	41.0	-3.0
	350 A-1500	41.0	-5.8
	250 A-1500	44.0	-3.8
	250 A-800	41.4	-5.1
300	50 Ω load	50	0.0
	HUAC 99	34	-1.5
350	50 Ω load	50.3	0.0
	HUAC 99	30.7	+0.9
400	50 Ω load	51.0	0.0
	HUAC 99	29.7	+2.5
	250 A-1000	33.6	+1.4
	350 A-1500	28.9	-2.0
	250 A-1500	35.2	-1.8
	250 A-800	30.4	-2.0

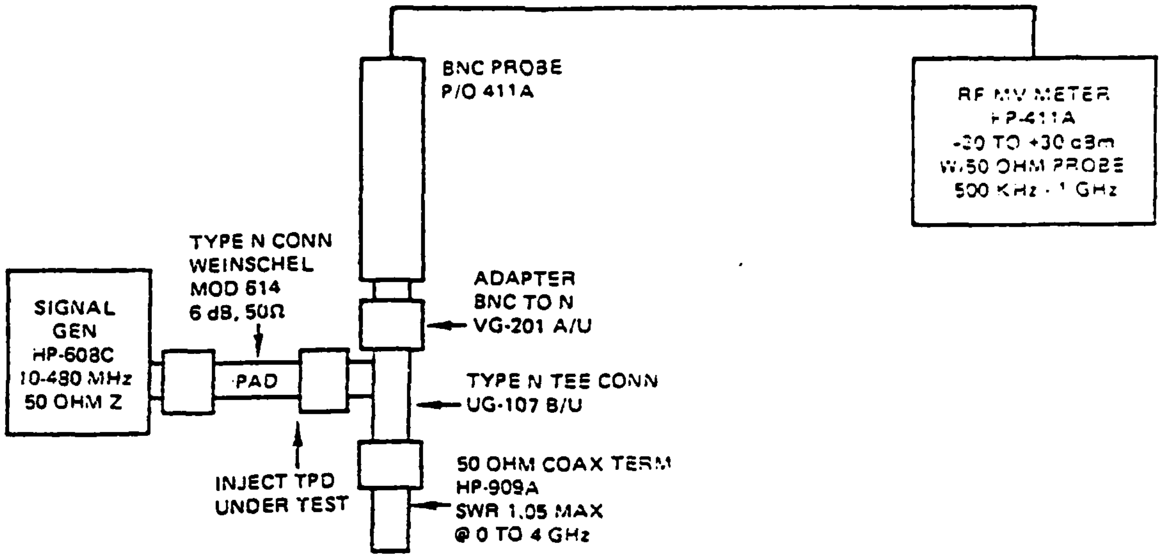


Figure 6.78 Insertion-Loss Measuring System for UHF TPD [6.25]

Table 6.27 UHF Insertion Loss Measurement [6.25]

Frequency (MHz)	TPD	Loss (dB)
225	HUAC 99	0.25
	250 A-1000	0.20
	350 A-1500	0.20
	250 A-1500	0.20
	250 A-800	0.20
300	HUAC 99	0.25
	250 A-1000	0.25
	350 A-1500	0.20
	250 A-1500	0.20
	250 A-800	0.20
400	HUAC 99	0.05
	250 A-1000	0.00
	350 A-1500	0.00
	250 A-1500	0.00
	250 A-800	0.00

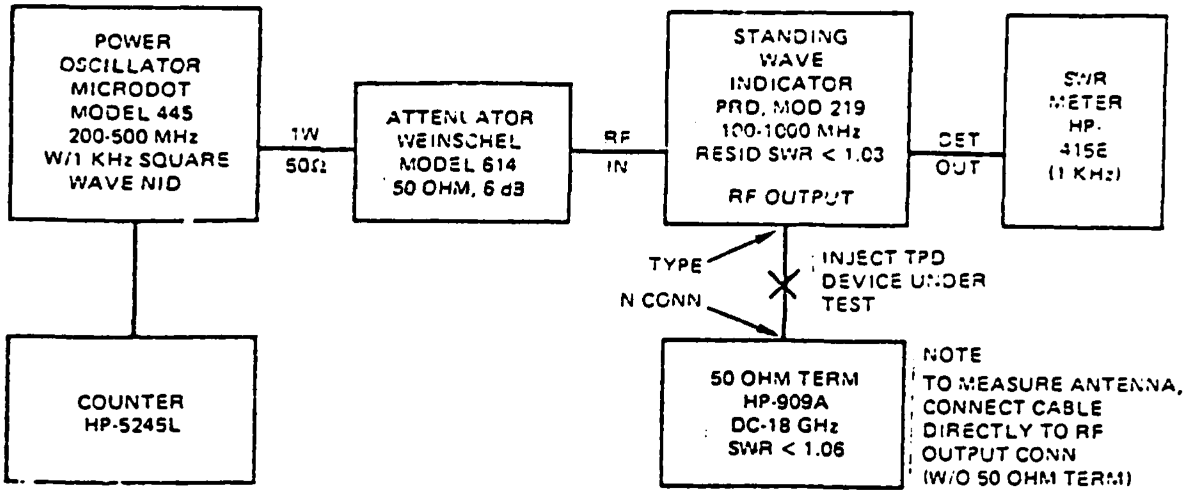


Figure 6.79 Intermodulation-Product Measuring System for UHF TPDs [6.25]

Table 6.28 VSWR for UHF TPDs Resistive Load [6.25]

Device	225 MHz	300 MHz	400 MHz
50 Ω load (no device)	1.028	1.03	1.026
HUAC 99	1.32	1.42	1.60
HUAC 98	1.29	1.36	1.53
HUAC 96	1.29	1.38	1.54
250 A-1000	1.24	1.30	1.41
350 A-1500	1.34	1.43	1.62
250 A-800	1.31	1.38	1.55
250 A-1500	1.22	1.26	1.38

Table 6.29 VSWR Data, HUAC TPDs and AS-390/SRC Ant. [6.25]

	300 MHz	400 MHz
Antenna only	1.43	1.85
Antenna + TPD 99 @ source	2.00	2.75
Antenna + TPD 99 @ ant.	1.66	2.00
Antenna + TPD 99 @ ant. + (98 @ source)	2.19	2.38

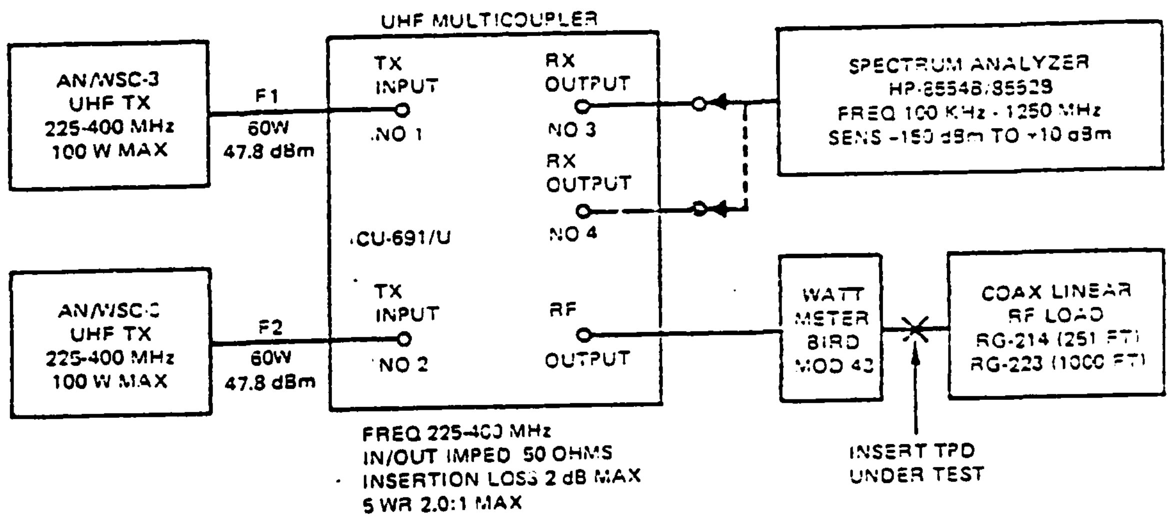


Figure 6.80 Intermodulation-Product Measuring System for UHF TPDs [6.25]

Two in-band frequencies, F_1 = 345 MHz and F_2 = 370 MHz were chosen for the first of these tests. Table 6.30 lists some of the possible intermodulation product frequencies to ninth order, with those that would fall within the band of interest marked with an asterisk. The 60 watts of power at F_1 and at F_2 is dissipated in the transmission line (4 dB/100 feet for the RG-214 and 8 dB/100 feet for the RG-223 for a total of 90 dB).

Figures 6.81 to 6.83 are oscillograms from the above system. In these figures F_1 and F_2 and the IM frequencies are of the order three in Table 6.30; the log reference (top of reticle) is -40 dBm with 10 dB/division; the center frequency is 300 MHz with 20 MHz/division scan. In Figure 6.81a are seen vestiges of leakage of F_1 and F_2 through the coupler port tuned to 395 MHz. In Figure 6.81b

Table 6.30 Some Intermodulation Product (IM) Frequencies F_1=345 MHz, F_2=370 MHz

$2F_1 - F_2 = 320$*	order 3
$2F_2 - F_1 = 395$*	
$3F_1 - 2F_2 = 295$*	order 5
$3F_2 - 2F_1 = 420$	
$4F_1 - 3F_2 = 270$*	order 7
$4F_2 - 3F_1 = 445$	
$5F_1 - 4F_2 = 245$*	order 9
$5F_2 - 4F_1 = 470$	

the two third order frequencies are simultaneously present (with a TPD in circuit F_1 and F_2 at 25 watts) by paralleling the two output ports of the coupler. Figures 6.82 and 6.83 are data from separate ports tuned to the appropriate IM frequencies. These data and those taken with the remaining TPDs are presented in Table 6.31.

A similar experiment as the above was then performed except that the driving frequencies were 280 MHz and 335 MHz to give a relatively strong IM at 2 x 280 - 335 = 225 MHz. As before, the driving power is 60 watts channel. Figure 6.84 shows oscillograms from the Fischer devices and Figure 6.85 shows those for the HUAC devices. It is interesting that no IM was observed for the Fischer 250A-1000 in Figure 6.84(b). In all but Figure 6.85(d) the log reference is -40 dBm. During the course of measuring HUAC 99 the IM level increased enormously. Compare (6.85(c) and 6.85(d)) to a level of -10 dBm (log reference of zero dBm) and was found to be caused by simply a "bad" connection at the gas-gap. Incidentally, a HP 410C voltmeter probe sufficed to introduce a similar IM of -53 dBm level.

6.5.3.4 Noise Figure Effects

Noise generation by the UHF TPDs was looked for by including them in the input of a RSR-20 receiver. This was fed with input signals at 225 and 400 MHz from a HP 608C signal generator modulated 90% at 1 KHz. At 6 μv input a GR 583-A output-power-meter indicated a (S + N)/N of 23 dB at the receiver output. The presence of any of the UHF TPDs had no effect at this level. With or without the devices, the minimum detectable signal was 0.16 μv. The devices have no effect upon noise-figure.

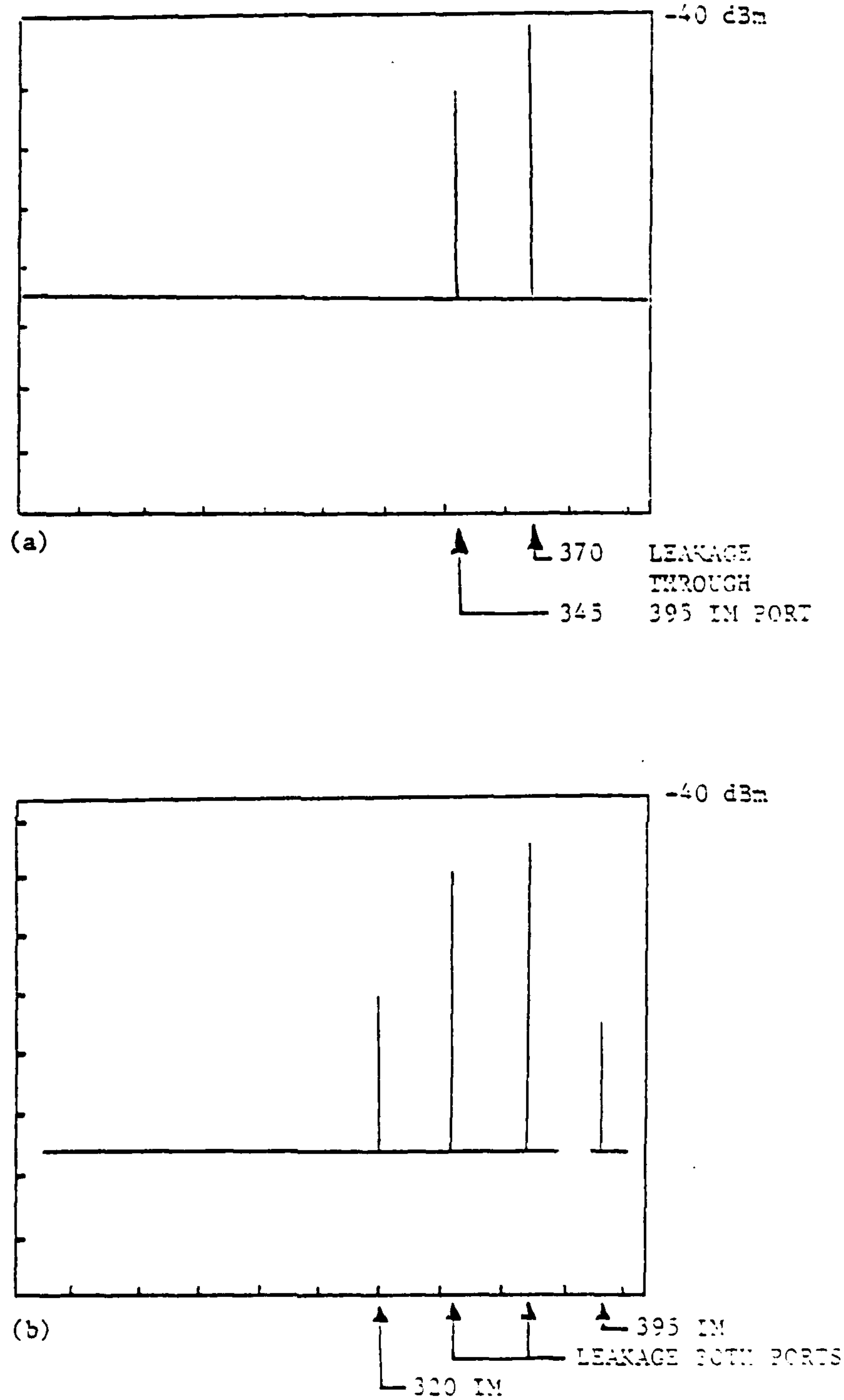


Figure 6.81(a) Leakge of 370 and 345 MHz Signals (60 Watt) Trough Output Port Tuned to 395 MHz
(b) Leakage and IM Signals Parallel Port with TPD [6.25]

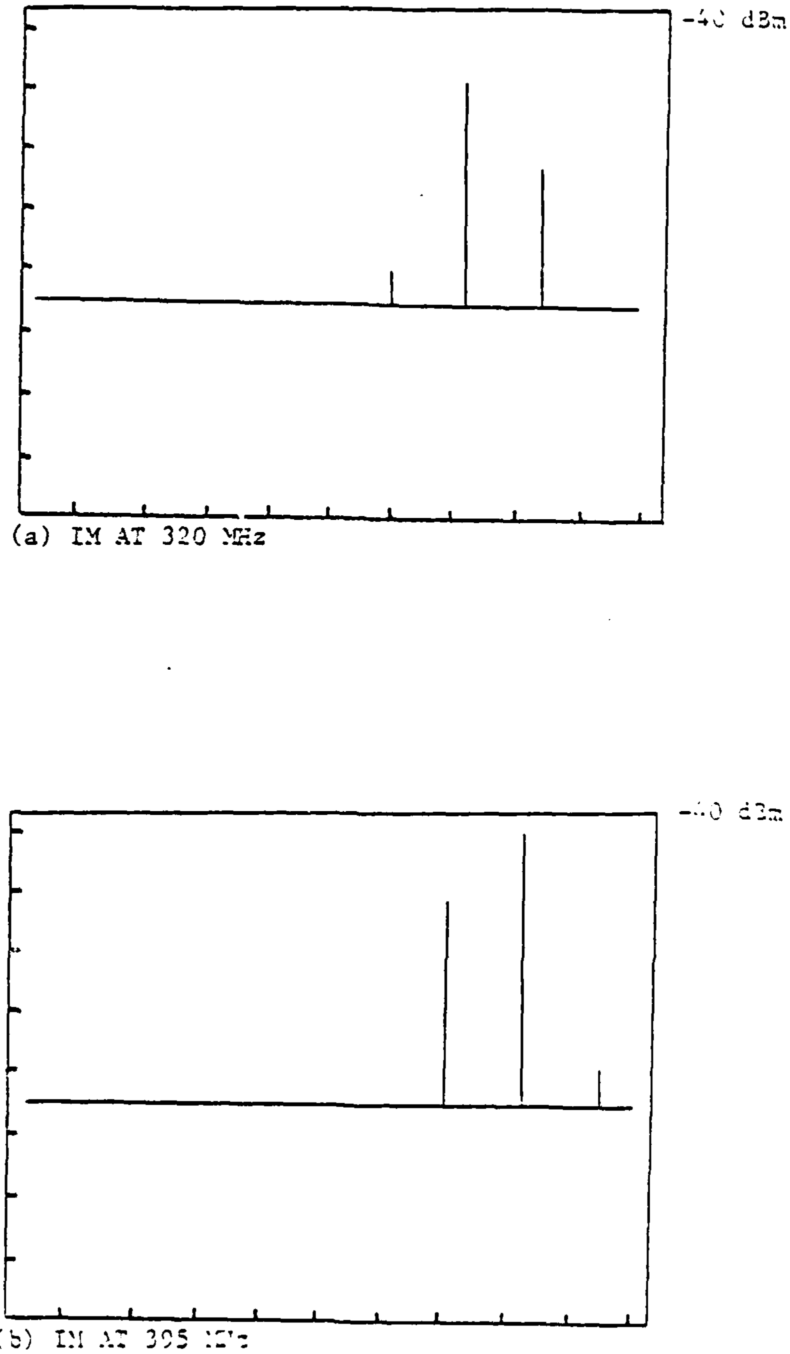
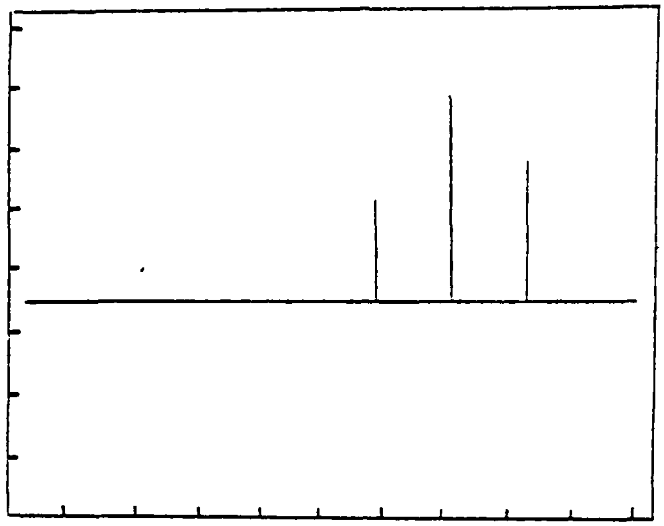
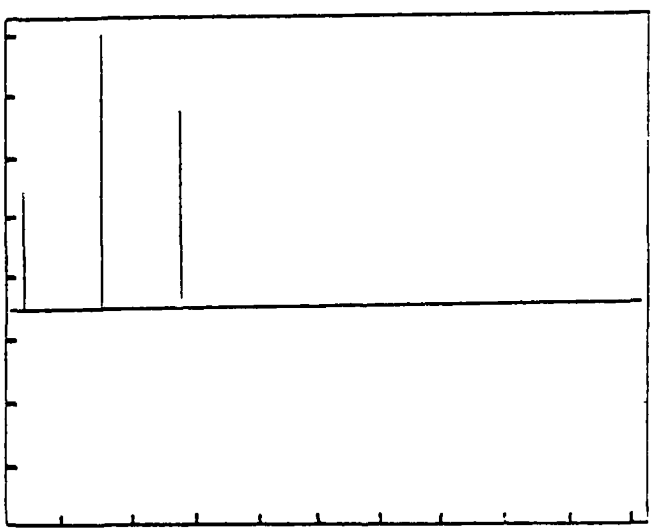


Figure 6.82 Intermodulation Signals (Third Order) from Fischer Device 250 A-1500 [6.25]



(a) IM AT 320 MHz



(b) IM AT 395 MHz

Figure 6.83 Intermodulation Signals for HLAC Device 96, [6.25]

Table 6.31 IM Power Level (dBm), 47.3 dBm Driving [6.25]

Device	320 MHz IM	395 MHz IM
150 A-800	-83	-82
250 A-1000	< -85	< -85
250 A-1500	-76 (Fig. 7.8)	-76
350 A-1500	-76	-74
HUAC 96	-66 (Fig. 7.9)	-65
HUAC 98	-65	-66
HUAC 99	-64	-63

6.5.3.5 VHF/UHF TPD Discussion

From these experiments in developing compatibility test procedures it is rather apparent that harmonic and intermodulation product generation is a major compatibility consideration in systems design utilizing protective devices. Further tests are in order for intermodulation product generation in HF TPDs which incorporate semiconductor devices. It is quite possible that these types of devices will be applicable only at the low-level conditions existing at receiver inputs thus complicating the problem of transmitters and transceivers. The following statements are in order at this stage of the investigation.

a. Multi-transmitter tests on devices at HF need to be done.

b. Power handling capability of the TPDs appears to be adequate, however definitive time duration tests with multiple threat level firings of the devices have yet to be done. Maximum power tests in normal operations have yet to be done.

c. Each TPD manufactured not just a "type" should be individually tested in a system.

d. Wherever possible, dissimilar metal junctions are to be avoided in fabrication of TPDs.

e. Ferromagnetic (and hence nonlinear) materials in spark gaps, devices, conductors, and/or shields are to be avoided where possible; especially at or in the proximity of high rf current carrying conductors.

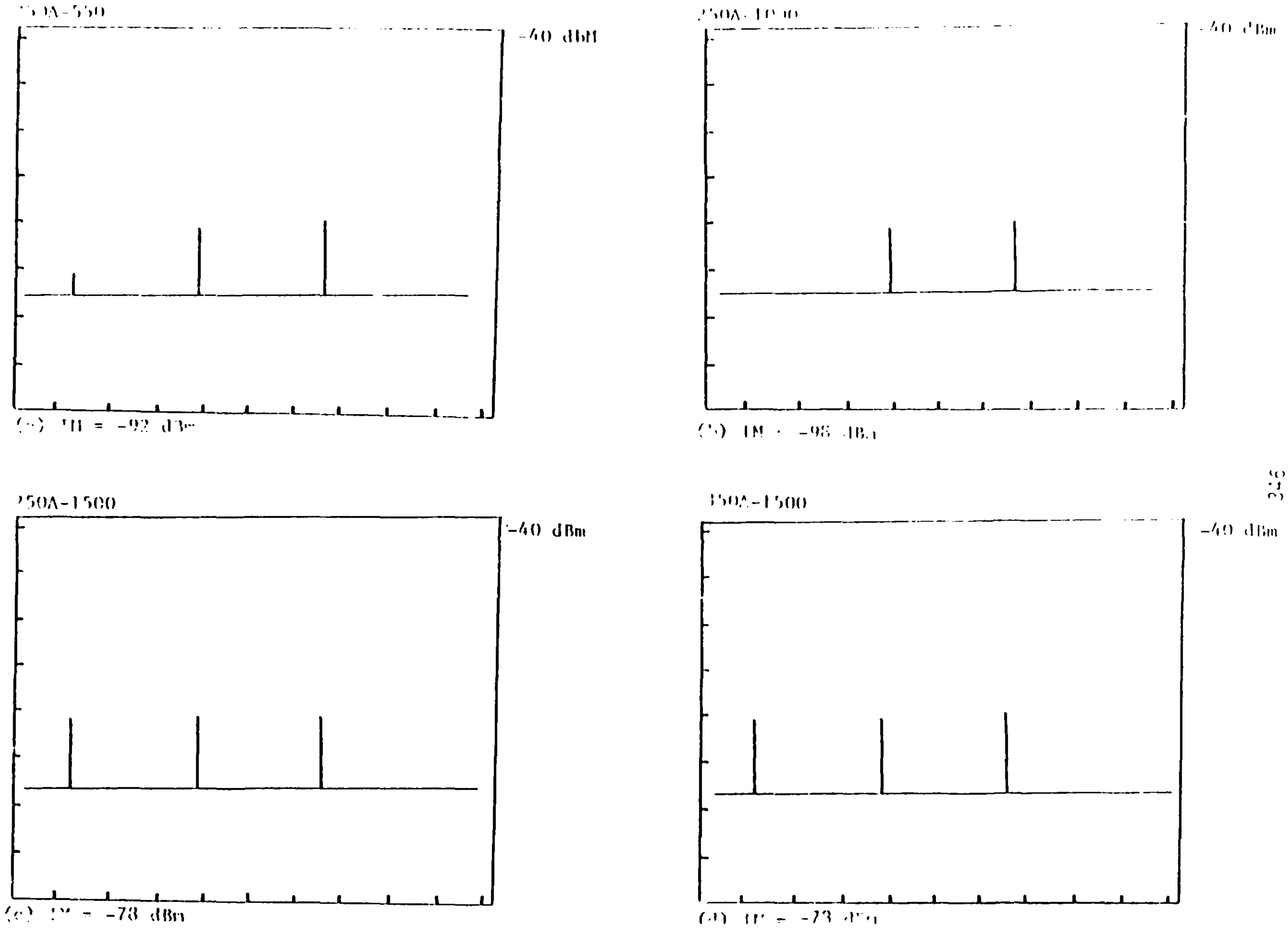
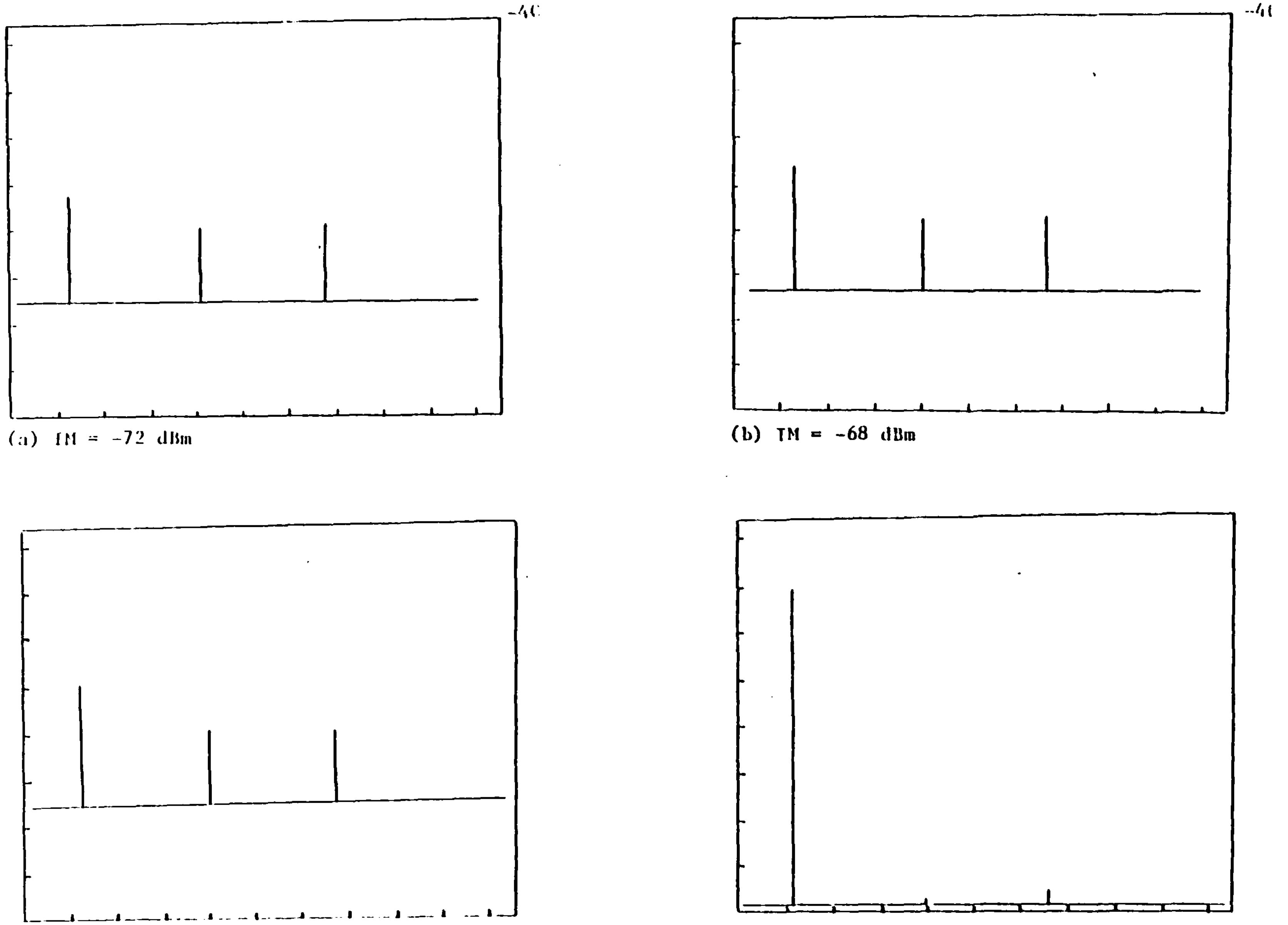


Figure 6.84 Fischer Devices, Intermod at 225 MHz [6.25]



(a) TM = -72 dBm

(b) TM = -68 dBm

(c) TM = -6[illegible] dBm

(d) TM = -10 dBm

Figure 6.85 HUAC Devices, Intermod at 225 MHz [6.25]

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CHAPTER 7

UPSET AND UPSET HARDENING

7.0 Executive Summary

Electromagnetic pulse (EMP) induced transients can be interpreted as data by digital processor or can temporarily saturate lentear devices. Although devices are not damaged, false information could be generated or desired information could be lost. These types of transient effects are generally termed upset. Upset may or may not affect mission completion.

Chapter 7 discusses the general problem of circuit upset and general techniques for hardening sensitive circuits to upset. Upset is dependent upon mutual coupling between circuit components (circuit geometry, i.e., printed circuit board layout) as well as the type of circuitry. The must susceptible type of circuitry is digital logic circuitry. The majority of this chapter contains methods for hardening digital systems from both a hardware and software approach.

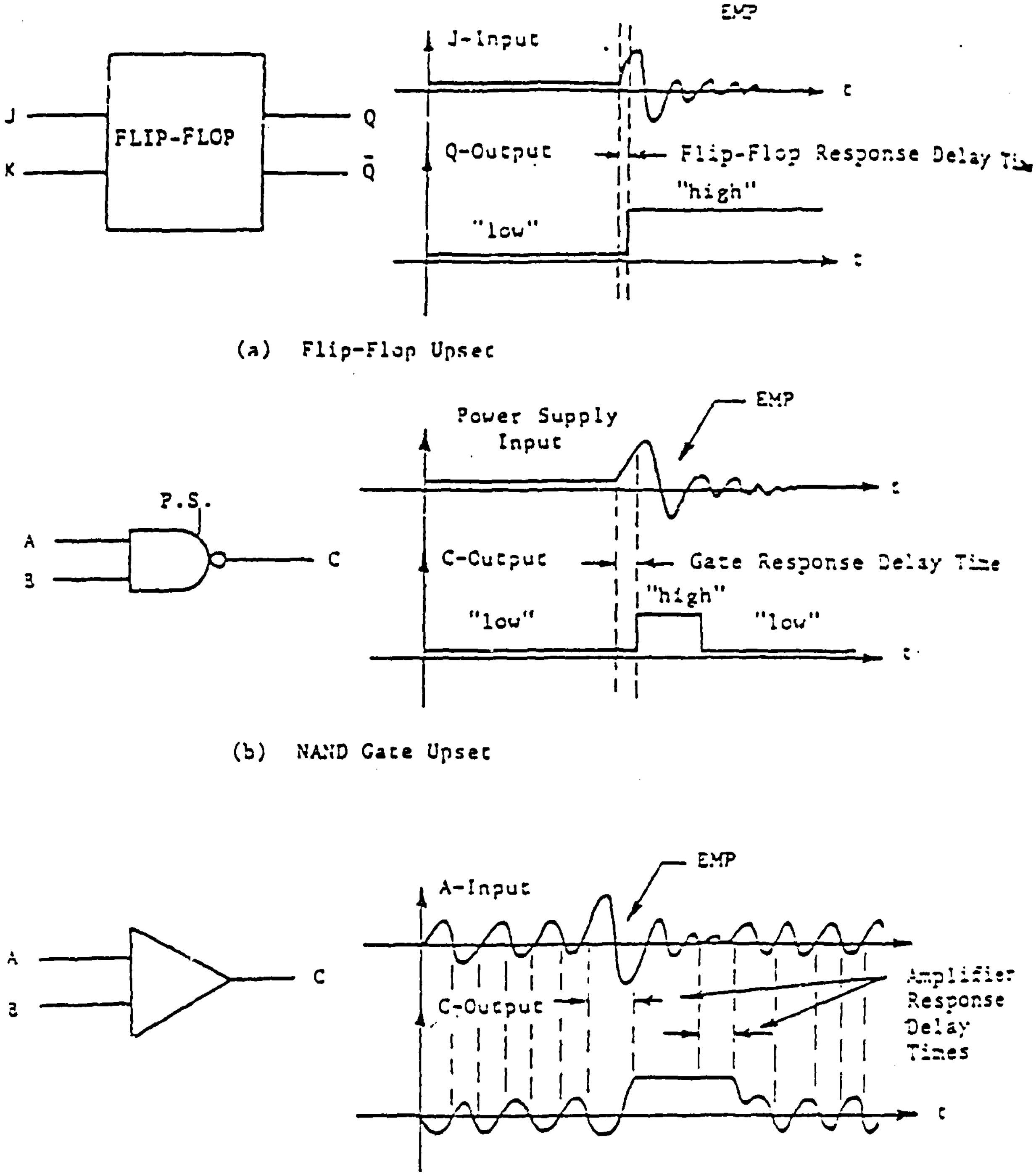
7.1 Introduction

Preceding chapters discussed the coupling of EMP energy into shipboard equipment. The energy enters equipment mainly through shield discontinuities and eventually appears on the center conductors of shielded cables. These cables efficiently transmit the energy to the electronics in which they are terminated. This EMP energy can cause system or circuit degradation in one of two ways. First, if the energy is large enough, components can be permanently damaged. Second, if not large enough to damage components, the energy may cause the electronics to respond in a deleterious manner and degrade system performance. This is called upset. Although upset generally occurs at lower energy levels than does component damage, this is not always the case [7.1]. In this chapter, circuit upset will be discussed.

Section 7.2 illustrates an example of upset. Section 7.3 discusses methods of estimating upset thresholds. Sections 7.4 and 7.5 discuss methods of hardening circuits to upset at the component and system level, respectively. Finally, Section 7.6 dicusses methods of upset hardening by system component selection.

7.2 Examples of Upset

Figures 7.1 [7.2] illustrates three types of possible upset. Part (a) shows a flip-flop responding to an EMP on the J-input. The flip-flop changes state, and the spurious data represented by this changed state could cause degradation in system performance. Part (b) shows a NAND gate changing state in response to EMP on the power supply input. The system could recognize the EMP as data, and the performance degradation would result. Part (c) shows a linear amplifier driven into saturation by an EMP signal superimposed on the input signal. Here, data could be lost while the amplifier is saturated, and again system performance would be degraded. System upset is defined as follows: if system performance is degraded, upset has occurred; if system performance is not degraded, upset has not occurred.



(a) Flip-Flop Upset

(b) NAND Gate Upset

(c) Amplifier Upset

Figure 7.1 Examples of Anomalous Circuit Response [7.2]

7.3 Threshold Analysis

Before designing an upset-hardened system, the designer needs a set of criteria stating the thresholds at which circuit upset may occur. For example, Figure 7.2 [7.3] shows a disturbing transient along with three circuit upset threshold levels. Here Circuit A is upset for a long time. T_1. and circuit C is not upset at all. The circuit upset threshold depends not only on the transient amplitude, but also upon the length of time the amplitude exeeds a certain level. The upset threshold depends upon the device fabrication, device type, and type of coupling between devices. Generally, digital devices are more prone to upset than linear devices; DC-coupled devices are more sensitive than ac-coupled devices; and integrated circuit devices are more sensitive than discrete devices. Figure 7.3 [7.4] illustrates the general nature of digital circuit upset as a function of upset signal frequency.

A conservative estimate of the voltage required to cause upset (V_u) can be obtained in terms of the DC upset threshold voltage (V_{dc}), the circuit propagation delay time (t_{pd}) (i.e., the time it takes a pulse to appear at the output when injected on the input), and the actual pulse width (t_u), according to the relationship

$$V_u = V_{dc} \left(\frac{t_{pd}}{t_u}\right)^{1/2} \tag{7.1}$$

This formula, which applies if $t_u < t_{pd}$, provides a conservative estimate. Figure 7.4 [7.4] shows the comparison between the measured and predicted values of the upset voltage V_u for a pulse applied on the input of an integrated circuit (I.C.) flip-flop. It can be seen that (7.1) predicts a lower voltage and is, therefore, conservative. In some cases, the formula may be too conservative and may cause unacceptable hardening penalties. In these cases more detailed analysis and testing could be required. Because an EMP transient may appear on more than one terminal of a device simultaneously, multiport analysis or testing may be required.

Reference 7.1 reports that transient upset is largely independent of the wave shape and that it depends mainly upon the peak value of the transient and on the length of time it exceeds the DC threshold. Therefore, testing may be performed with rectangular wave pulses. An EMP pulse is usually in the form of a damped sinusoid; therefore, a relation is needed between a rectangular pulse and a damped sinusoid. From Chapter 5, the relationship is:

$$f = \frac{1}{1.3t}, \tag{7.2}$$

where f is the damped sinusoid frequency, and t is the rectangular pulse width. If (7.2) is satisfied, the amplitude of the rectangular pulse which causes upset is the same as the amplitude of the damped sinusoid which would cause upset.

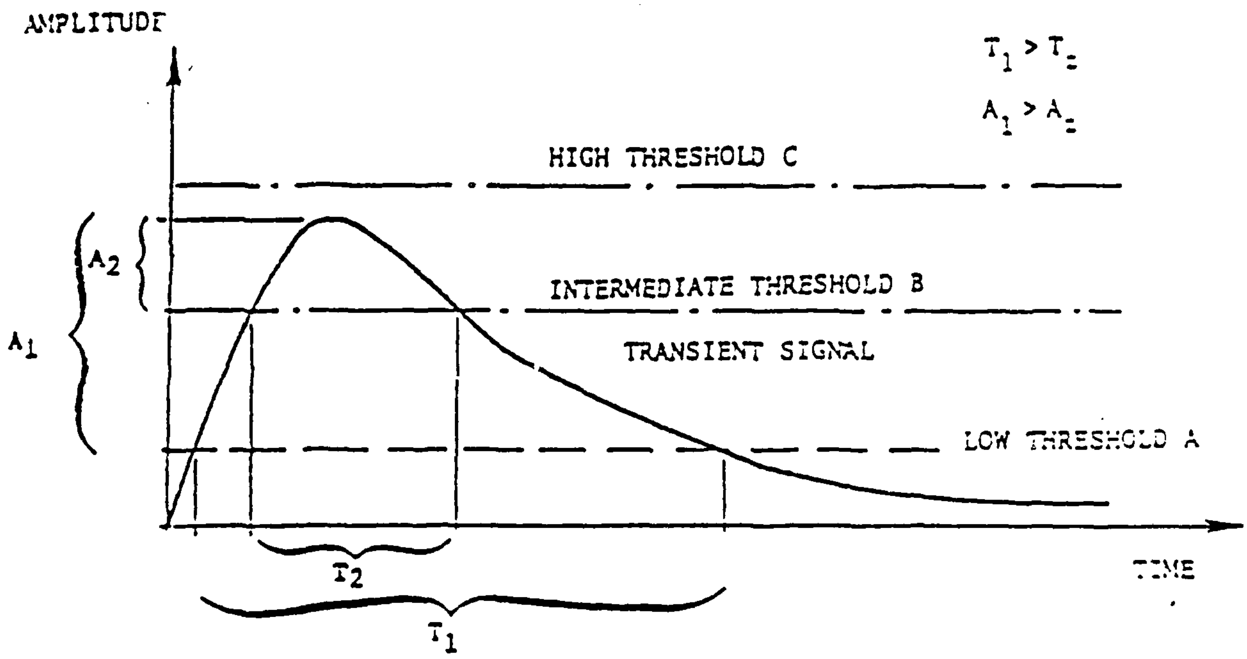


Figure 7.2 Circuit Threshold [7.3]

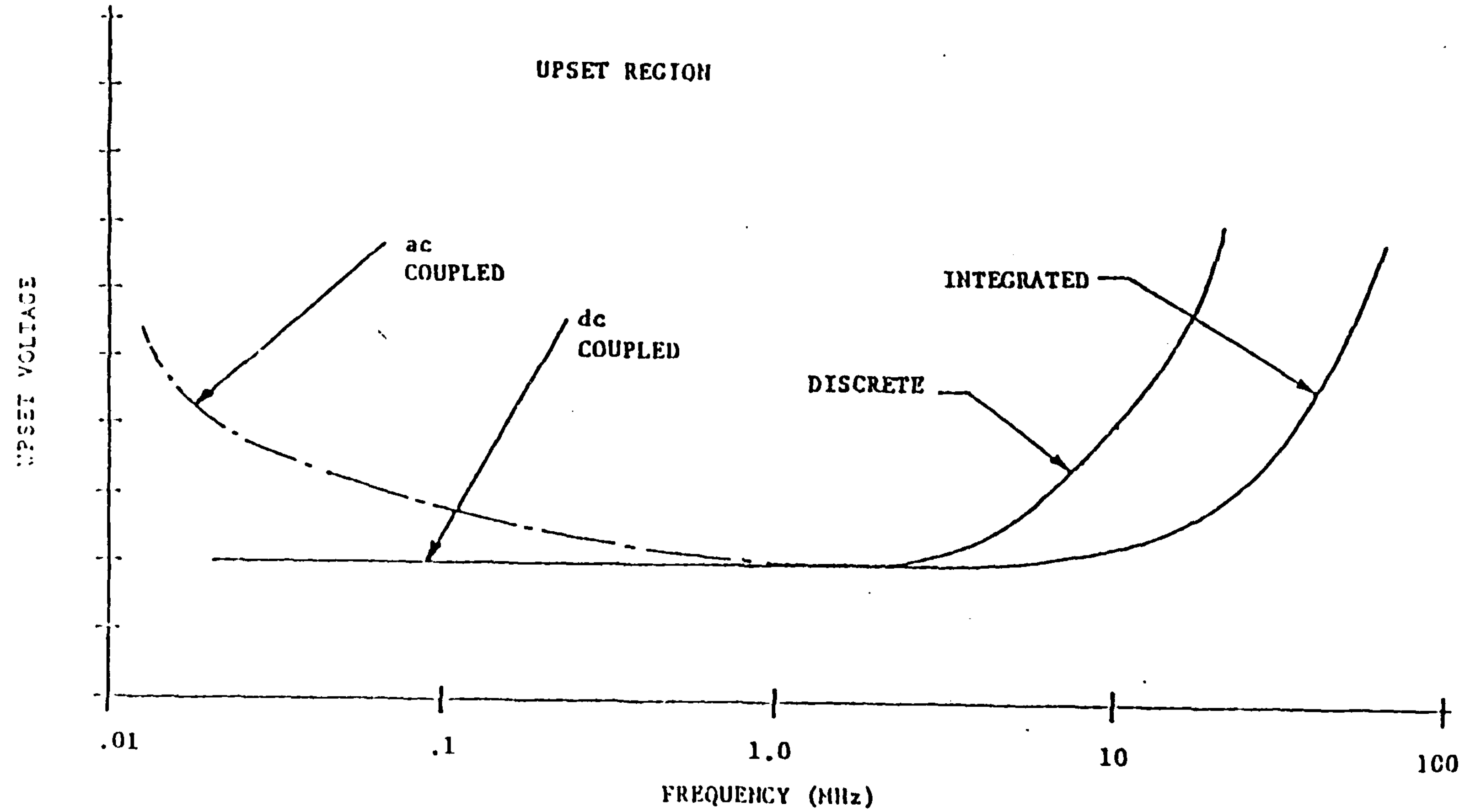


Figure 7.3 Digital Circuit Upset Threshold Trends [7.4]

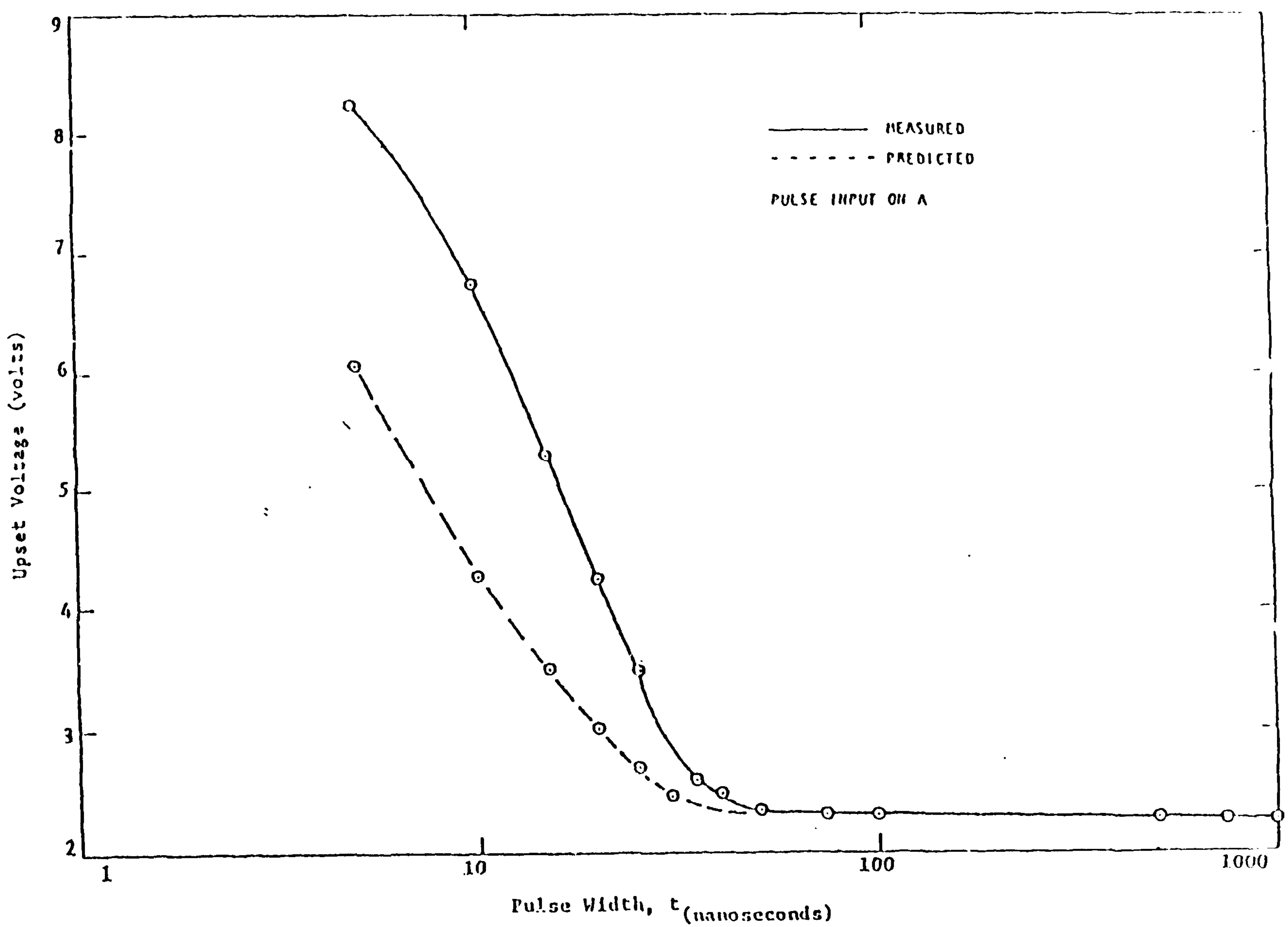


Figure 7.4 Comparison of Predicted and Measured Upset Levels for Short Pulse Durations [7.4]

In order to use (7.1), t_{pd} and V_{dc} must be known. t_{pd} is usually specified on a manufacturer's data sheet, but V_{dc}, which may often be found from DC analysis of the circuit involved, often depends upon the original logic state of the circuit, i.e., the upset voltage to change from a logical "1" state to a logical "0" state may be different than that required to change from a logical "0" state to a logical "1" state.

A simple example of calculating the DC threshold is given in Figure 7.5 [7.5]. This figure shows the input circuit for a Sandia Laboratories radiation-hardened nonsaturating DTL (diode transistor logic) dual four-input gate, constructed with dielectric isolation and thin-film resistors. It has a low noise margin (1.2V), high speed (10-nsec propagation time), and medium supply voltage (+9 V). Assume that the input is being held near ground potential (logical zero). Now, notice that the input will cause current to flow into T_1 if it is raised high enough to let current flow through the two diodes and transistors T_1 and T_2. If the semiconductor junction forward voltage drops are all equal to V_0, the input must be increased to $3V_0$ before balance is achieved. For silicon diodes and transistors, the voltage V_0 is about 0.6 V; therefore, the DC threshold for this configuration is approximately 1.8V. Conversely, the DC threshold for turning T_1 and T_2 conduction off is $3V_0$ -9.0 or -7.2 V. This means that the transient necessary for turn-on must be at least 1.8 V, and the transient for turn-off must be at least -7.2 V. Unbalance of this sort is undesirable from an EMP hardness standpoint, if the smaller sensitivity is undesirably small.

Often the analysis will not be so simple, and computer analysis using some of the network analysis programs (ECAP, TRAC, SCEPTRE, CIRCUS 2, NET-2, etc.) may be required. Reference 7.4 which discusses threshold analysis in more detail, contains some more difficult sample problems.

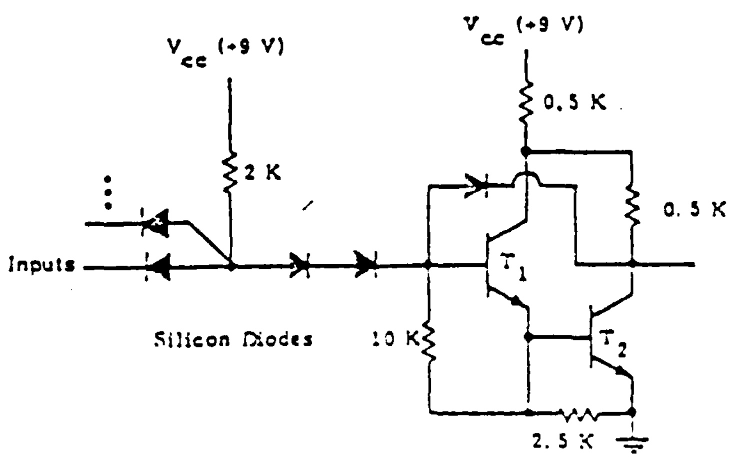
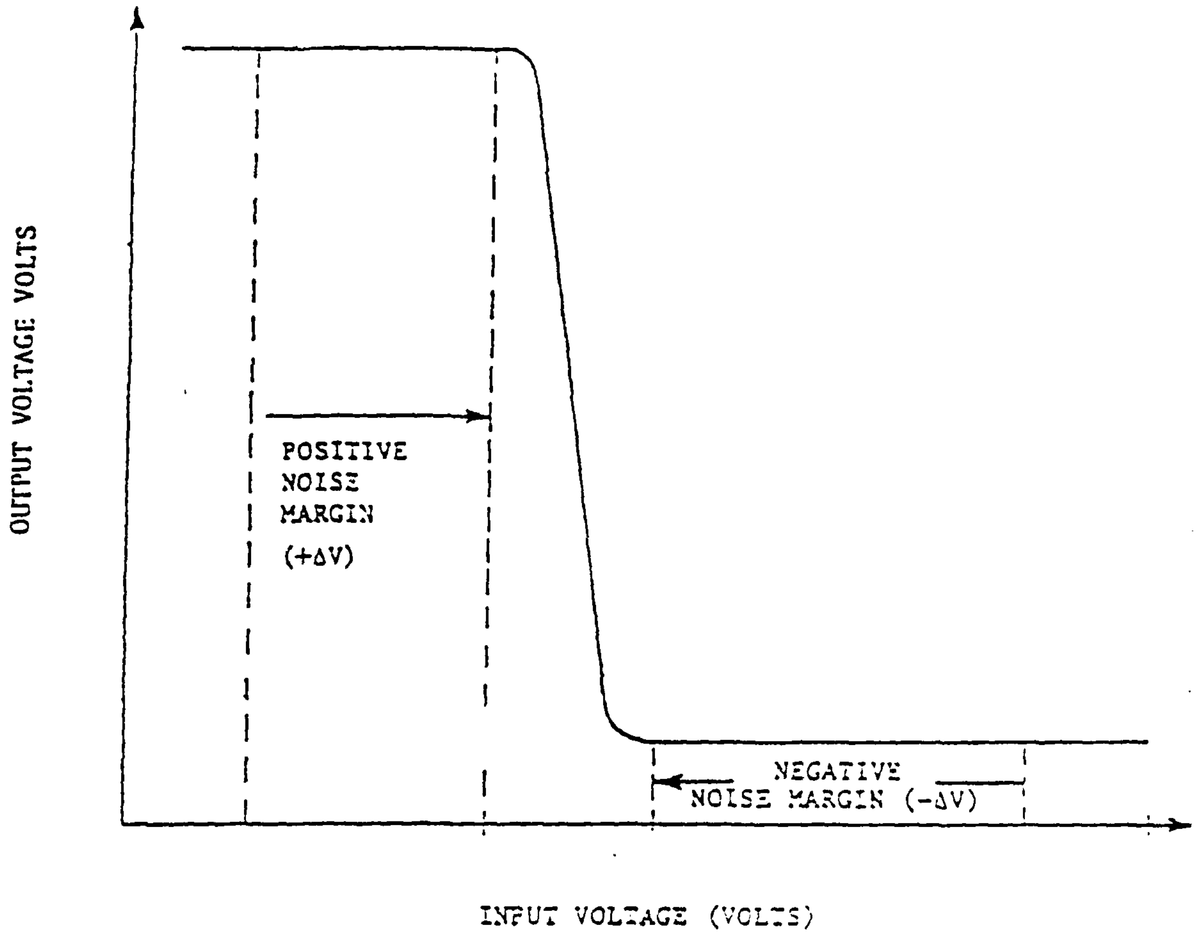
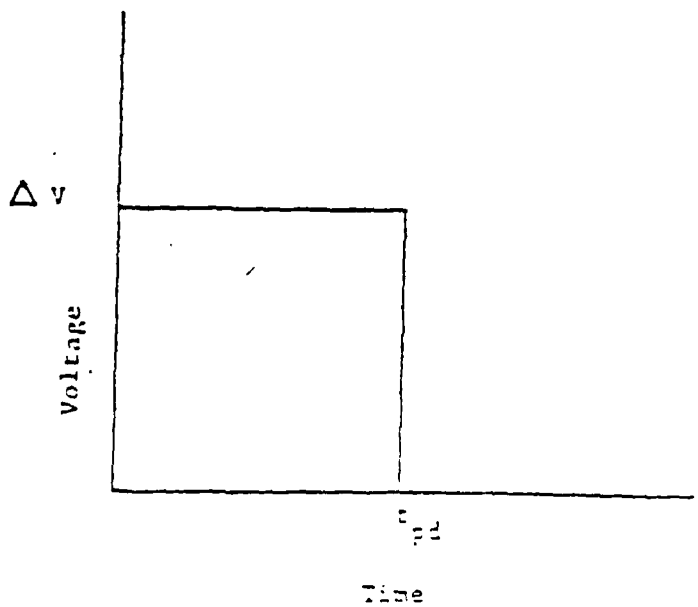


Figure 7.5 Input Circuitry for Sandia DTL Gate [7.5]



(a) IC Transfer Function



(b) Minimum V-T Characteristic for Upset

Figure 7.5 Typical Logic Transfer Function [illegible]

7.4 Subsystem Upset Hardening

7.4.1 Component Selection Hardening

Some degree of circuit hardening can be obtained by proper selection of components. The basic idea is to choose components whose frequency response and amplitude response are sufficient to perform the primary circuit function, but no better. This applies mainly to digital electronics and has limited application to linear circuits.

Figure 7.6 [7.2] illustrates a digital transfer function. Part (a) is the voltage transfer function, which shows the positive and negative noise margins, ΔV. If an EMP signal larger than ΔV is present for at least as long as the propatation delay, t_{pd}, upset will occur. Part (b) illustrates the minimum voltage-time characteristic for upset. Of course, this makes sense if the positive and negative noise margins are equal, which is desirable, only because an EMP signal is bipolar. It is clear that component hardening means to increase ΔV and t_{pd}. But increased ΔV means an increase in logic supply voltage and power dissipation. Increased t_{pd} means a slower data rate.

Common integrated circuit logic families are RTL (resistor-transistor logic), DTL (diode-transistor logic), TTL (transistor-transistor logic), ECL (emitter-coupled logic), HTL (high threshold logic), P-MOS (p-channel MOS logic), and C-MOS (complementary MOS logic). Tables 7.1 and 7.2 [7.2] show comparisons of the various logic families. Table 7.1 shows the t_{pd} N.I. (time delay-noise immunity) product, which may be regarded as an EMP figure of merit. Table 7.2 is a compilation of a large number of parameters.

Figure 7.7 [7.2] illustrates the improvement in noise immunity that can be obtained by choosing HTL instead of DTL. One could obtain higher noise immunity with discrete logic, if the cost, reliability, and size penalties are acceptable.

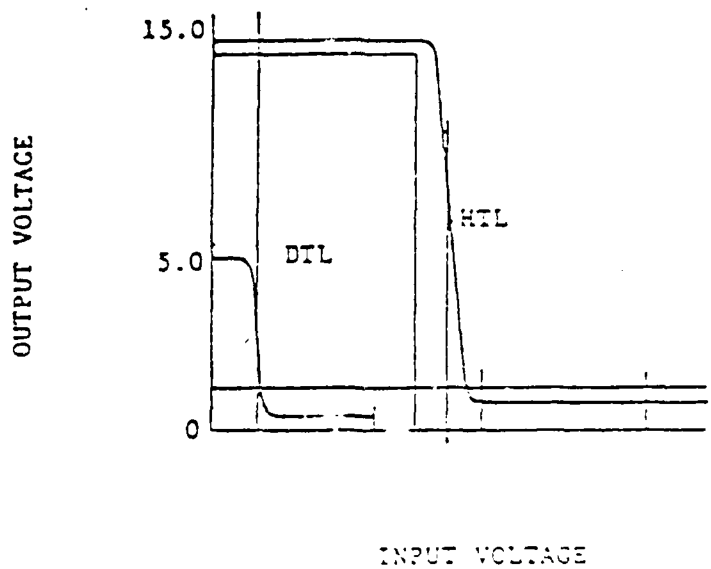


Figure 7.7 Logic Family Transfer Function Comparison [7.2]

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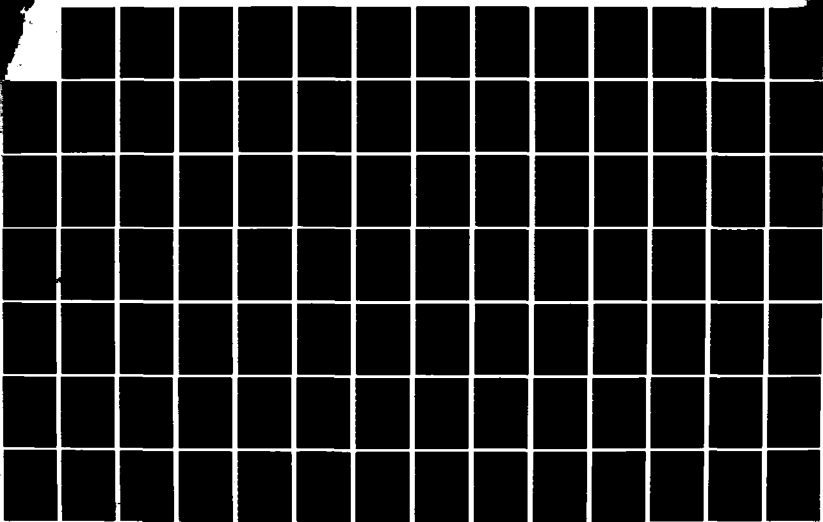

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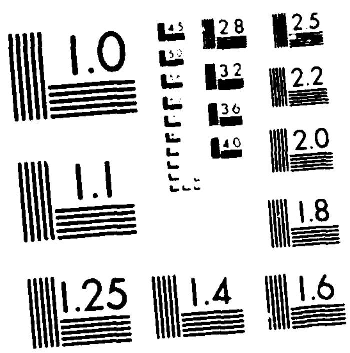


MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

Table 7.1 Digital Logic Family Comparison Matrix [7.2]

TYPICAL DC NOISE MARGIN. (VOLTS)	MAX INPUT IMPEDANCE (OHMS)	DC PROPAGATION DELAY RANGE (ns) 100 — 10 — 1	T_{pd} N.I.* PRODUCT (NS×VOLTS)	GATE POWER DISS. (mW)
1.21-6.5	0-100 >100	CMOS HTL PMOS	75-1500 200-800 200-2000	.02-2.0** 20-200 10-125
.81-1.2	0-100 >100	TTL DTL	6-50 12-66	1-70 2-70
.41-.80	0-100 >100			
0-.40	0-100 >100	ECL RTL	.25-2.0 .6-8.0	30-110 2-20

* Propagation delay time (T_{pd}), noise immunity (N.I.) product.

** In Microwatts

Table 7.2 Comparison Chart of the Major IC Digital Logic Families [7.2]

	Parameters	RTL	Low-Power RTL	DTL	HTL	12-ns TTL	6-ns TTL	4-ns ECL	2-ns ECL	1-ns ECL	P-MOS	CMOS
1	Circuit form	← resistor-transistor →		diode-transistor	diode-zener transistor	← transistor-transistor →		emitter-coupled current mode →			p-channel MOS	Complementary MOS
2	Positive logic function of basic gate	← NOR →		← NAND →				← OR/NOR →			NAND	NOR or NAND
3	Wired positive logic function	← Implied AND (same functions) →		Implied AND	Implied AND (A-O-I)	← AND-OR-INVERT →		Implied OR (all functions)			← none →	
4	Typical high-level Z_{in} ohms	640	3.6 k	6 k or 2 k	13 k or 1.5 k	70	10	18	6	6	2 k	1.5 k
5	Typical low-level Z_o	R_{sat}	R_{sat}	R_{sat}	R_{sat}	R_{sat}	R_{sat}	15 ohms or 2.7 mA	6 ohms or 6.7 mA	.6 ohms or 21 mA	25 k	1.5 k
6	Fanout	5	4	8	10	10	10	25	25 inputs or 50 ohms	10 low-Z inputs or 50 ohms	20	50 or higher
7	Specified Temperature Range, °C	-55 to 125 0 to 75 15 to 55	-55 to 125 0 to 75 15 to 55	-55 to 125 0 to 75	-30 to 75	-55 to 125 0 to 70	-55 to 125 0 to 75	-55 to 125	-55 to 125 0 to 75	0 to 75	-55 to 125 0 to 75	-55 to 125
8	Supply voltage	3.0V ± 10% 3.6V ± 10%	3.0V ± 10% 3.6V ± 10%	5.0V ± 10%	15 ± 1 V	5.0V ± 10% 5.0V ± 5%	5.0V ± 10% 5.0V ± 5%	-5.2V + 20% - 10%	-5.2V + 20% - 10%	-5.2V ± 10%	-27 ± 2V -13 ± 1V	4.5 to 16V
9	Typical power dissipation per gate	12 mW	2.5 mW	8 mW or 12 mW	55 mW	12 mW	22 mW	40 mW	55 mW plus load	55 mW plus load	0.2 to 10 mW	0.01 mW static 1 mW at 1 MHz
10	Immunity to external noise	nominal	fair	good	excellent	very good	very good	good	good	good	nominal	very good
11	Noise generation	medium	low medium	medium	medium	medium-high	high	low	low medium	medium	medium	low-medium
12	Propagation delay per gate, ns	12	27	30	90	12	6	4	2	1	300	70
13	Typical clock rate for flip-flops, MHz	8	2.5	12 to 30	4	15 to 30	30 to 60	60 to 120	200	400	2	5
14	Number of functions, family growth rate	high; growing	high; growing	fairly high, few functions in TTL	nominal; growing	very high; growing	very high; growing	very high; growing	high; growing	high; growing	low; growing	low; growing
15	Cost per function	low	low	low	medium	low	medium	low	medium	high	medium to high	medium to high

The advantage of logic family selection with respect to voltage-pulse-width is illustrated in Figure 7.8 [7.2]. The left-hand column shows a positive pulse input with Gate No. 1 on, and the right-hand column shows a negative pulse input with Gate No. 1 off. The upset energy in both cases is shown. The advantage of the HTL is apparent.

It should be noted that EMP hardening by component selection may decrease hardening to neutrons and gamma radiation.

7.4.2 Circuit Design Hardening

One problem that occurs with linear circuits is that an EMP signal can drive the circuit into a saturated nonlinear condition. This condition can last longer than the EMP signal, because of the storage time associated with the charge stored in semiconductor junctions and circuit capacitors. Figure 7.9 [7.2] illustrates the problem of saturation of a simple amplifier. The large positive and negative swings of the input signal will drive Q_1 into saturation or cut off, respectively. Part (b) shows the input impedance profile for these cases, and Parts (c) and (d) show the input equivalent circuits for both conditions. The charging time constant for Part (c) is less than that for Part (d); if the input is a sinusoid, a DC value will be stored in the capacitor as indicated in Part (e). After the transient is past, the circuit in Part (e) recovers, the amplifier does not perform correctly, and system degradation may occur during this time.

A simple remedy for this would be to put the back-to-back zener diode configuration of Figure 7.10 [7.2] across the amplifier input. Limiting for two different zener voltages V_{z1} and V_{z2} is indicated as well as the circuit outage times, Δt_1 amd Δt_2. respectively. These outage times would be less than that for the unprotected circuit of Figure 7.9 because the zener recovery is probably faster than the RC time constant of the equivalent circuit in Figure 7.9e.

Figure 7.11 [7.2] illustrates other techniques for preventing saturation. Part (a) shows a collector-base clamp. CR_1 is a Schottky barrier diode with low capacitance (therefore high frequency response) and with a forward drop less than the collector base voltage. Parts (b), (c), and (d) show zener clamping of gain, input and output respectively.

In addition to saturation, a circuit may "latch up" (power must be removed before the circuit can be restored) in response to an EMP transient signal. One example (Figure 7.12) is that of an open base transistor circuit; collector current is shown as a function of collector-emitter voltage. Normally, the operating point is at Point a, and I_C is small. A transient voltage greater than V_{CEO} can drive the operating point to Point b where the transistor is latched to this high current level [7.5].

Latch up can also occur for transistors grown in a semiconductor substrate, where the transistor is isolated from the substrate by a p-n junction. A transient could cause the transistor to latch into conduction like an npnp or SCR device. For this reason, dielectric isolation is preferred over junction isolation.

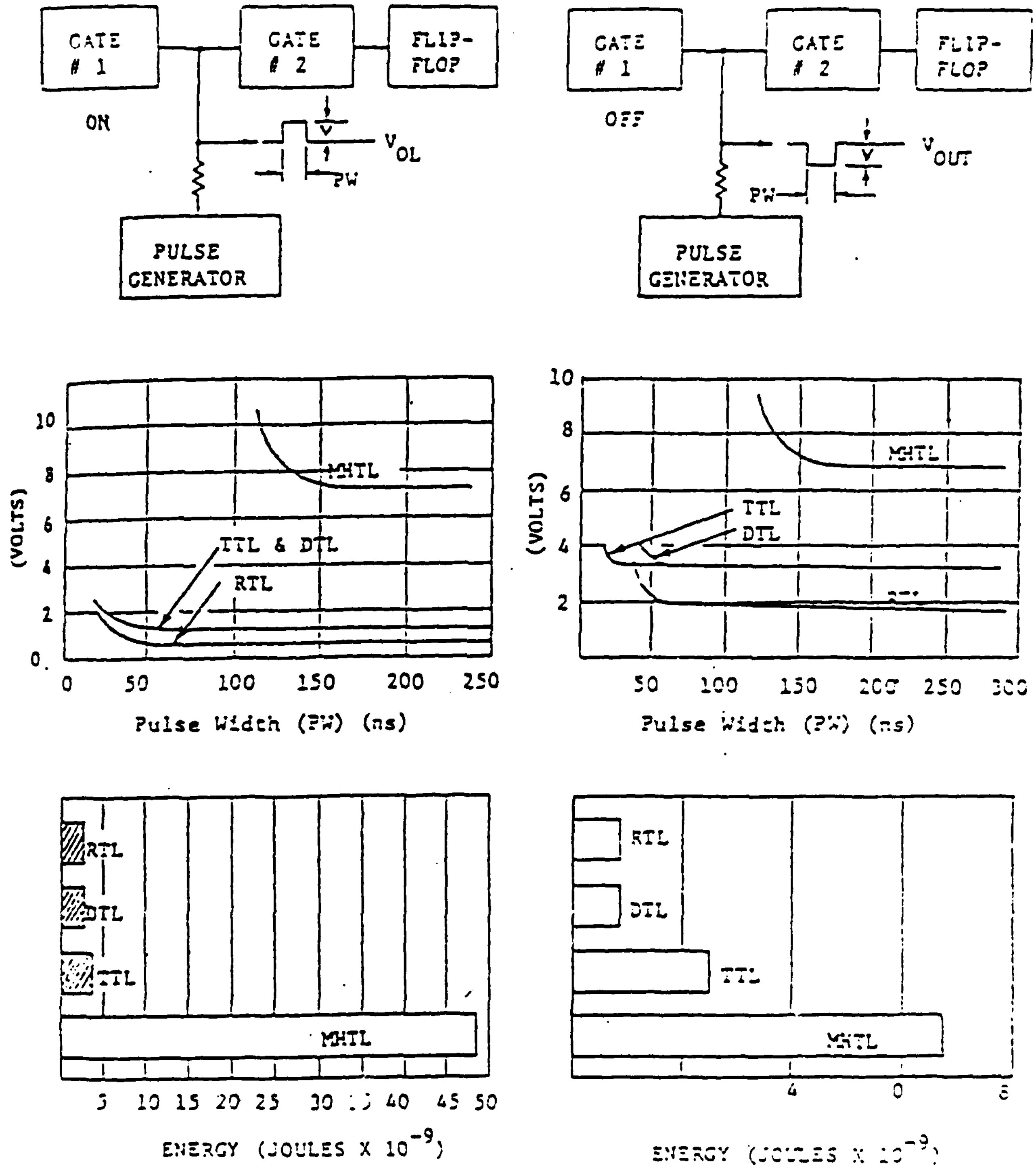


Figure 7.8 Comparison of Logic Family Upset Threshold [7.2]

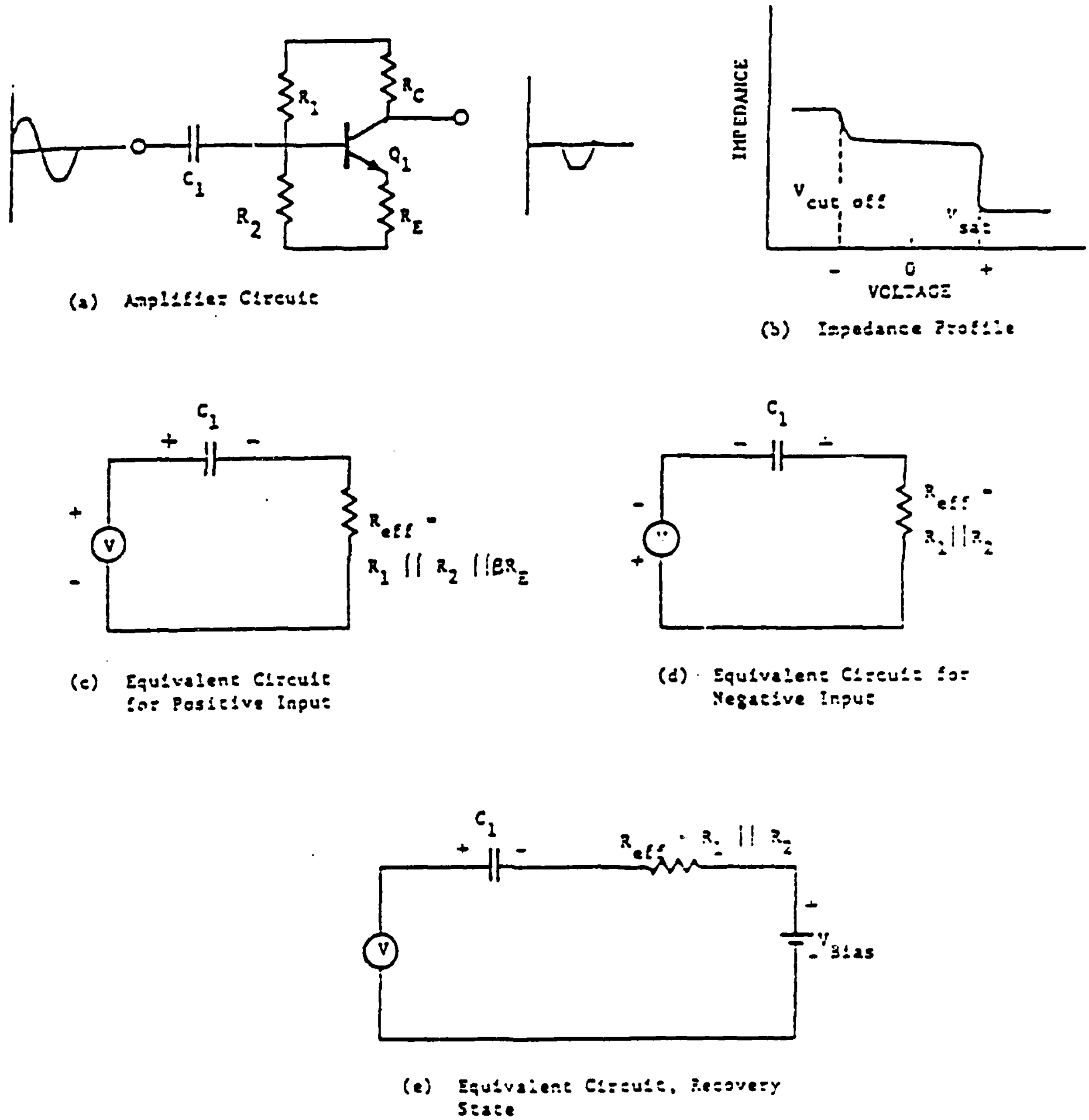


Figure 7.9 Example of Amplifier Saturation [7.2]

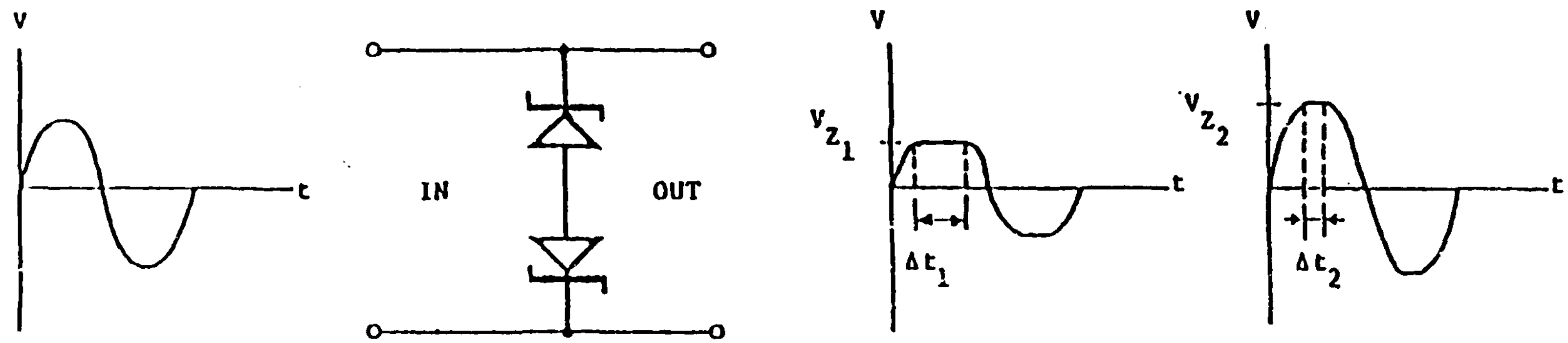
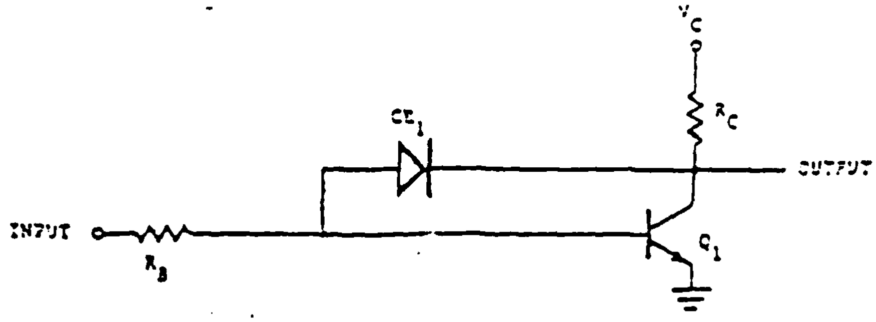
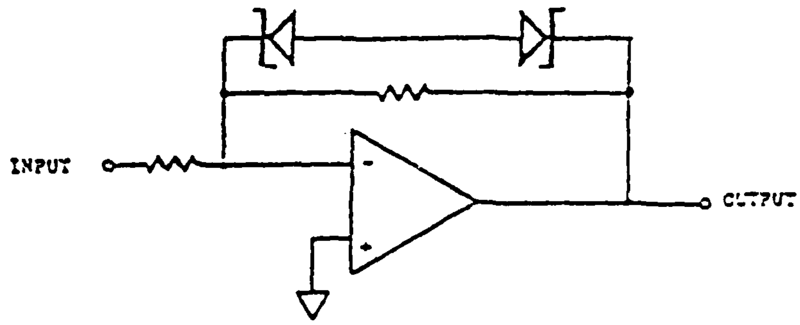


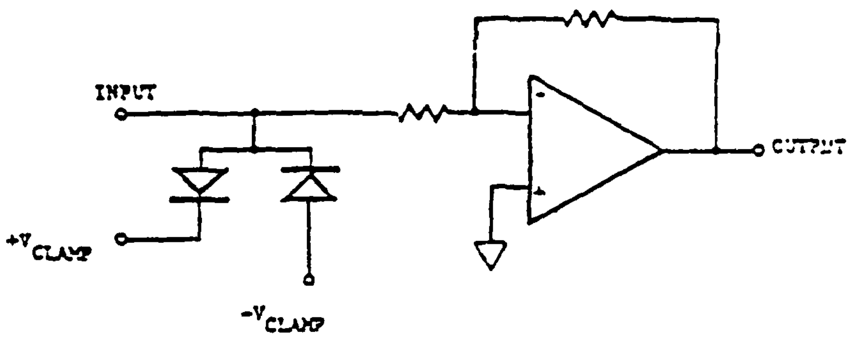
Figure 7.10 Bipolar Zener Diode Amplitude Limiting [7.2]



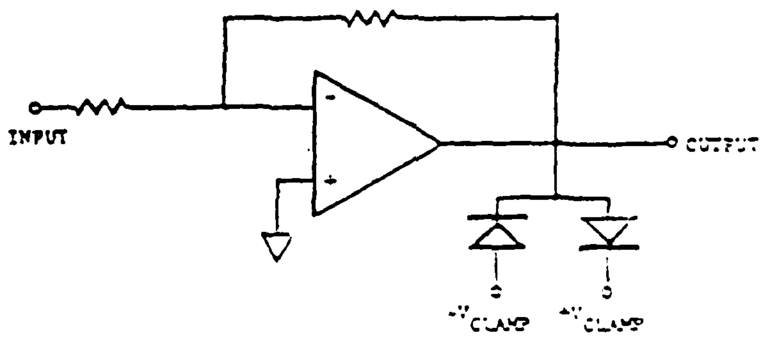
(a) Collector-Base Clamp



(b) Inverting Op-Amp Gain Limiting



(c) Op-Amp Input Clamping



(d) Op-Amp Output Clamping

Figure 7.11 Anti-Saturation Techniques [7.2]

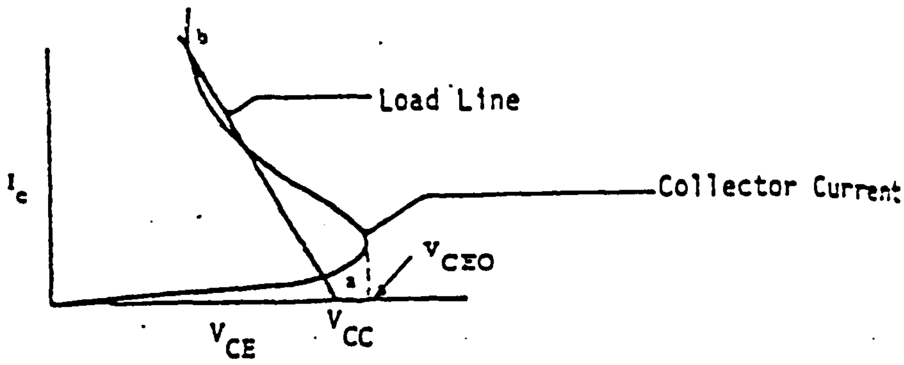


Figure 7.12 Latch Up Response [7.5]

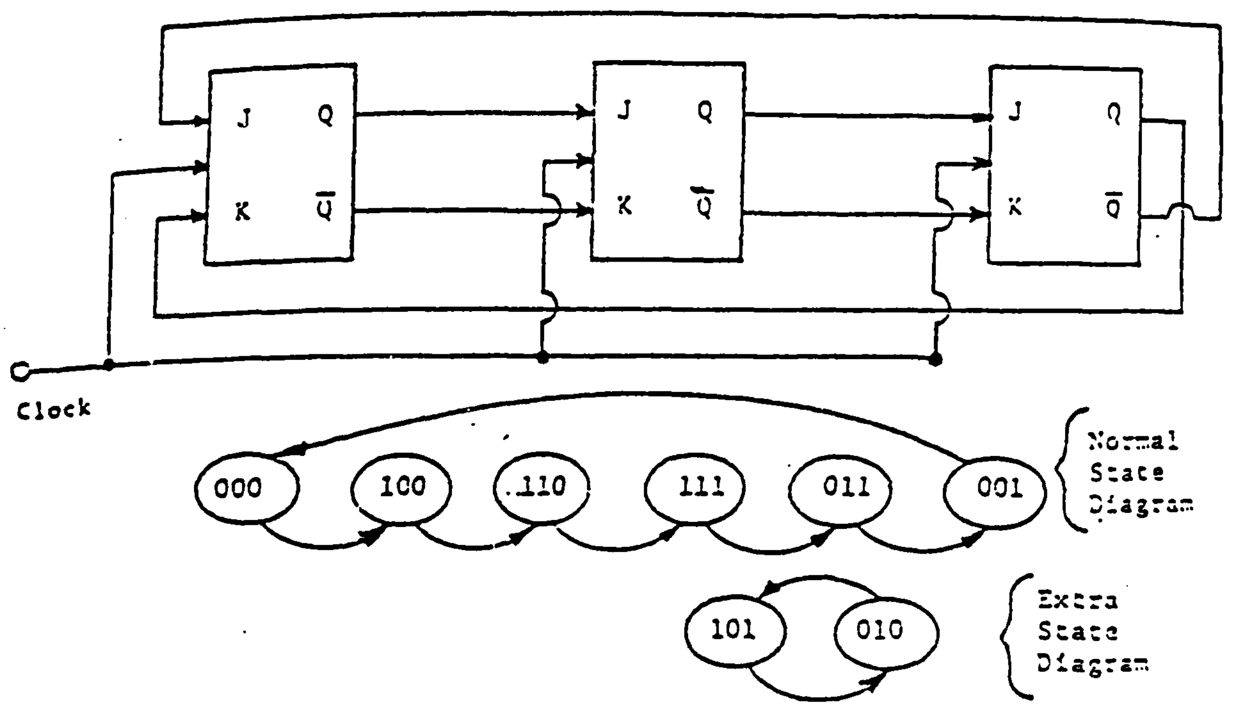


Figure 7.13 States of a Johnson Counter [7.2]

Digital counters may latch up in a trapping state. This is illustrated by the Johnson counter of Figure 7.13 [7.2]. The three binary circuits have eight possible states, but here only six are used, and the other two states normally never occur. This configuration provides a divide-by-six operation. A transient, however, could cause the counter to latch up into the extra states. Figure 7.14 [7.2] shows a modification which allows the counter to sequence into its normal operating mode. This problem can occur in any counter circuit in which some states are not used; therefore, these extra (trapping) states should be eliminated.

A pulse amplitude discriminator may be used to block the passage of EMP induced transients (Figure 7.15). When the input voltage is less than the reference voltage V_{ref}, the input pulse is transmitted to the output. If the input pulse is greater than V_{ref}, the comparator output changes sign and the input pulse is not transmitted to the output [7.2].

In a delay network for digital signals (Figure 7.16a), the input signal enables a pre-set counter decremented by a clock [7.3]. If the signal is present when the countdown is completed, the signal is passed to the output. This delay network is useful when the pulse width of the data signals is larger than the EMP transient pulse width. A variation on this is shown in Figure 7.16b, where information is allowed to transfer only during the presence of an information transfer enable signal, such as a clock. In this case, upset is not prevented, but the probability of upset is reduced.

7.4.3 Hybrid Hardening Techniques

Often one technique of hardening is not sufficient, and a combination of techniques must be used [7.2].

Consider the problem of a circuit that latches up or saturates as a result of an EMP transient. The frequency spectra of the signal and EMP are shown in Figure 7.17a. If amplitude limiting alone were used for hardening, the low frequency EMP components could still cause long subsystem interruption. But, if a high pass filter were also used to eliminate the low frequency EMP components, the outtage time would be reduced (Figure 7.17b).

Logic family selection and low pass filtering can be combined as shown in Figure 7.18. Part (a) shows the amplitude frequency spectrum of the various signals involved. Curve 1 is the EMP spectrum, Curve 2 is the EMP spectrum after low pass filtering, and Curve 3 is the data frequency spectrum. Part (b) shows the upset threshold for two logic families as a function of frequency. Without filtering, both logic families will be upset, because the EMP signal at point A has a value V_3 which is greater than the upset threshold for both families. The low pass filter puts the EMP peak value at point 3, and it is seen that logic family 1 will be upset, but logic family 2 will not.

7.5 System Level Upset Hardening

7.5.1 Error Criticality Reduction

Error criticality reduction does not prevent EMP induced errors, but it reduces their effects on system performance This reduction can be implemented by

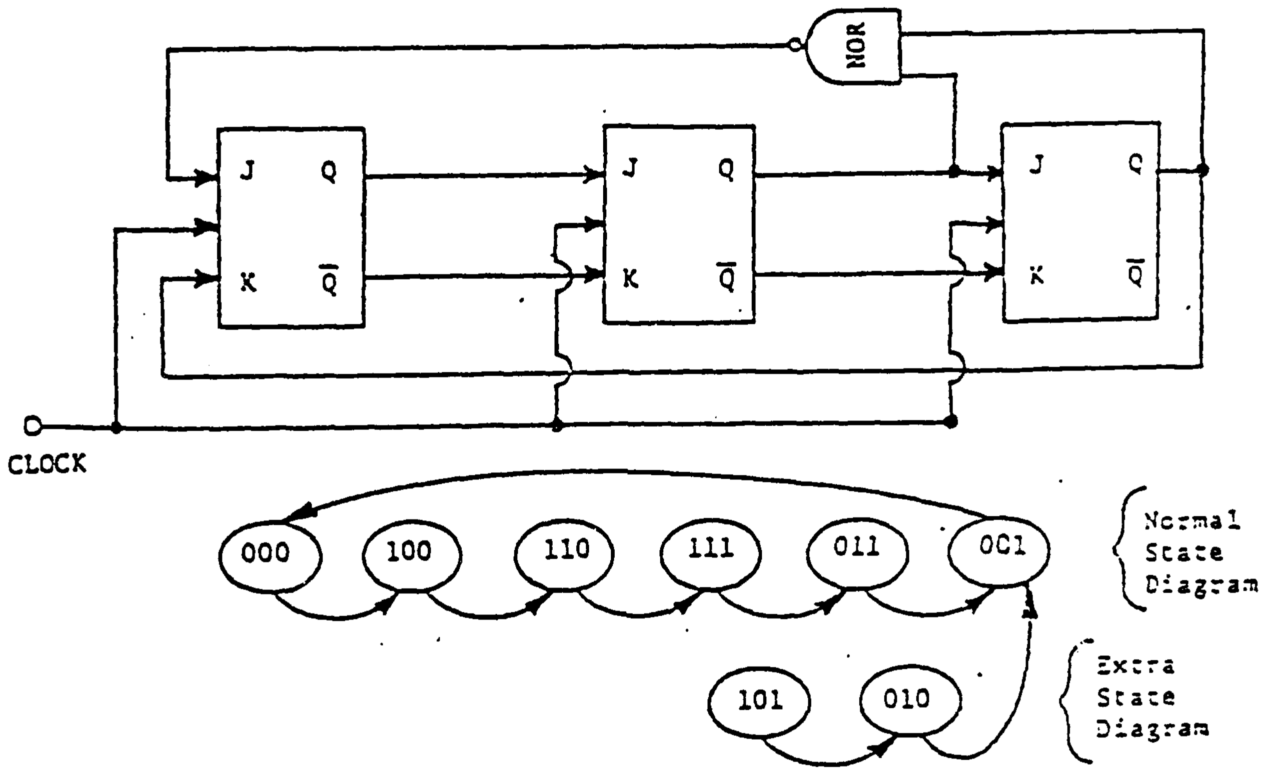


Figure 7.14 Modified Johnson Counter Eliminating Trapping States [7.2]

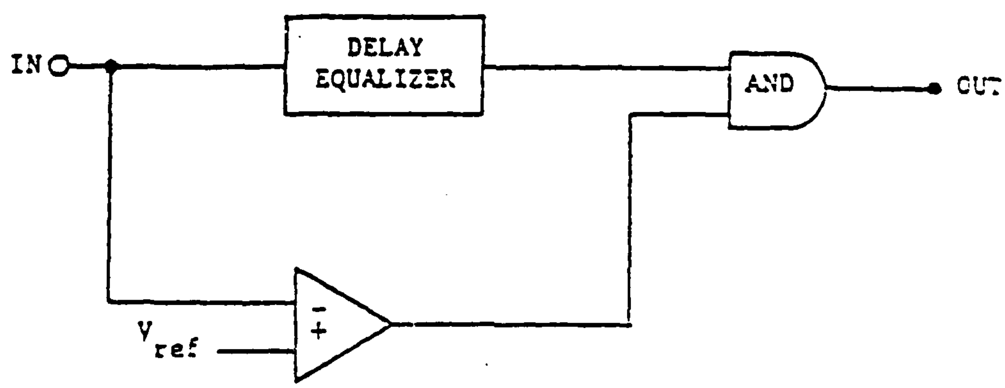
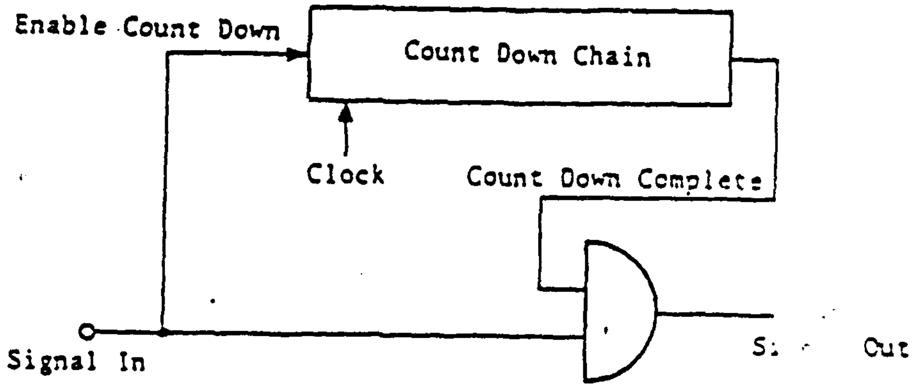
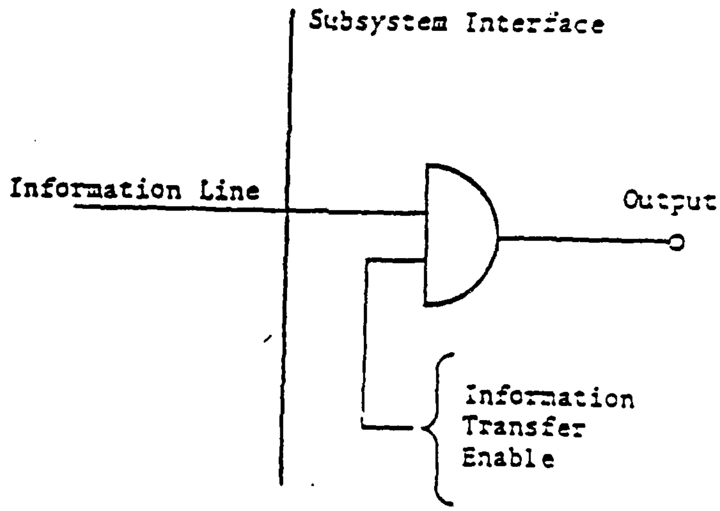


Figure 7.15 Digital Amplitude Discrimination [7.2]

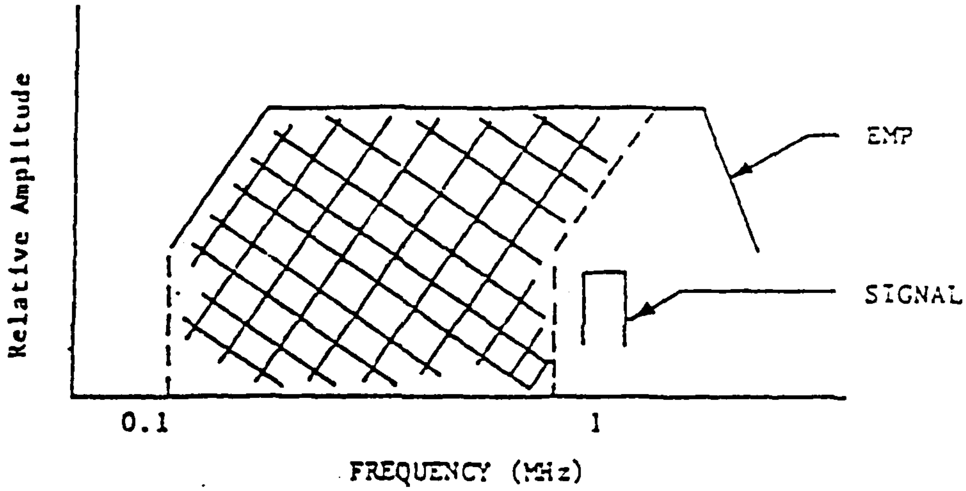


a. Digital Time Discrimination

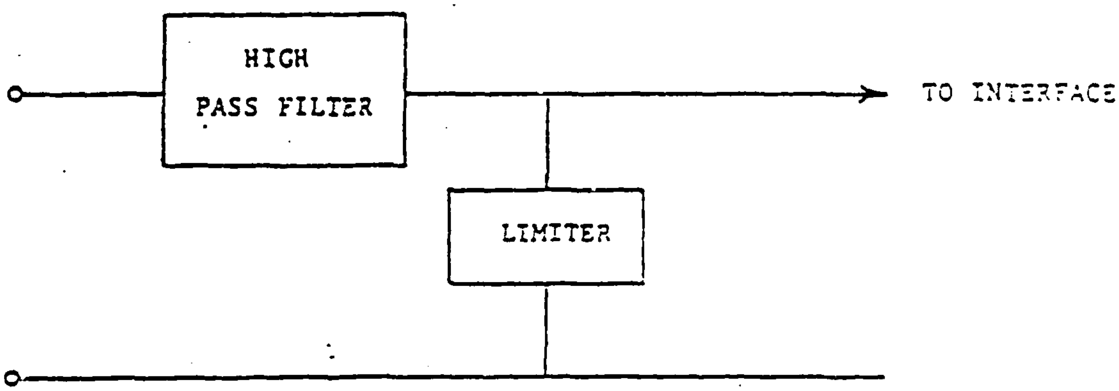


b. Information Transfer Enable Gating

Figure 7.16 EMP Time Discrimination Circuits [7.3]

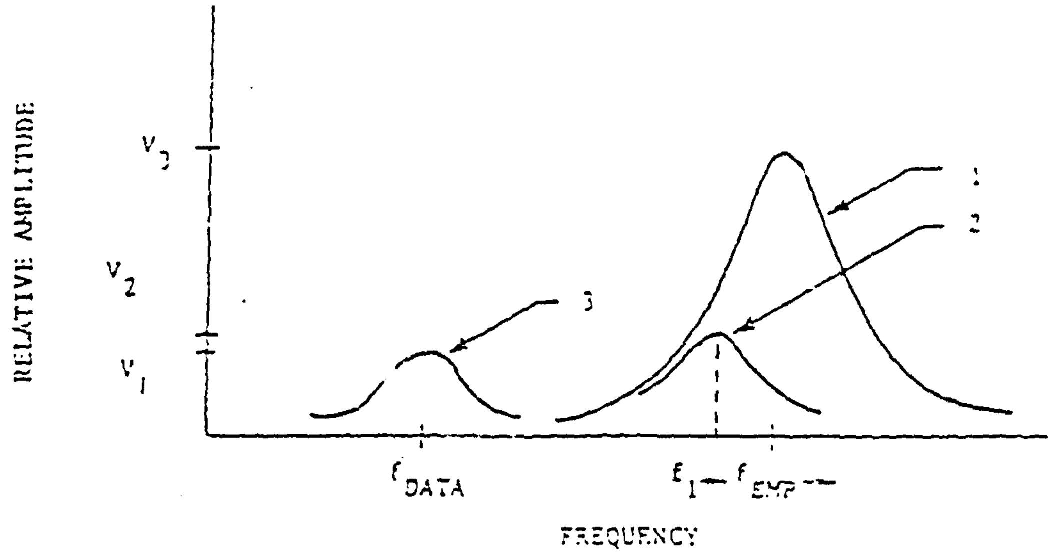


(a) Signal and EMP Characteristics

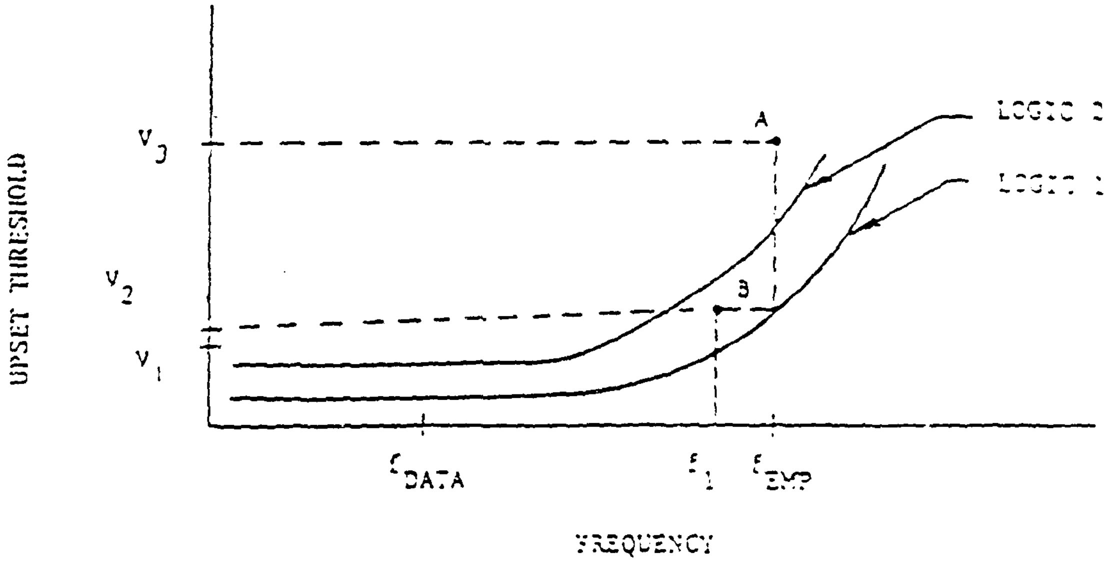


(b) Hybrid Upset Hardening Network

Figure 7.17 Upset Hardening Using Combined Filtering and Limiting [7.2]



(a) EMP/Data Frequency Spectra



(b) Logic Upset Level Comparison

Figure 7.18 Upset Hardening Using Combined Filtering and IC Selection [7.2]

changing the interface points within a system. For example consider two system design formats for a doppler radar distance indicator system (Figure 7.19).

In Format 1, the radar data are transmitted over a data line to the accumulator and display unit. EMP transients induced on the cables will feed into the accumulator and could cause a permanent error in the data display. In Format 2, the accumulator is located in the same elctronics box as the radar, and data are periodically transmitted to a register located near the display. EMP transients will still appear on the data lines and cause an error in the register. However, in that the register is periodically updated by the accumulator, the error in the register is erased after a very short time. In this case, the EMP transient is of little consequence[7.2].

Upset duration in digital systems can be reduced by use of a master reset or synchronization signal. If sequencing operations are synchronized only at the beginning of an operation, permanent upset could occur, but if operations are periodically synchronized or reset, the upset duration is temporary.

7.5.2 Parameter Constraint Technique

In this technique, advantage is taken of the physical constraints on the variables monitored. Consider the case of tracking aircraft through the use of radar. In this case, an airplane has a maximum speed and acceleration and there are realistic limits on the distance traveled by the aircraft during a fixed time. However, the data obtained by the monitor (Figure 7.19) could be distorted as a result of EMP; the monitor could then indicate that the airplane had traveled 100 miles in one digital time frame or that the distance traveled in that time frame was negative. This error can be sensed electronically, and an appropriate system response to the error can be made.

7.5.3 Digital Coding Hardening

Special digital coding techniques can be used to harden systems. For example, a sequential system can be designed so that a particular sequence of pulses, instead of a single pulse, is necessary for a state change. An example logic network is shown in Figure 7.20 [7.5]. The sequence necessary to get an output pulse Z is that X_1 must occur first, followed by X_2, followed by X_3. The J-K flip-flop* reset states are logical zero. If the pulse sequence X_1, X_2, X_3 were produced by well-shielded circuitry, the chances of the sequence occurring as the result of EMP-induced transients is small. The flip-flop network of Figure 7.20 and its output must also be well shielded, but the transients on lines carrying X_1 and X_2 annot be interpreted as control pulses; therefore, these lines can extend over long distances without shielding. This technique is difficult to apply for general system protection but might be useful for some special circuits.

Error detecting and correcting coding techniques are discussed in Reference 7.2.

*J-K flip-flops operate so that a pulse at the J input causes the flip-flop to "set" to one; a pulse at the K input causes the flip-flop to "reset" to zero; and simultaneous pulses at both inputs cause the flip-flop to "trigger" (change state).

FORMAT 1. THE DOPPLER RADAR GENERATES ONE PULSE FOR EVERY 0.1 MILE TRAVELED. THESE PULSES ARE TRANSFERRED OVER THE DATA LINE TO AN ACCUMULATOR IN THE DISPLAY UNIT WHICH UPDATES A TOTAL DISTANCE COUNT.

FORMAT 2. THE TOTAL DISTANCE ACCUMULATOR IS IN THE DOPPLER RADAR UNIT. THE ACCUMULATOR CONTENTS ARE TRANSFERRED IN SERIAL FORMAT TO A REGISTER IN THE SOLID STATE DISPLAY.

Figure 7.19 Example Problem in Functional Layout Based pm Susceptibility [7.2]

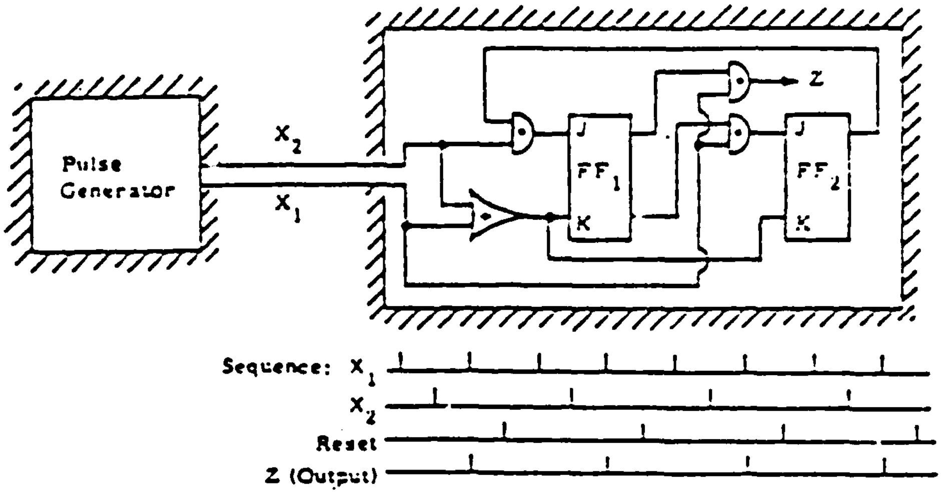


Figure 7.20 Functional Hardening Example [7.6]

7.5.4 Circumvention

Circumvention involves sensing an EMP event and initiating some preplanned system response. The system would respond by rejecting all data being sent during the EMP event and then either requesting immediate retransmission, recycling stored pre-event data, or simply waiting for a new set of data.

Requesting an immediate retransmission involves a return link to the data originating system and a memory in that data system. The data receiver must have the capability to receive delayed data. This added complexity increases system costs and weight and decreases reliability.

Circumvention requires that the EMP event be detected. A separate external antenna or a current probe can be used to detect cable currents in electronic packages. Either method presents the problem of determining the initiation level. If this level is set too low, inconsequential EMP events or electromagnetic interference may initiate circumvention.

Another form of circumvention that applies to manned equipment is visual indication of an EMP event; in this case, the operator could manually reset or recycle the systems involved.

One advantage of circumvention is that it may already be included in the nuclear radiation hardening design of a system and with some modification could be used for EMP hardening.

7.6 Automatic Data Processing (ADP) Selection Criteria

7.6.1 Background

The effects of EMP on ADP components is of particular concern [7.6] because of the inherent susceptibility resulting from its speed, discrete signal nature, logic levels, and component parts. A particular very serious vulnerability problem for digital circuits in computer components is the potential disruption of logic states and the distortion of digital signals. For the vast majority of systems it is not realistic to shield or otherwise protect the system components from transients that will be disruptive. The result is that measures often must be taken to permit the system to tolerate upsets such that overall performance is not adversely affected. The toleration requirement can sometimes be met at the component level. More often than not, it has to be incorporated through software at the system level. Selection of ADP components more than any other major generic component class must take into account the system operational requirements, capabilities, software limitations, and hardware compatibilities.

ADP upset toleration can be achieved through:
(See Table 7.3 for definitions)

- hardware and software redundancy
- error detection/correction
- process redundancy
- plausibility checks
- traps
- timers
- checkpoint-rollback

Each of these techniques have been implemented in ADP systems in dozens of variations and combinations.

In the selection of ADP systems the following items are extremely important.

7.6.2 Magnetic Tapes and Disks

Magnetic tapes and disks, when in a passive state, can be considered hard. Any possible upset or damage to such storage devices is limited to that caused by the equipment which accesses those storage media (i.e., tape drives and disk drives). Further tapes and disks are not normally subject to damage and upset even when mounted on drives unless read and write operations are in progress when the drives experience the effects of EMP upset.

7.6.3 Memory Selection Criteria

Computer memory should be selected with the consideration that transients could appear on some or all hardware inputs at the same time and that power may be lost for generally a short but indeterminate time. Therefore:

Volatile memory should be avoided.

High threshold memory should be sought.

Table 7.3 Definitions for ADP Equipment [7.6]

Checkpoint	A process whereby critical information is recorded on a backup or redundant storage medium for use in a rollback or restart operation in the event the primary information is lost or damaged
Checkpoint rollback (CPRB)	A fault tolerance technique used to protect against the effects of upset. A process whereby (1) critical information is preiodically and routinely recorded on a backup or redundant storage medium and (2) when an upset fault is detected, any lost or damaged information is restored from the checkpointed copy and a restart is performed.
Hardware redundancy	Hardware redundancy involves the use of redundant components, circuits or sub-systems (including computer peripherals) to protect against faults. Redundancy can be provided to perform identical functions for comparison to detect errors or it may be provided as a means of backup in the event an active unit fails.
Plausibility checks	Plausibility checks are usually software or possibly human checks which verify that information, being processed or which is the result of computations, fall within realistic bounds. Plausibility checks are useful for detection of errors caused by upset.
Process redundancy	Process redundancy involves the multiple execution of a process and comparison of the results. Process redundancy is useful for fault detection.
Rollback	A process whereby, upon detecting a fault, critical information is restored form a previous checkpoint and the process or system is restarted at the point of that checkpoint.
Software	In general: a set of programs, procedures, and possibly associated documentation concerned with the operation of a data processing system. For example, compilers, library routines, manuals, circuit diagrams. Software as used in this document does not include procedures and documentation. Contrast with hardware.
Trap	A trap is a conditional jump to a known location, automatically activated by hardware, with the location from which the jump occurred recorded. Traps are useful for fault detection.
Time-out error	Time-out is the time interval allotted for certain operations to occur; for example, response to polling, addressing or performance of I/O. A time-out error occurs if the task takes more time than has been allotted.
Timer	A timer is a hardware of software mechanism which monitors on-going tasks to assure that the normal time required for the task is not exceeded.

Inherent error checking is desirable in read-write cycle.

Transient surge protection in terms of clamping and limiting devices is desirable.

High impedance inputs and outputs (provided surge protection is provided) are desirable. Series resistance (carbon composition resistors) of at least 100 ohms is desirable on the input and output lines.

Internal voltage regulation is desirable. At the minimum, a 10uF capacitor with a .01uF parallel ceramic capacitor should be placed between the DC input and ground.

Memories should be housed in good EMI/RFI enclosures.

Maximum use of ferrite beads and feed-through capacitors is desirable.

MOS devices employed in the memory must have internal bipolar protection.

The system must be able to recover from a massive upset without affecting its restoral capability.

Restoral must be accomplished within the mission (or operational) requirements.

Redundancy in processing and hardware are particularly desirable.

All critical software and data must be backed up.

Back-up storage for restoral should be on off-line magnetic disk or tape. Sequential memory is preferred over random memory for critical restoral software and data.

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7.2 EMP Upset Hardening Guidelines, The Boeing Company, Contract No. F29601-72-C-0028, December 1972.

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CHAPTER 8

COMMON MODE REJECTION (CMR) TECHNIQUES AND OPTICAL ISOLATION

8.0 Executive Summary

EMP induced transients are generally coupled to cables in the common mode. Chapter 8 discusses general techniques for reducing these transients. This is generally accomplished by using special circuits which allow only the differential mode signal to couple to electronics and to reject the common mode signal. Also discussed in this chapter are the advances in using fiber optics as optical isolators between equipment.

8.1 Background

Common mode rejection (CMR) techniques and optical isolation provide alternative or additional means of decoupling EMP transients from sensitive electronic circuits. As in other decoupling techniques, the attenuation provided by CMR is most often achieved at the expense of bandwidth, weight, additional circuit complexity, or cost. The most common decoupling techniques involve use of transformers and balanced circuits, or optical isolators and fiber optics, although it may be expected that the order will be reversed with new advances and experience with optics engineering technology.

The use of transformers and balanced circuits for attenuation of EMP transients at some or all subsystem interfaces can be thought of as a subset of a generic differential signaling technique [8.1]. This balanced signal approach is useful for EMP environments because EMP transients are usually induced on cables in the common mode, and a balanced configuration using two signal lines allows the propagation of information in the differential mode. The desired signal may now require additional interface circuitry to reject the common mode and convert the balanced signal to an unbalanced signal. Note that both balanced cabling and balanced interface circuitry are required to achieve the desired result. A hardness improvement of about 20 dB between 1 and 10 MHz can be expected for a design configuration incorporating balanced differential signaling, as opposed to a similar unbalanced configuration. Up to 60 dB may be possible at lower frequencies; common mode rejection is most efficient at low frequencies where stray capacitance and inductive imbalance can be neglected.

Optical systems as a means of decoupling EMP transients from sensitive circuits have some inherent advantages in EMP hardening, namely, their immunity to electromagnetic pulse phenomena. At one time their practicality was dubious, but the pace of present technology is making optical communications systems attractive due not only to distinctly military advantages, but also lower system cost, increased bandwidths, and higher data rates. Improved excitation, detection, and transmission systems have further enhanced the applicability of optical systems used in communications. Possible additional benefits, besides greater EMP hardening and other aspects noted above, are higher reliability, lower maintenance and life-cycle costs, and longer mean time between failures. These latter benefits have been indicated by studies, but as yet have not been adequately demonstrated.

Section 8.2 discusses the use of transformers and balanced circuits for rejecting the common mode signal. Section 8.3 discusses optical isolation techniques. Section 8.4 discusses the use of fiber optics. Section 8.5 gives examples of CMR techniques at the non-antenna interface.

8.2 Transformers and Balanced Circuits

Isolation transformers for decoupling induced EMP transients from electronic circuitry must be placed as close as possible to the cable entry to the circuitry [8.2]. The hardened design procedures involve center-tapping the signal/control line side of the transformer to ground with a ground lead as short as possible, and in any case no longer than 2 inches.

The side of the transformer connecting to the sensitive electronics should have a differential suppression device.

The use of a transformer to allow a differential mode signal to pass is shown in Figure 8.1 [8.3]. Balancing the transformer about its center taps enables common mode signals, such as those from EMP transients, to be rejected. A transformer can also be used to convert a balanced line to an unbalanced line or vice versa. To achieve the function, the transformer is connected at the input and output terminals of the signal lines, as shown in Figure 8.2.

Although transformers are used incidently in some hybrids, none are specifically for protective purposes [8.4]. Transformers are readily available and when properly applied, can be among the most effective of the EMP isolators. They can block common-mode noise, withstand moderate voltages and, given the proper core material, limit and dissipate. They also can be tuned and electrostatically isolated.

Design considerations to be aware of are [8.4]:

a. Avoid narrow hysteresis-loop, quick saturation cores which might generate transients of their own.

b. Use the natural dissipation characteristics of the available cores by selecting laminations as thick as feasible. Some loss even might be permitted at the operating frequency.

c. Use a metal-type rather than a foil-type electrostatic shield.

d. Specify a transient insulation breakdown test rather than the standard DC and 60 Hz tests.

e. If critical, provide a means of balance adjustment.

A balanced circuit such as a differential amplifier can also be used to provide CMR. Common mode signals are rejected by the circuit design shown in Figure 8.3. Figure 8.4 shows the conversion of an unbalanced line to a balanced line.

It should be noted that differential amplifiers have an advantage over transformers in low frequency characteristics, but they also have high input impedances, are susceptible to oscillation at high frequencies, and may be damaged or fail when exposed to large common mode overvoltages. On the other hand, transformers cannot pass DC signals and insertion loss can attenuate the signal. In addition, transformers may also require protection against burnout and coil to coil arcing.

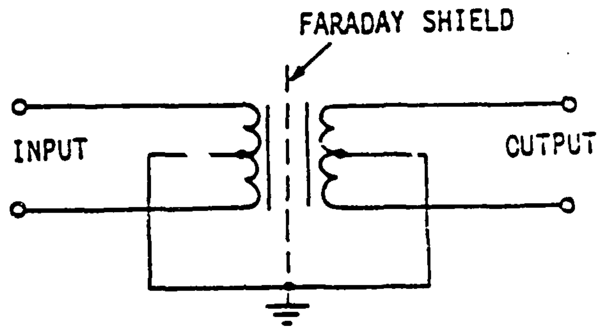


Figure 8.1 Differential Transformer

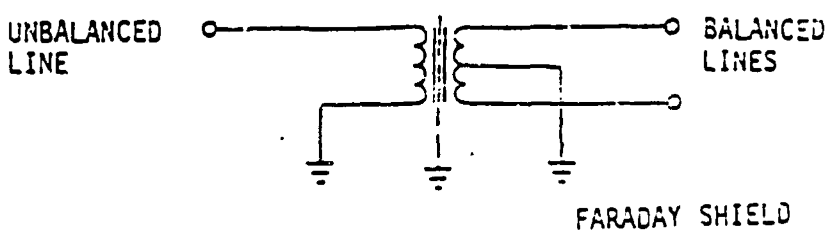


Figure 8.2 Balancing Transformer

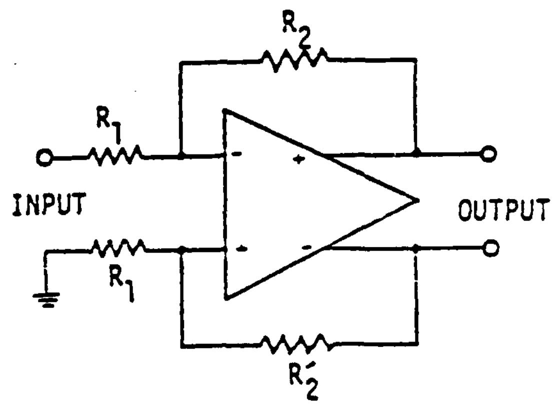


Figure 8.3 Conversion of Unbalanced to Balanced Lines

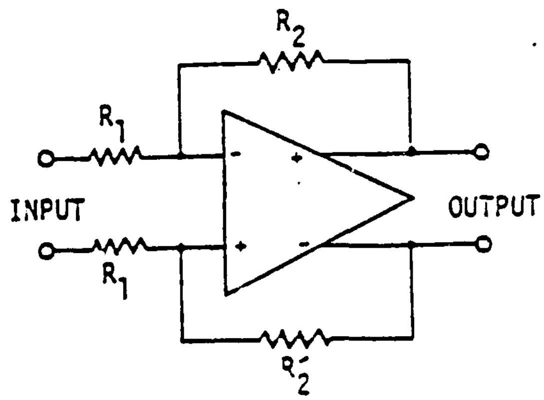


Figure 8.4 Differential Amplifier External Connections

Another balanced circuit is a differential scheme employing two phased logic in which the differential amplifier is replaced with a differential voltage level detector (Figure 8.5). In this case, the output changes state with a differential change in the input.

8.3 Optical Isolators

The decision to use optical isolators and fiber optics can be expected to be the result of a selection process involving a long and complex iterative

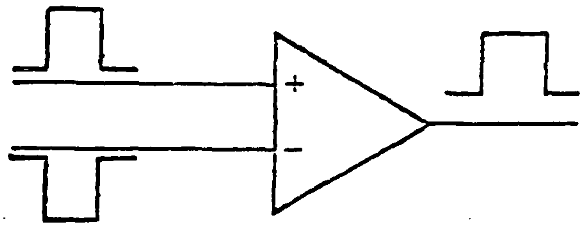


Figure 8.5 Level Detector as Logic Interface

procedure. Tradeoffs have to be made between optimum electro-optical performance parameters and realistic design and cost constraints. The iterative design procedure can be aided by a link power gain or loss budget, which quantifies by table of formula the optical gain (or loss) at the electro-optical component interface points, along with the systems requirements [8.5]. The conclusion of this process is a quantified design margin which can be compared or evaluated with respect to the system performance specifications.

The electronics industry is developing integrated and hybrid circuits specifically designed for driving solid-state light sources to be used in fiber optic systems. Most of these circuits are intended for digital applications. The designer using optical isolators should pay special attention to the driver circuitry. Presumably he will want to use other CMR techniques coupled with the driver circuitry to ensure that these devices are not vulnerable.

The types of semiconductor light sources most likely to be used by the military services in fiber optic communication systems are light-emitting diodes (LED) and laser diodes. Both of these can be fabricated from several different semiconductor materials to yield somewhat different properties, primarily different emission wavelengths. The operating wavelengths are chosen to be compatible with fiber transmission properties and range from 0.6 to approximately 1.3 μm.

Lasers have always been preferred for long distance over LEDs because of their narrower spectral width, larger modulation bandwidth, and greater launch power into multimode fibers. LEDs offer the advantages of stability and longevity within the required modulation bandwidths up to 170 MHz. A lightwave communication system has been demonstrated by Bell Laboratories that uses LEDs to produce light at 1.3 μm.

8.4 Fiber Optics

Optical fibers are immune to electromagnetic pickup and therefore do not produce electrical pulses capable of causing damage to other components.

With the development of the laser in the early 1960's came the promise that the immense information carrying capacity of optical radiation would be forthcoming. It was out of the need for a reliable low loss transmission media that research on optical fibers proceeded. In 1970 Corning demonstrated an optical fiber with a 20 dB/km attenuation [8.6].

Because these losses were comparable to the losses suffered in the coaxial cable transmission lines the outlook for the fiber optic system greatly improved. Since then, higher quality fibers have been developed, so that now laboratory samples of graded index multimode fibers are produced with attenuations as low as 1 dB/km while commercial cables have been assembled and used with attenuations of less than 5 dB/km [8.7].

The advances in light transmitters and receivers have been equally impressive. For analog intensity modulation or short distance digital communications, LEDs are the preferred source. The newer devices have a nearly linear relationship between light output and current input and a long lifetime (10^5 hours).

For digital communications over long distances the injection lasers tend to be the preferred source because about 15 dB more optical power can be coupled into a fiber than could be achieved with a LED. The spectral width of their optical output is about an order of magnitude narrower than of a LED so that pulse dispersion in the fiber is less of a problem.

PIN diode or avalanche photodiodes (APDs) are the receivers used in most systems; PIN diodes are cheaper and take lower bias voltage than APDs (15-100 volts compared to 400-800 volts). However, APDs are about 20 times more sensitive, and so the APDs are often used in long-run, high data rate systems.

Modern military forces make extensive use of radar systems, electronic controls, computer data analysis, ballistic missiles, radio controlled missiles, as well as local and long distance communications systems. In each type of system we can expect to see increasing use of fiber optics communication links.

In addition to the potential advantage of lower system cost and higher data rates that make fiber optics desirable in general, there are a number of distinctly military advantages [8.9].

1) Fiber optic cables are immune to radio frequency interference that is often important when a number of electronic systems are used in close proximity.
2) Fiber optic links are immune to electromagnetic countermeasures.
3) Fiber optic links are immune to electromagnetic pule phenomena.
4) Fiber optic links cannot be tapped like normal phone lines and field wire cables. This allows secure communication without encoding.
5) Fiber optic cables are smaller and weigh less than wire cables, thereby reducing transportation costs and logistic problems.

If one contemplates using fiber optic intra-rack communications of low-level possible applications would include

1) Replacement for cables in intra-rack communications of low-level digital or analog signals.
2) Replacement of communication cables between electronic systems in an unshielded or poorly shielded structure, i.e., terminals/computer. crypto/transmitter, etc.

3) Replacement for wire in a phone system.

4) Replacement for coaxial cables/repeaters in a long haul telephone system.

There are several reasons that one would choose not to use fiber optics in these systems, among the most significant are the costs of retrofitting existing equipment, and the possibly poor reliability of newly designed fiber optic circuits. Experience with new fiber optic data links shows that there are serious problems with the reliability of fiber optic cable connections when assembled by poorly trained and inexperienced personnel. Because military systems may be assembled under similar adverse conditions, these problems can be expected, at least initially, in all new applications. Consequently, the designer of military equipment must weigh the benefits derived from using fiber optics against the possible cost increases and reliability problems that may occur.

Numerous fiber cables have surfaced that exhibit different parameters. Generic fiber designs include glass/glass, plastic clad silica and all plastic. Relative merits are compared in Table 8.1 [8.10]. A primary distinguishing feature between the fibers is their performance over temperatures, moisture, and other environmental conditions. Glass fibers fare better in harsh factory atmospheres - presumably also in shipboard environments. Because the fiber optic technology is relatively new, it is appropriate to review the benefits resulting from the use of this technology with regard to practical questions of cost, weight, and reliability, as well as other technical concerns. The following information is drawn directly from References 8.11 and 8.12.

Table 8.1 Comparison of Parameters Between Glass and Plastic Fibers [8.10]

	Fiber Diameter		Optical Parameters		
Fiber Type	Core, μm	Clad, μm	Numerical Aperture at 90 Percent Power	3dB Bandwidth, MHz·km	Attenuation at 850 nm, dB/km
All plastic	1000	1030	0.45	≥5	≤600 at 660 μm
	370	400			
Plastic clad silica	200	300-600	0.2-0.3	≥10	≤30
Glass/glass	200	230-280	0.3	≥10	≤15
	100	140	0.3	20-200	≤10

Common Mode Rejection Ratio

$$CMRR = 20 \log Vem/V_D$$

where

Vem = common mode input voltage

V_D = equivalent differential mode input required to produce the same output resulting from Vem.

CMRR range is 10 dB to 36 dB. The values from 10 dB to 30 dB are based totally on manufacturer's specifications. The added 6 dB is an estimate of the amount of increased CMRR which may be obtained through special installation techniques. Until experimental data exists to support this range evaluation for an EMP environment, optical isolators should be considered to have questionable credibility rating.

Electromagnetic Compatibility

A properly jacketed optical cable will neither emit nor pick up electromagnetic radiation, insuring security of communication and immunity from interference and crosstalk to a degree not possible with electrical cables. Suitably designed fiber optic interfaces have been proven to be immune to all forms of electromagnetic compatibility problems - crosstalk, short circuit loading, EMI, RFI, ground loops, ground isolation, ringing and echoes.

Weight and Size

The fiber optic transmission line is much smaller and lighter than an electrical line of equivalent bandwidth. When electrical lines must meet EMP-immunity requirements, the weight and size reduction advantages of fiber optic lines are increased.

Bandwidth and Improved Multiplexing Capacity

The wide bandwidth capacity of fiber optics can far surpass the 1 MHz limit of twisted-shielded-pair wire and the 20 MHz data rate limit of coaxial cable. This feature offers excellent multiplexing bandwidth possibilities; light sources already have demonstrated a 300 MHz capability.

Cost

Life cycle costs of fiber optics systems promise to be markedly less than those of electrical systems. After development, tooling, and preproduction, it is expected that fiber optics lines can be produced in comparable volume at a fraction of the recurring cost of producing electrical lines. Furthermore, when the multiplexing capability of fiber optics is fully realized, fewer lines will be required, resulting in an order of magnitude reduction in the procurement cost of interface components.

Logistics support costs will be less, due not only to fewer supply/support items and requirements, but also to reduced maintenance and increased longevity as compared with electrical systems.

Reliability and Maintainability

The great multiplexing capability of fiber optics will reduce the quantity and complexity of interfaces to correspondingly enhance system reliability and maintainability. The single optical junction of fiber optic line with source, detector should be an external reliable interface that does not require electrical or mechanical contacts. Fewer, more reliable, and less complex components of the fiber optics system mean less troubleshooting and preventive corrective maintenance along with simplified maintenance support.

Safety

Cutting or breakage of fiber optic lines during transmission does not produce sparks or other hazards. This offers safety advantages for fiber optic systems located in areas which contain fuel, ammunition, oxygen, etc., as well as during catastrophic situations to which a military platform may be subjected.

Cost Burden

As shown in Figure 8.6, the cost of metals for wiring is rising while the cost of fiber optics is declining. Although present fiber optic bundles and cables are more expensive than equivalent size metal wire, the difference is diminishing due to the availability of materials and will diminish more rapidly as fiber production increases.

For equivalent channel capacity, however, optical fibers are now less expensive than wire [8.16]:

(a) A study conducted by the NELC, San Diego, California, compared the cost of a fiber optic system for the A-7 aircraft (ALOFT) against a coax cable system. As shown in Tables 8.2 and 8.3, the cost of the fiber optic system is slightly higher. However, as technology and production continue, the cost of fiber optics is expected to fall.

(b) Other factors to be considered in the cost burden are operational support and maintainability/reliability. Fiber optics promise greater maintainability/reliability than similar coax cables. There are fewer electrical/mechanical connections and multiplexing will reduce the quantity and complexity of interfaces.

(c) EMP/EMI immunity is another factor which affects cost burden. A coax cable with enough shielding to provide the same amount of EMP/EMI immunity would be extremely expensive and heavy [8.13].

Flight Worthiness

There are few problems related to the use of fiber optics in avionic systems. Shock, vibration, temperature, humidity, and altitude have no effect on fiber optic systems, although the LEDs used are slightly temperature dependent. Twists, turns, bends, etc., are no real problem. A fiber optic system is safe in a hazardous area due to the fact that there is no electrical transmission in the cable.

A multiplexed fiber optic system would be lighter than a similar coax system, as well as having less volume.

Summary

Signal attenuation as low as 1 dB/km (low loss) has been produced although medium loss (200 to 500 dB/km) cables are suitable for avionic systems. Data rates of 3×10^{10} bits/s over 1 km length of cable have been obtained. By use of a semiconductor laser source, data rates up to gigabits/s may be realized [8.14]. Fiber optic cable is generally lighter and smaller than coax cable. A comparison [8.15] showed fiber optic cables around 8 lbs/1000 feet and

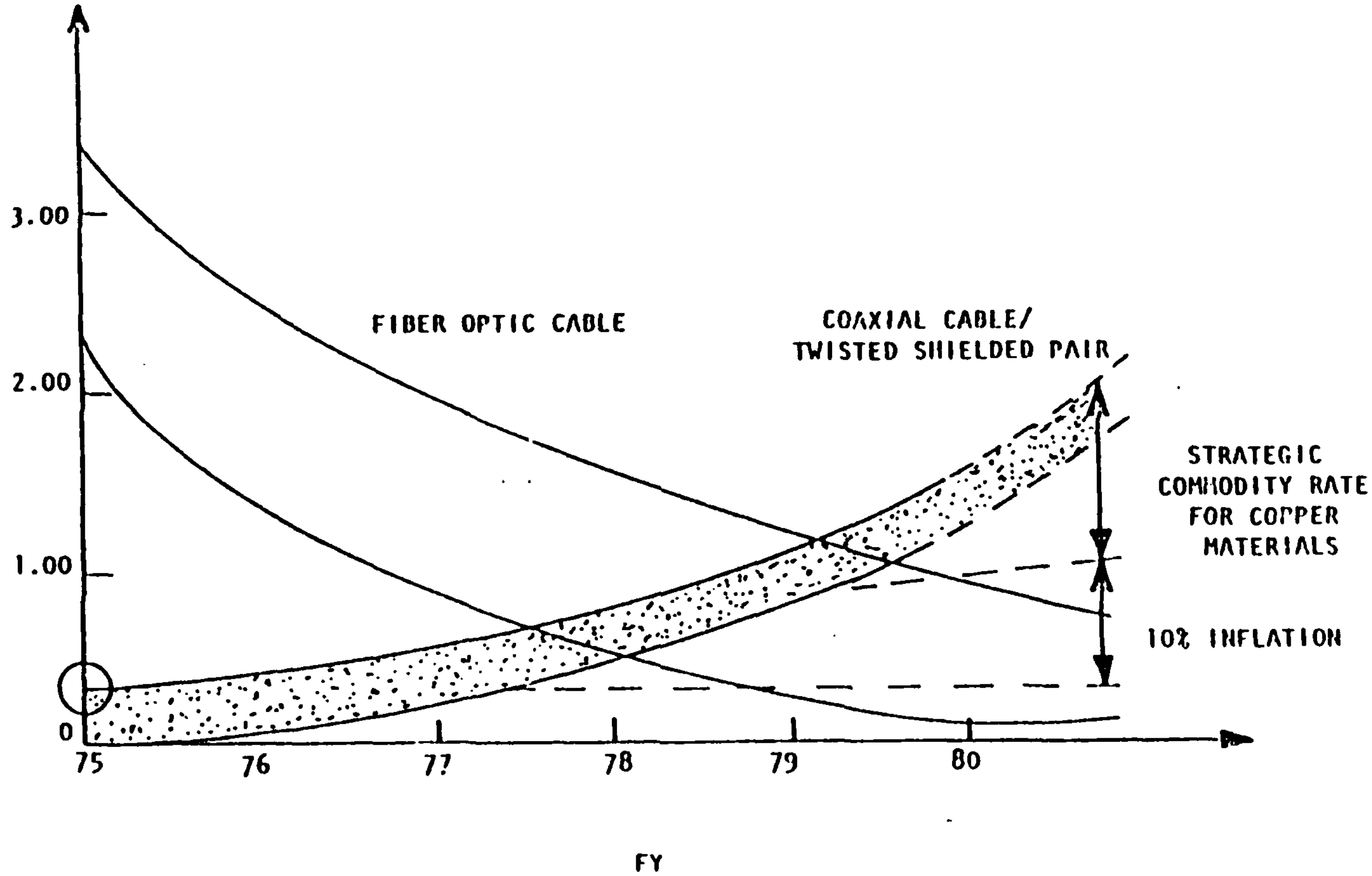


Figure 8.6 Cable Costs Versus Time [8.16]

Table 8.2 A-7 Aloft Displaced Wires and Connectors* [8.16]

COMPONENT	TYPE	R'ORD QNTY	$COST/UNIT	TOTAL COST	UNIT WT	TOTAL WT
COAXIAL CABLE	RG-179B/V	222 FT	$0.1045/FT	23.20	0.0170 LBS/FT	3.77 LBS
WIRE, UNSHIELDED	M22754/16-22	222 FT	0.0228/FT	5.06	0.00368 LBS/FT	0.82 LBS
WIRE, SHIELDED	M17500A22/TE1T14	456 FT	0.0882/FT	40.22	0.0088 LBS/FT	4.01 LBS
2 WIRES, SHIELDED	M27500A22/TE2T14	192 FT	0.1405/FT	26.98	0.0169 LBS/FT	3.24 LBS
3 WIRES, SHIELDED	M27500A22/TE3T14	24 FT	0.1700/FT	4.08	0.0206 LBS/FT	0.49 LBS
WIRE, 2 SHIELDS	M27500A22/TE1V14	543 FT	0.1285/FT	69.74	0.0188 LBS/FT	10.21 LBS
2 WIRES, 2 SHIELDS	M27500A22/TE2V14	231 FT	0.2314/FT	53.44	0.0319 LBS/FT	7.37 LBS
CONNECTOR, RECEPTACLE (212 CONTACTS)	CVC6092 - IN	7 EA*	30.79 EA	61.58	0.72 LBS EA	1.44 LBS
CONNECTOR, RECEPTACLE (212 CONTACTS)	CVC6093 - IN	2 EA*	32.81 EA	65.62	0.64 LBS EA	1.28 LBS
COST OF TERMINATING ABOVE AND TESTING FINAL HARNESS	LABOR	42 HRS.	20.00/HR	840.00		2.00 LBS**
COST/WEIGHT TOTALS				$1,189.92		34.63 LBS

*These connectors are not actually replaced by the aloft components, but an approximately equal number of contacts (424) are idle in the subsystems involved after aloft modification. In actuality these 424 signal contacts are normally distributed over 9 of these types of connectors along with power wires in the original computer interface configuration.

**This additional approximate weight is generated by the termination, potting, and harnessing materials.

Table 8.3 A-7 Aloft Fiber Optic Cables and Connectors

COMPONENT	TYPE	R'QRD QNTY	$COST/UNIT	TOTAL COST	UNIT WT	TOTAL WT
FIBER OPTIC CABLE*	VALTEC (IBM P/N L20-262-1)	224 FT	$ 2.50/FT	560.00	1.3 LBS/100 FT	2.91
	VALTEC (P/N L20-262-2)	224 FT	2.00/FT	448.00	0.68 LBS/100 FT	1.52
SINGLE CHANNEL BULKHEAD CONNECTORS	IBM (P/N L20-24)	13 EA	2.50 EA	32.50	0.0297 LBS EA	0.38
SINGLE CHANNEL PRESSURE BULKHEAD CONNECTORS	NELC (P/N 6507)	5 EA	3.50 EA	17.50	0.0499 LBS EA	0.25
MULTICHANNEL BULKHEAD (RACK-PANEL) CONNECTOR	ITT CANNON (P/N DBK-4B)	1 EA	294.05**	294.05	0.559 LBS EA	0.55
COST OF TERMINATING, POLISHING, AND TESTING FINAL HARNESS	LABOR	12 HRS	20.00 HR	240.00		
COST/WEIGHT TOTALS				$1,592.05		5.61

* The first listed fiber optic cable was the cable selected by IBM for their delivery of the aloft system. The second listed cable is the alternative set of cables being procured by NELC in time for the flight test. The new cable has the same optical properties, but utilizes a new lightweight, nonconductive HYREL© jacket in lieu of the PVC jacketed, steel MONOCOIL© for protective packaging.

** $500.00 setup.

36 to 40 mils thick, and coax cable from 29 to 500 lbs/1000 feet and .012 to 8 inches thick. Comparing three equivalent cables 4 mm (1/8 inch) in diameter and 300 meters long, the bandwidth of fiber optics (300 MHz) far surpasses the 20 MHz data rate limit of coaxial cable and the 1 MHz limit of shielded, twisted pair cable. Due to this bandwidth advantage, fiber optics offers a significant reduction in cable weight and volume on a total system basis as compared to wire systems. This was clearly demonstrated in an A-7 aircraft's navigation and weapons delivery system where a weight savings of 70 pounds and a 95 percent reduction in total wire length (4800 feet to 260 feet) were realized using data multiplexing and fiber optics.

Although few problems are experienced with fiber optic cables, there are some problems in regard to metallic connectors, LED sources, and photoelectric receivers. These all must be shielded from EMP/EMI. LEDs are temperature dependent [8.16]. The current cost of connectors, sources, and receivers are high, although this is expected to change. See also References 8.17 through 8.25.

8.5 Examples of Use of CMR Techniques for Non-Antenna Interfaces

An EMP hardened circuit test showed that pulse transformer coupled circuits can provide very good immunity against EMP induced surges with inexpensive, simple components. Cable driver and receiver circuits were built and tested under both pulse injection and EMP simulated fields. The data rate capability of these circuits was arbitrarily set at 1 million bits per second (mbps).

A further research and development effort deals with the practical application of EMP hardening to two specific areas by using the pulse transformer technique. The first area is protection of a flip-flop circuit within a computer system and the second is the design of a pulse transformer coupled wideband data transmission link.

In the first application, it was suspected that an existing problem within the computer caused a control flip-flop output transistor to fail when the computer was subjected to a simulated EMP test. Although methods for protecting this transistor existed (protective devices or filtering), it was desired to apply the pulse transformer technique to prevent excessive EMP coupled energy from reaching the transistor. This technique, if successful, could then be used more generally to provide circuit immunity as shown in work on transformer coupled data links.

The second application, the pulse transformer data coupling technique was refined for use in systems requiring 1 MHz to 10 MHz data transmission rates. Also, the effects of alternate transformer winding configurations were investigated; winding type as well as circuit connection as series or shunt transformers were checked. The transformers were tested for their common mode rejection properties by both frequency domain and pulse tests while the transformer - line receiver combination was subjected to functional tests under both pulse injection and parallel plate simulator tests. The significance of the common mode rejection properties of the various configurations was then analyzed with a view toward determining preferred protection approaches.

8.5.1 Pulse Transformer for EMP Protection of Flip-Flops

The application of miniature pulse transformers for coupling vulnerable circuits within a computer was developed. In particular, pulse transformer circuits were designed to interface with certain logic gates in a computer system, where a suspected EMP coupling problem existed. The goal was to protect a flip-flop output transistor, which fed a gate through an approximate 2 foot length of wire. Because the operation of the computer is asynchronous, and it was decided not to alter any existing clocking or logic within the computer, the added isolation circuit had to pass direct current. An upper pulse rate capability of 1 mbps was deemed more than adequate to accommodate the smallest transition periods of this first generation, transistorized, discrete component machine. Hence a DC-to-DC converter, in effect, was required with a pulse transformer to isolate the flip-flop from the long connecting wire. Also, the number of components and their size had to be minimized because the existing boards were already highly populated.

There were two general techniques by which this coupling could be accomplished:

1. Convert the flip-flop's DC output to AC (for a pulse train), transmit the AC through a shunt connected pulse transformer and rectify the received signal. This was done with an oscillator, gated by the flip-flop output. Two types of oscillators were built for this function:

   a. a blocking oscillator whose pulse transformer was the isolation transformer.

   b. a gated (ring) oscillator composed of logic gates.

   The principle of this technique is shown in Figure 8.7a where the transformer provides common mode rejection to any EMP coupled energy.

2. Use of a series connected transformer. A series connected pulse transformer can be used for circuit protection as shown in Figure 8.7b. The flip-flop passes a differential signal through the series transformer to the receiving logic gate, but rejects an EMP coupled pulse since it appears common mode. The principle of a series transformer common mode rejection and its performance are presented under Paragraph 8.2.5 - Pulse Transformer Coupled Wideband Data Transmission Link. For computer circuit protection, it would represent a very simple and effective means of protecting the flip-flop with the wiring shown in Figure 8.7b.

Of the two techniques, the shunt transformer circuit has been found to be generally more versatile. Because of its isolation properties, it does not depend on a good ground return for its operation. The following paragraphs describe the interface circuitry required for shunt connected transformer implementation.

The first approach investigated for coupling the flip-flop to the shunt transformer was a blocking oscillator circuit. A schematic for the blocking oscillator implementation is shown in Figure 8.8. The flip-flop (No. 326) gates the blocking oscillator, composed of Q_2 and the transmitting pulse transformer, on or off through Q_1. When the flip-flop output is 0 volts, Q_1 is off and the circuit oscillates at a frequency determined by the transformer inductance and circuit resistance. When the flip-flop output is -6 volts, the base of Q_1 is

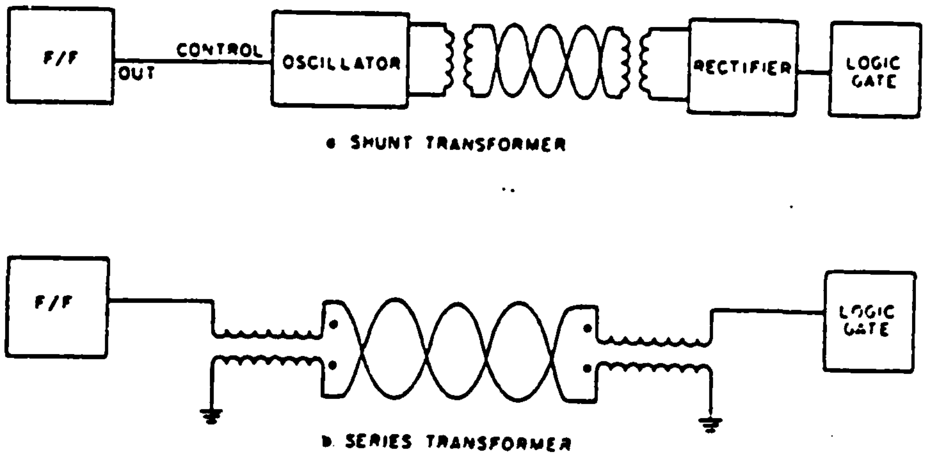


Figure 8.7 Application of Pulse Transformer to Isolate Flip-Flop [8.26]

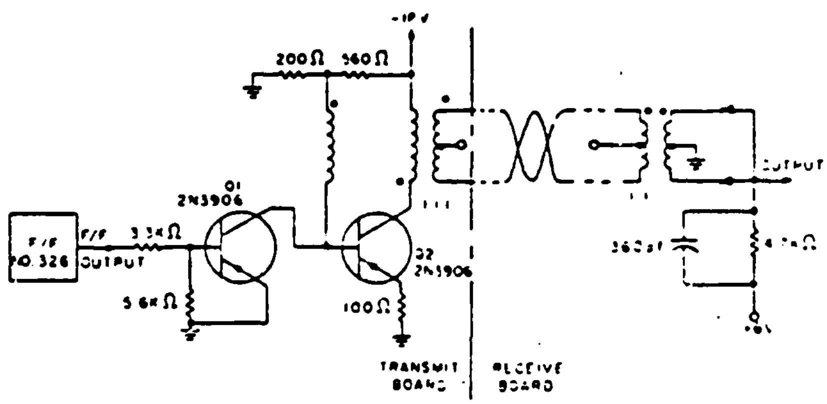


Figure 8.8 Blocking Oscillator Implementation [8.26]

held off, preventing oscillation. The secondary of a receiving transformer contained on the end of a twisted pair line is shown connected to a full-wave rectifier. The rectifier output is 0 volts or -6 volts, reproducing the original flip-flop's output.

In a preferred approach, a gated oscillator using an IC is shown in Figure 8.9 where the frequency of oscillation is independent of the pulse transformer properties. This circuit uses a quad dual-input gate IC driving a pulse transformer. Three gates in a feedback loop oscillate while the fourth gate is controlled by the flip-flop. The oscillator frequency of this approach (as in the blocking oscillator approach) must be much greater than the computer clock rate so as not to introduce too much delay in the flip-flop output path. The circuit shown oscillates at about 5 MHz. Figure 8.9 also shows alternate wiring configurations, whereby the rectifier can be used on a receiving transformer or on the secondary of the transmitting transformer. In the latter case, a fully balanced transmission link is sacrificed for the ability to place all componentry on the transmitting board. Some degree of common-mode rejection is provided, however.

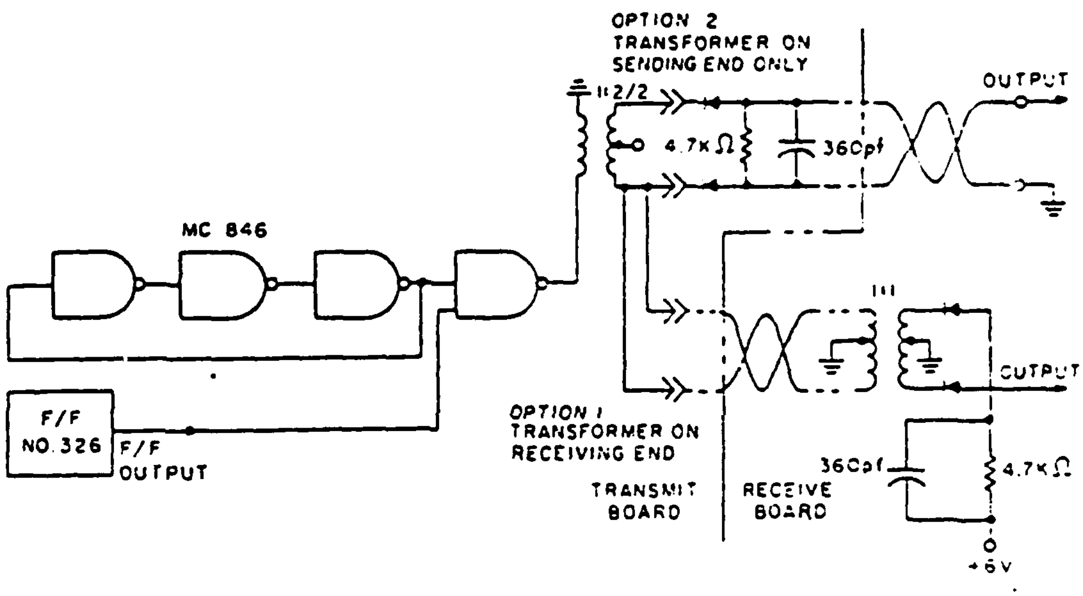


Figure 8.9 Gated (Ring) IC Oscillator Implementation [3.26]

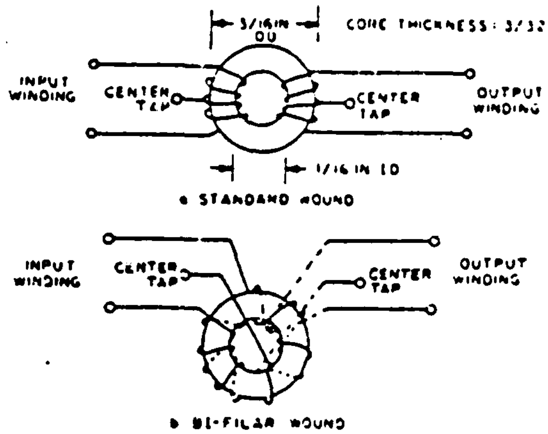


Figure 8.10 Alternate Winding Configurations [8.26]

8.5.2 Pulse Transformer Coupled Wideband Data Transmission Link

The main areas of investigation in the development of a pulse transformer coupled wideband data transmission link were:

1. Design or selection of suitable transformer(s).
2. Determination of optimum winding arrangement.
3. Design of driver and receiver amplifiers.

These areas are elaborated upon in the following paragraphs.

8.5.2.1 Transformer Selection

The main objective in design or selection of a suitable transformer was to obtain a single miniature pulse transformer which could function over the entire range of data rates. In general, small transformers are good for high frequencies, while large transformers are good at low frequencies.

In one approach, two relatively small (3/16" OD) transformers (one each for transmitting and receiving circuits) were hand wound, and, when properly driven, provided capability for transmission from 30 thousand bits per second (kbps) to 10 million bits per second. Slightly larger commercial transformers (1/2 x 3.8 x 5.8", potted) functioned from 1 kbps to 2 mbps. The hand wound cores were wound both in bi-filar and standard modes for comparison, as shown in Figure 8.10.

In an alternate approach, a single large (2 x 2 x 1-1/2") commercially available transformer was shown to be capable of transmitting data over the whole range. Although this transformer has a voltage-time (ET) product of 25 x 10^{-3}

volt-seconds, its high quality (low leakage inductance and low winding capacitance) allows it to function at high bit rates as well as low bit rates.

8.5.2.2 Winding Arrangements

Winding arrangement refers to the connection of the transformer primary and secondary to the cable. Series connected transformer circuits were explored, as well as shunt connected transformers. The two basic types are depicted in Figure 8.11 (a and b). Obviously, there is no lower frequency limit when using series connected transformers. Series connection will theoretically offer the same common-mode voltage rejection as shunt connection, and a single miniature pulse transformer will function for the whole data rate range of interest. It does not provide the ground isolation features inherent in shunt connection, however, A typical circuit employing series transformers which will pass a differential signal but reject a common mode signal is shown in Figure 8.11c. An analysis of this circuit reveals that the output voltage is given by

$$V_{out} = \frac{RV_{in}}{s(L-\frac{M^2}{L}) + R} \tag{8.1}$$

where L is the self inductance of the cells, M is the mutual inductance between the coils, and s is the Laplace operator. Under ideal coupling conditions M equals L and (8.1) reduces to

$$V_{out} = V_{in} \,. \tag{8.2}$$

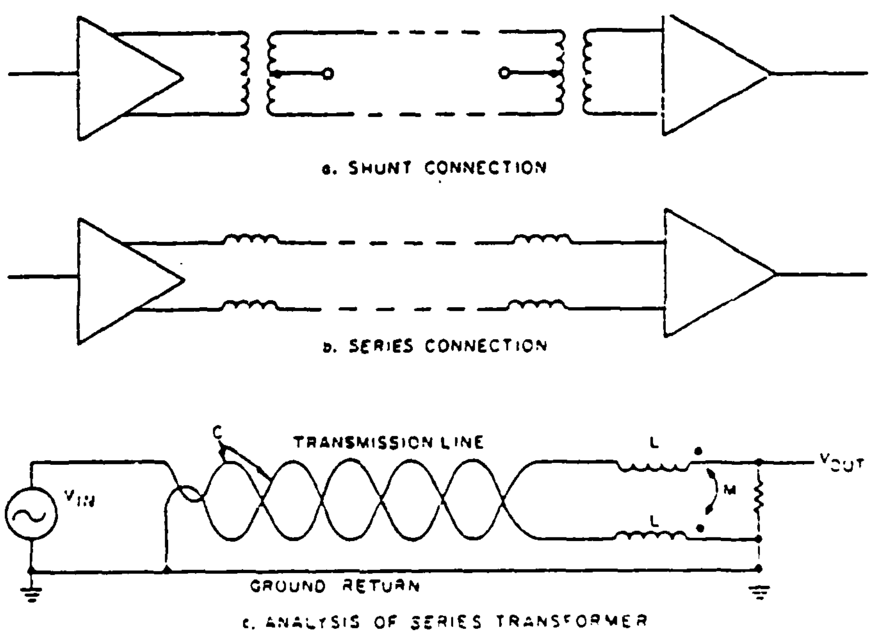


Figure 8.11 Winding Arrangements [8.26]

If a common mode signal, V_{com}, were injected at point C, the output voltage due to V_{com} would be given by:

$$V_{out} = \frac{RV_{com}}{s(L+M) + \frac{RL}{L-M}} \tag{8.3}$$

If L = M, Equation (8.3) reduces to

$$V_{out} = 0 .$$

Thus, it has been shown that under ideal conditions the series transformer will transmit differential signals unattenuated, while completely attenuating common mode signals.

This analysis assumes that grounds were ideal and that no common mode signal appeared on the ground return lead. If either of these conditions is not met, or if the conditions are only partially met, then the common mode rejection of the system will deteriorate accordingly.

8.5.2.3 Design and Performance of Coupling Circuits

8.5.2 3.1 Shunt Transformer Circuit

The critical component in the transformer interface circuit is the transformer driver. It is found that the effective bandwidth of a particular pulse transformer is directly related to or directly affected by the transistor drive circuit. A novel feedback amplifier was designed for extending the low frequency response of a given transformer. principle is based on providing greater drive current through the transfo primary as the pulse width increases. This circuit is not required for series connected transformers.

If a pulse transformer is driven from a voltage source, the low frequency response can be significantly extended when compared to driving it from a matched or higher impedance source. This is seen in Figure 8.12 where a typical pulse transformer terminated in 1.3 kΩ is driven from two different impedance levels: 50Ω and 1.3 kΩ. This particular transformer is bi-filar wound. The basic limitation with low impedance drive is the excessive current demand at low frequencies.

The driving circuit for extending the low frequency cut off of a pulse transformer is given in Figure 8.13a, with successive improvement factors. The input drives a differential switch composed of transistors Q_1 and Q_2, with a current source transistor Q_3. The primary winding, P, is driven from the collector of Q_1 and the secondary winding, S, drives the cable. As a first improvement, R_s is placed across the primary to reduce the driving impedance. Then a third winding F, on the transformer, provides a feedback signal to Q_2 to further improve the low frequency response without increasing power drain.

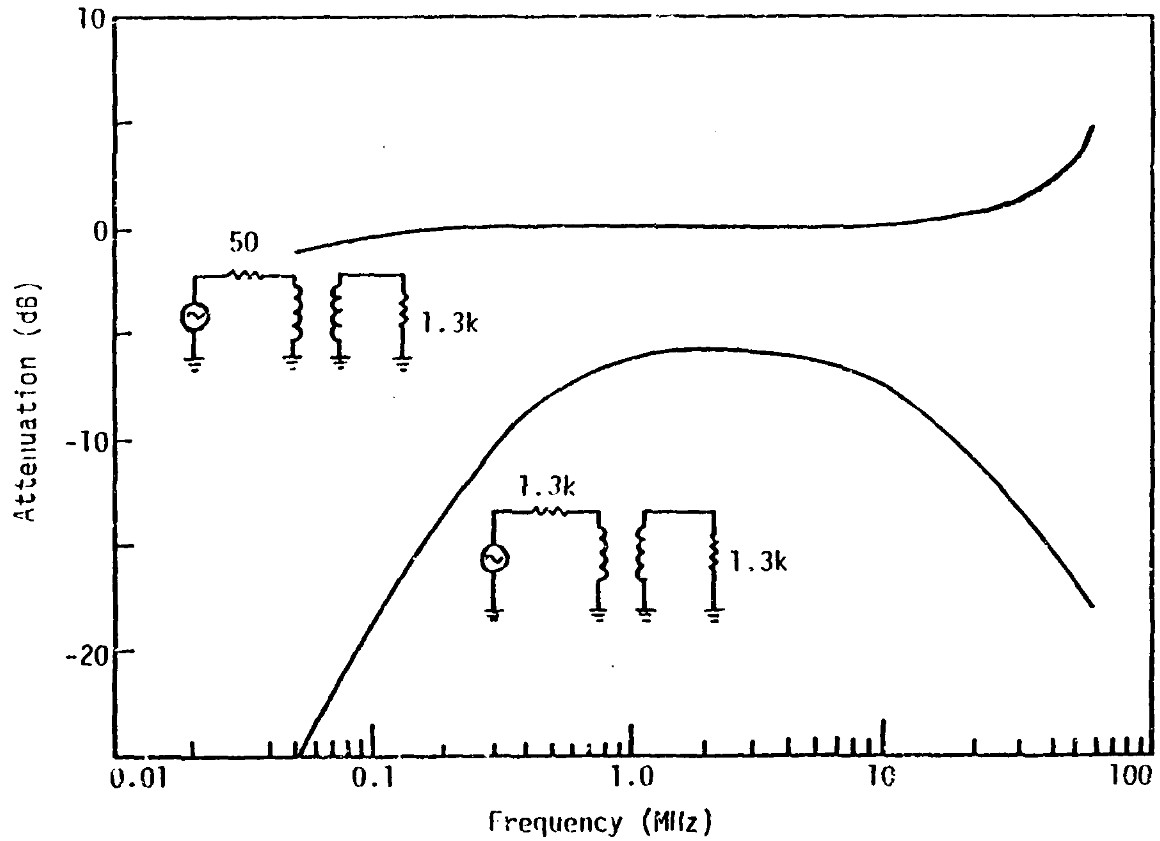
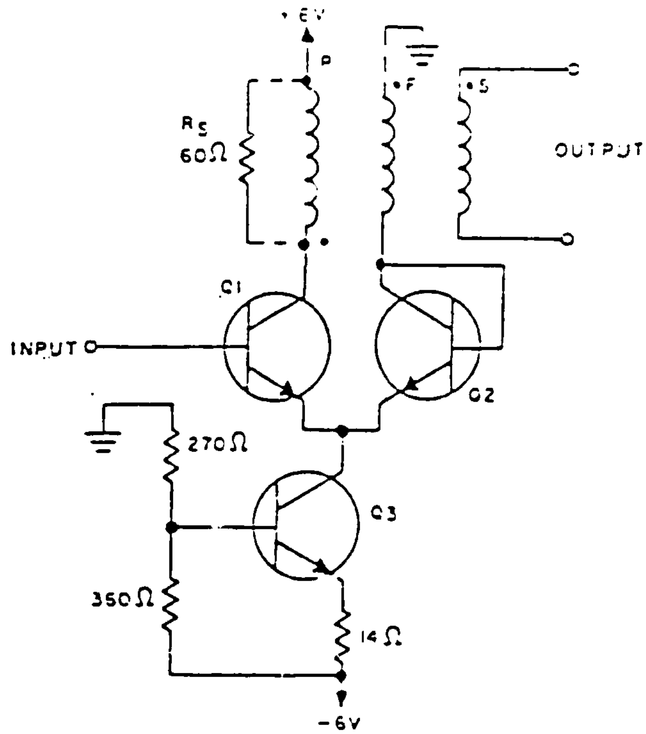
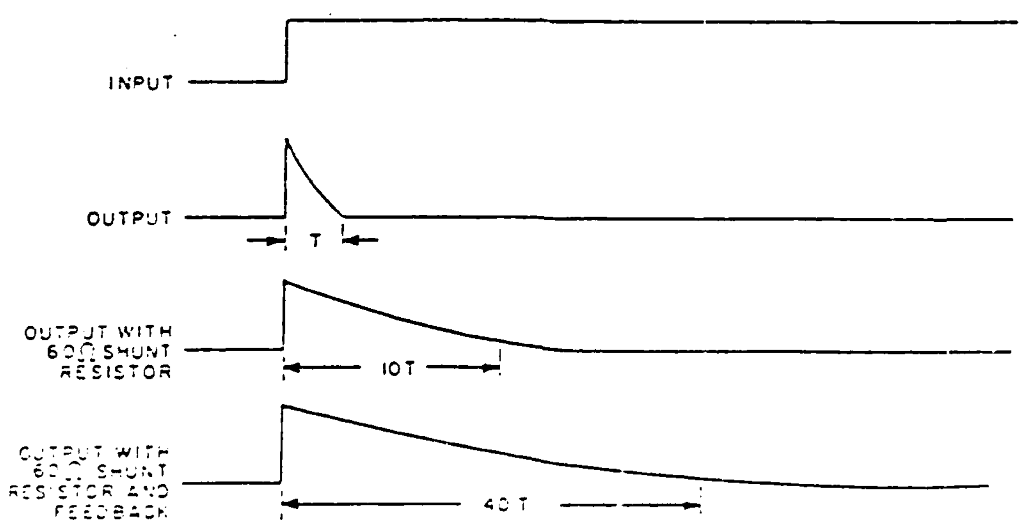


Figure 8.12 Effect of Driving with Different Source Impedances [8.26]



a. Schematic



b. Waveforms

Figure 8.13 Driving Circuit for Extending Low Frequency Cutoff of a Pulse Transformer [8.26]

The feedback operates in the following manner. A measure of the output voltage, effectively impressed on the base of Q_2, is compared to the input voltage. If the output voltage tends to drop below the input voltage a greater share of the current source (from Q_3) will flow through Q_1 and winding P; if the output voltage tends to exceed the input voltage, a larger portion of the current source flows through the feedback winding F. By shifting current between windings P and F, the output voltage on S will track the input voltage until Q_1 either cuts off or turns on completely.

These limits are ultimately determined by the input pulse width, the magnitude of the current source and the characteristics of the transformer. Figure 8.13b shows the relative effects of providing a low impedance source and then feedback to the basic transformer drive circuit. The output pulse width is extended by a factor of ten by using a low impedance source and an additional factor of four (total of 40) by using feedback, when compared to driving the pulse transformer directly from the differential switch.

The complete transmission link, including the differential pulse receiver, is shown in Figure 8.14. The waveforms of the transmission line for both transformer types operating at the extremes of their bit range are shown in Figures 8.15 and 8.16. Ideally, each waveform should approach a square wave for best signal-to-noise transmission. The actual waveforms are considered satisfactory at their worst case conditions of minimum bit rate.

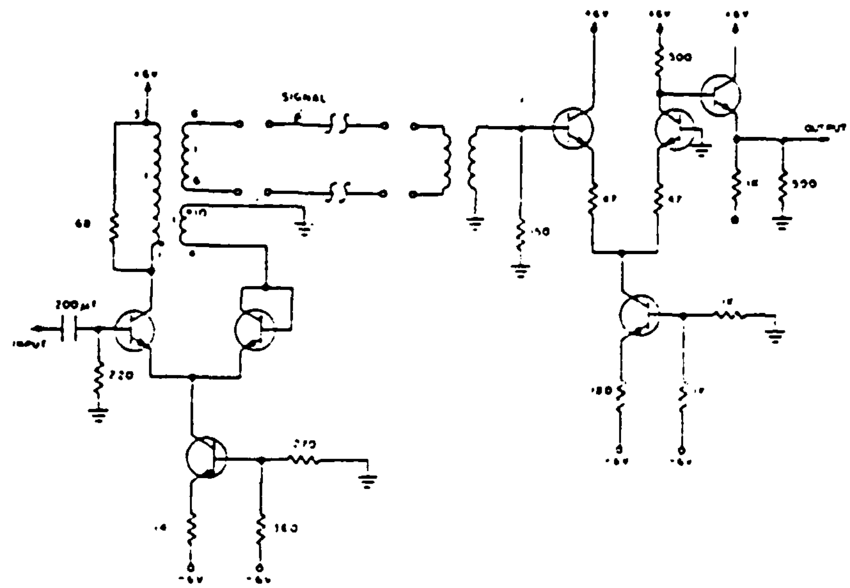


Figure 8.14 Line Driver and Receiver
(1 kbps to mbps) [8.26]

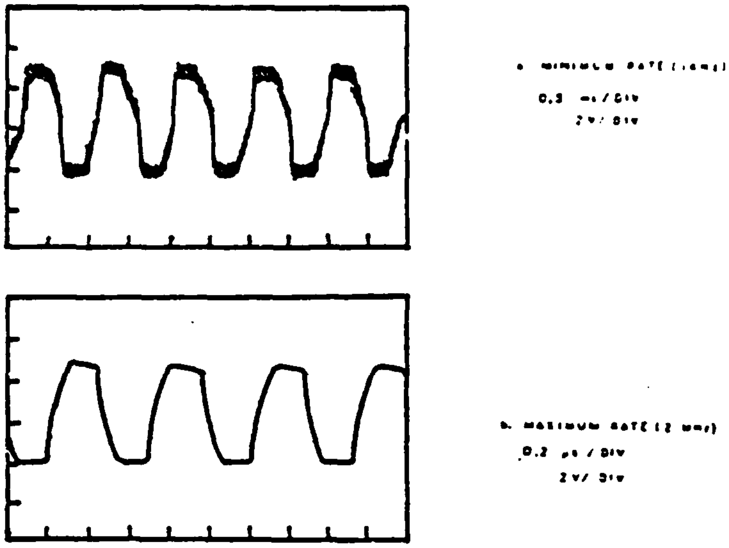


Figure 8.15 Waveforms for Lower Bit Range (Large Transformer L_{cc} = 1 mh) [8.26]

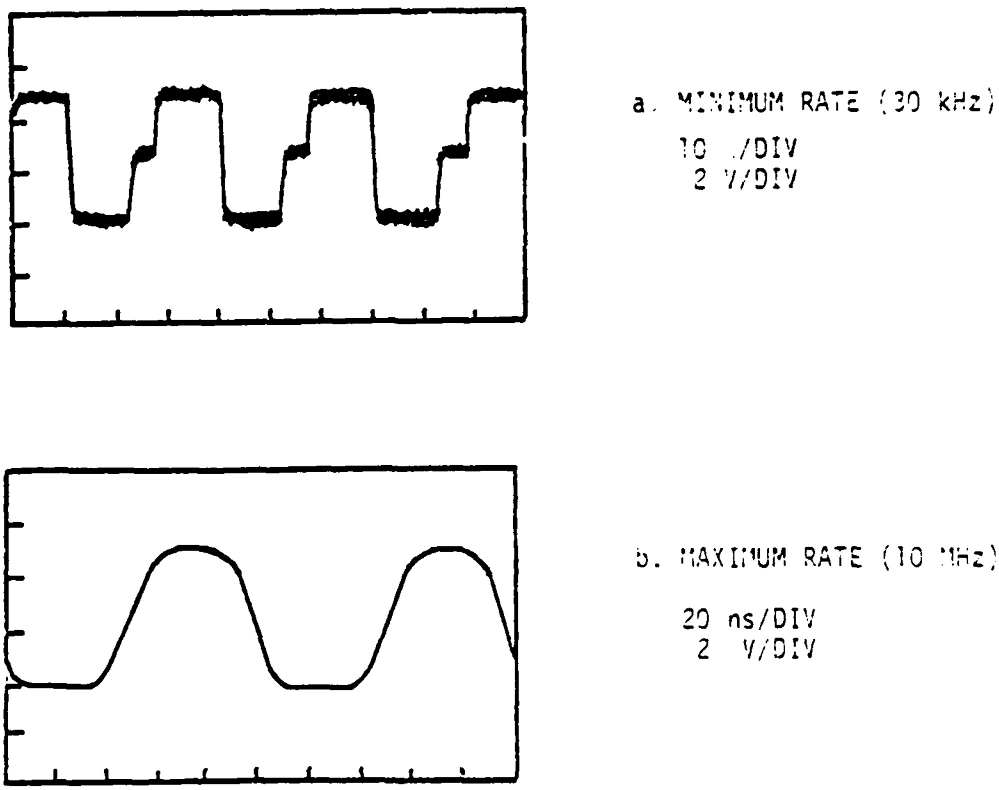


Figure 8.16 Waveforms for Higher Bit Range (Small Transformer L_{oc} = 200 μH) [8.26]

8.5.2.3.2 Wide Bandwidth Transformer

A commercially available wide band transformer was purchased in an attempt to obtain a component capable of functioning over the whole data band of interest; i.e., a single transformer capable of holding a pulse as long as 1 ms and as short as 0.1 μs. The Deerfield Laboratory of Los Altos, California, manufactures transformers which easily meet these specifications. The model 162 75 Ω transformer was driven as shown in Figure 8.17 for testing. It is seen that the feedback winding is not required. The operating waveforms of Figure 8.17 are shown in Figure 8.18, where pulse inputs of 0.1 μs, 50 μs and 2.4 ms are displayed. The fidelity over the whole range is noted from about 400 bps to 10 mbps. The volume and cost of this transformer are, however, much higher than those of two miniature units used to cover the whole range. The per unit cost is $75, versus approximately $2 to $3 for the small units, and the volume factor is at least 25 to 1.

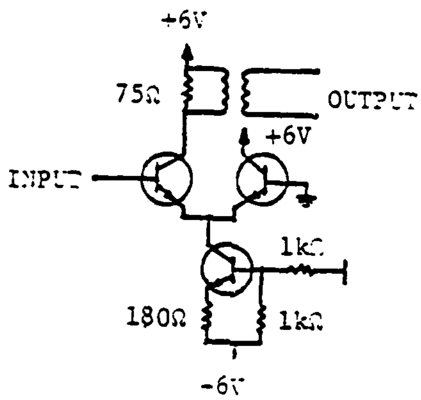


Figure 8.17 Wide Bandwidth Transformer Driver [8.26]

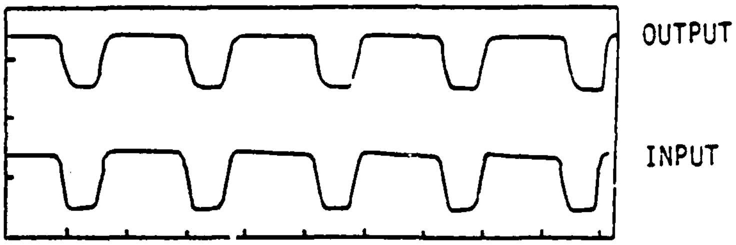
8.5.2.3.3 Series Transformer Circuit

A complete transmission link for a series transformer connection is shown in Figure 8.19. Both the driver and receiver circuits consist of a TTL gate and emitter follower, and a single transformer serves from DC to 10 mbps.

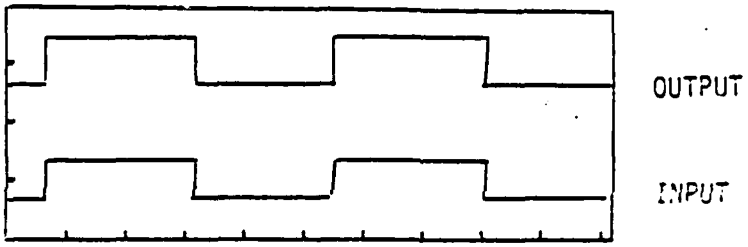
8.5.3 Common Mode Frequency Tests

Series of tests were performed to determine the common mode properties of the various transformers used in the circuits. The first test was concerned with the common-mode rejection (CMR) property of the transformer in the frequency domain. Figure 8.20 shows the test set-up for the shunt and series transformer circuit configurations.

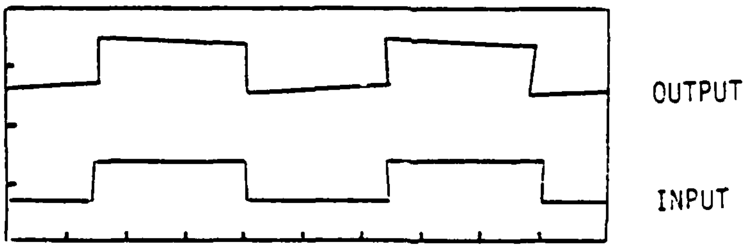
Results of the common mode rejection tests (Figure 8.21) show that the CMR of the shunt transformers decreases monotonically with increasing frequency, while the series transformers CMR decreases at both very low and very high frequencies. These trends are readily understood by referring to (3.1).



1V/DIV., 0.1μS/DIV.



1V/DIV., 20μS/DIV.



1V/DIV., 1mS/DIV.

Figure 8.18 Waveforms of Wide Bandwidth Transformer [8.26]

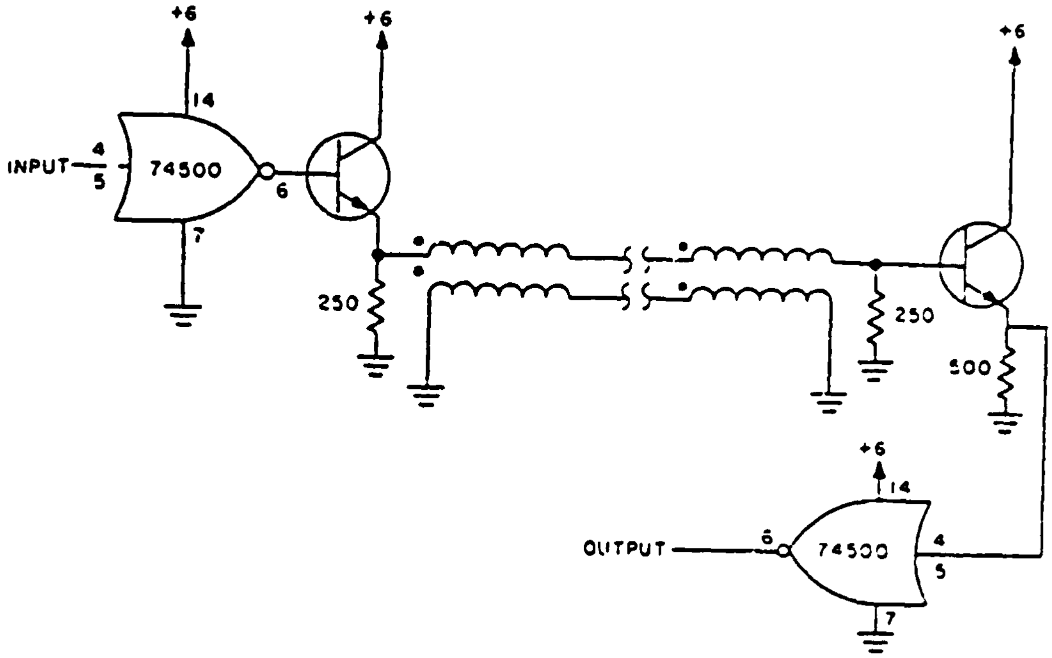


Figure 8.19 Series Transformer Line Driver and Receiver [3.26]

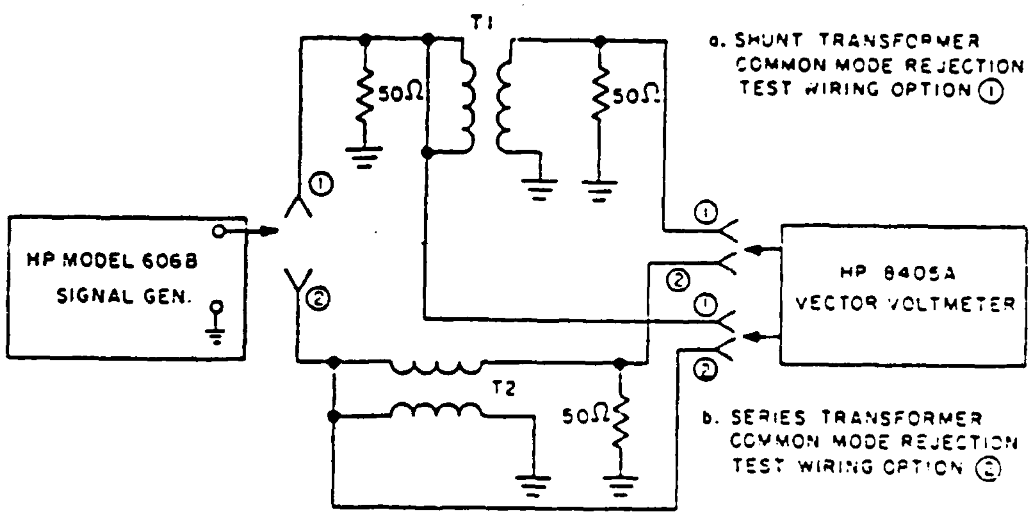


Figure 8.20 Common Mode Rejection Test Setups [3.26]

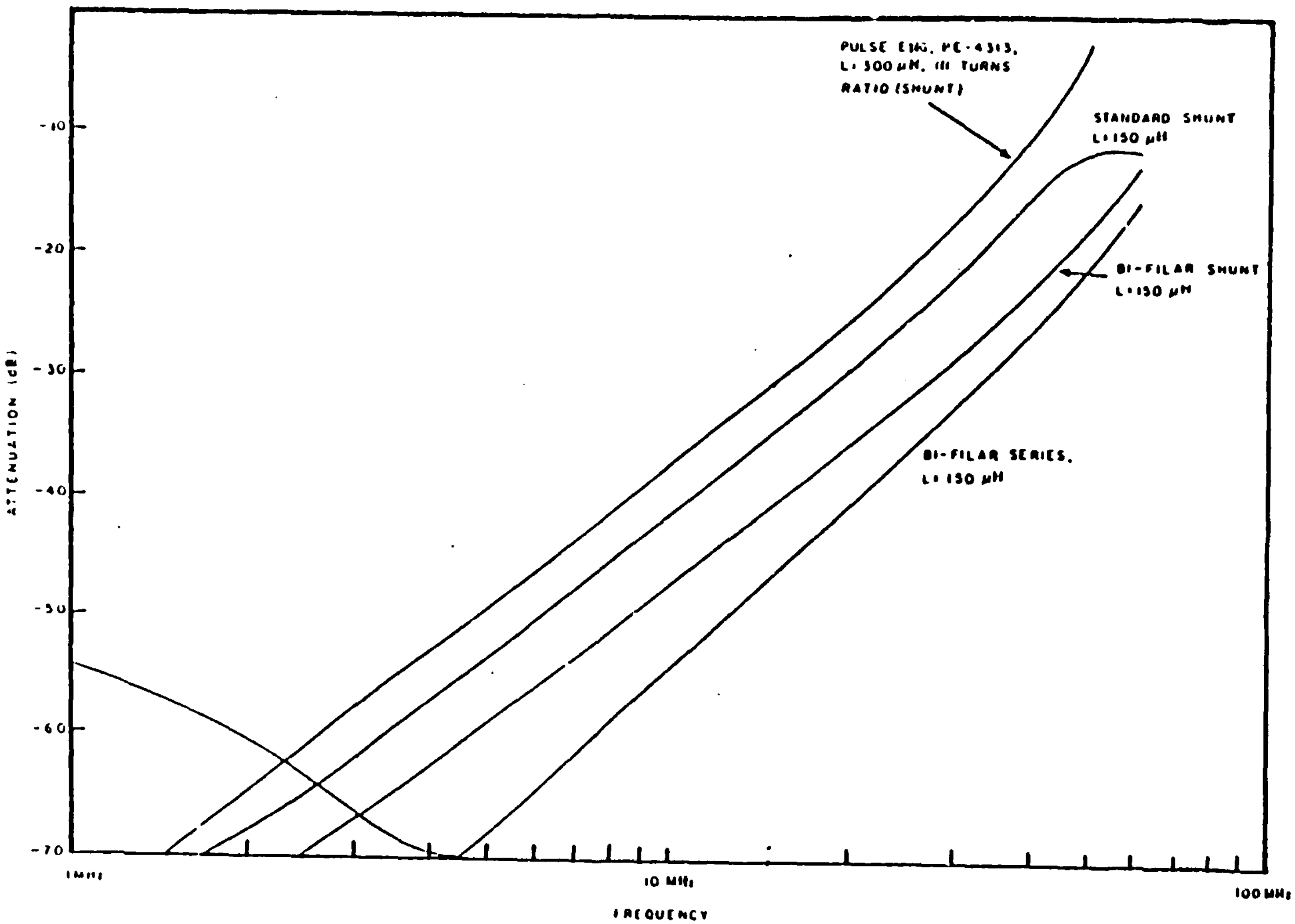


Figure 8.21 Common Mode Rejection Test Curves (Pulse Transformers In Shunt and Series Circuit Configuration) [8.26]

The common mode rejection ratio (CMRR) often is of greater significance as a figure of merit in specifying a transformer than the common mode rejection. The CMRR is defined as

$$\text{CMRR} = \text{CMR/Differential Transmission.}$$

Thus, the next test was concerned with the CMRR, which can be determined by measurement of the differential transmission characteristics of the transformers. The test configuration is shown in Figure 8.22 and the test results in Figure 8.23. The CMRR determined from the above formula is shown in Figure 8.24 for various transformer types and configurations.

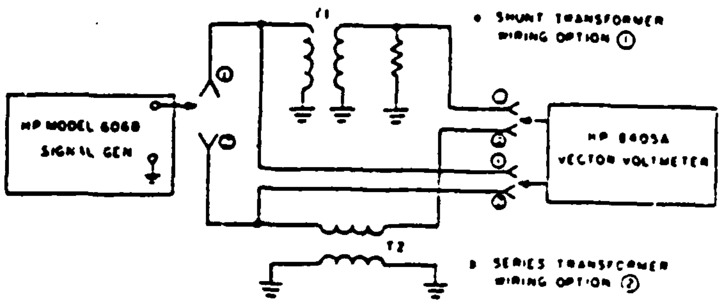


Figure 8.22 Differential Transmission Test Setup [8.26]

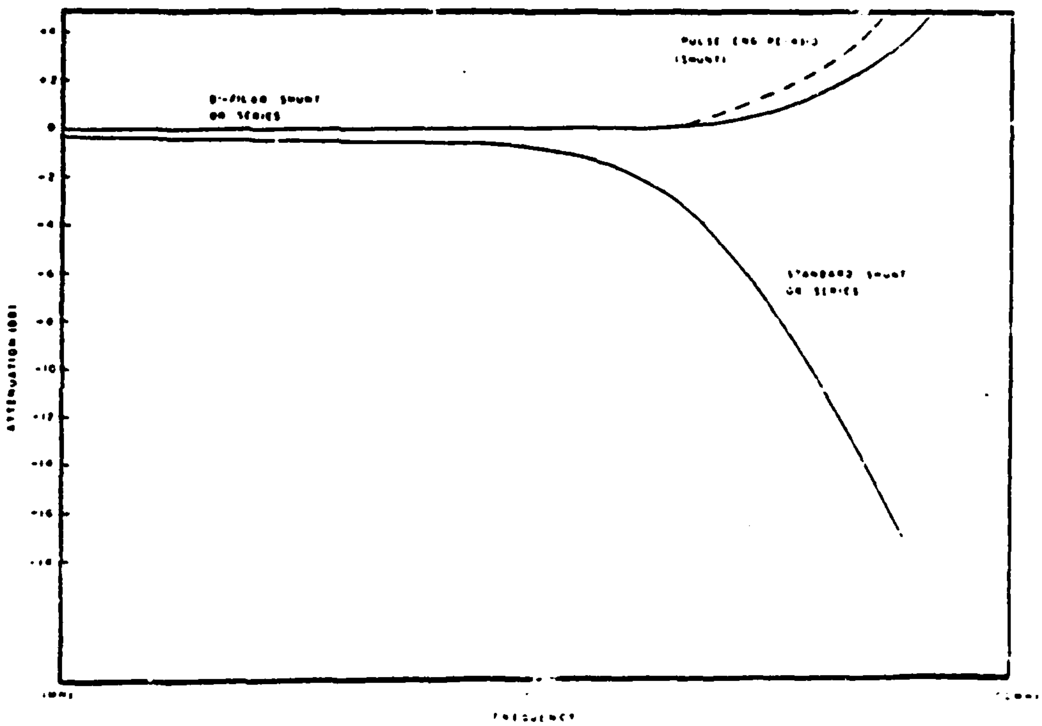


Figure 8.23 Differential Transmission Test Curves [8.26]

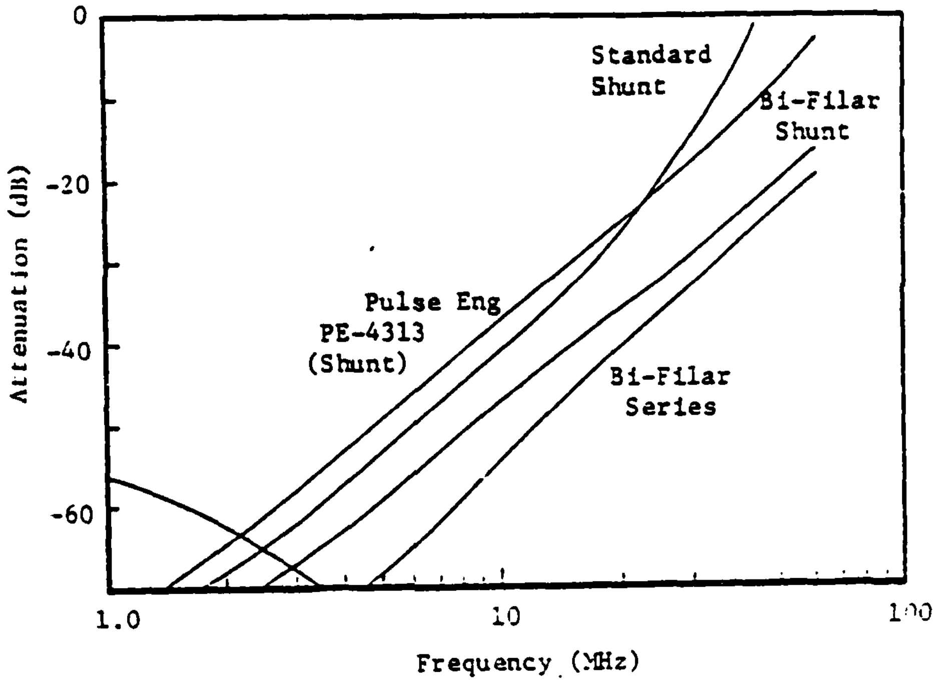


Figure 8.24 Common Mode Rejection Ratio (CMRR)* Curves
*CMRR = Common Mode Rejection ÷ Diff. Trans.

8.5.4 Pulse Injection Tests

Pulse injection testing was utilized to determine the common mode pulse response of the transformer and to functionally test the transmission link. Both a sub-nanosecond risetime multikilovolt pulse generator (SNMKPG) and a Velonix pulse generator was used in these tests.

The first of these tests was designed to measure the common mode rejection of the transformers to pulses applied at the transformer terminals. The test set-up is shown in Figure 8.25. Figure 8.26a shows the input pulse and Figure 8.26b shows the output waveforms for the standard and bi-filar wound transformers. The output waveform with no transformer (direct wired) in the test set-up is shown as a reference in Figure 8.26b.

The set-up for the second type of test is given in Figure 8.27. Here, a much higher voltage and faster risetime was used and the output from the receiver amplifier was monitored to determine the functional response. Because the cable wires are shorted together, the signal from the line driver will not reach the receiver during the test. The 4300-volt pulse injected on the cable did reach the receiver and caused ringing (about 13 volts peak for 1.8 s). Subsequent tests on the circuit with the short removed from the cable revealed that the 4300-volt, 50 ns pulse caused no damage to the circuits.

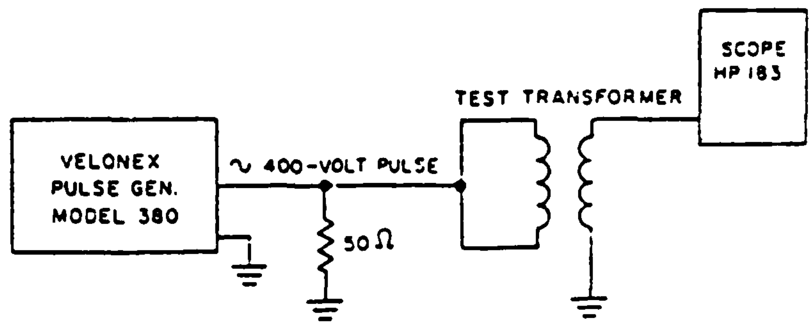


Figure 8.25 Pulse Injection Test Setup [8.26]

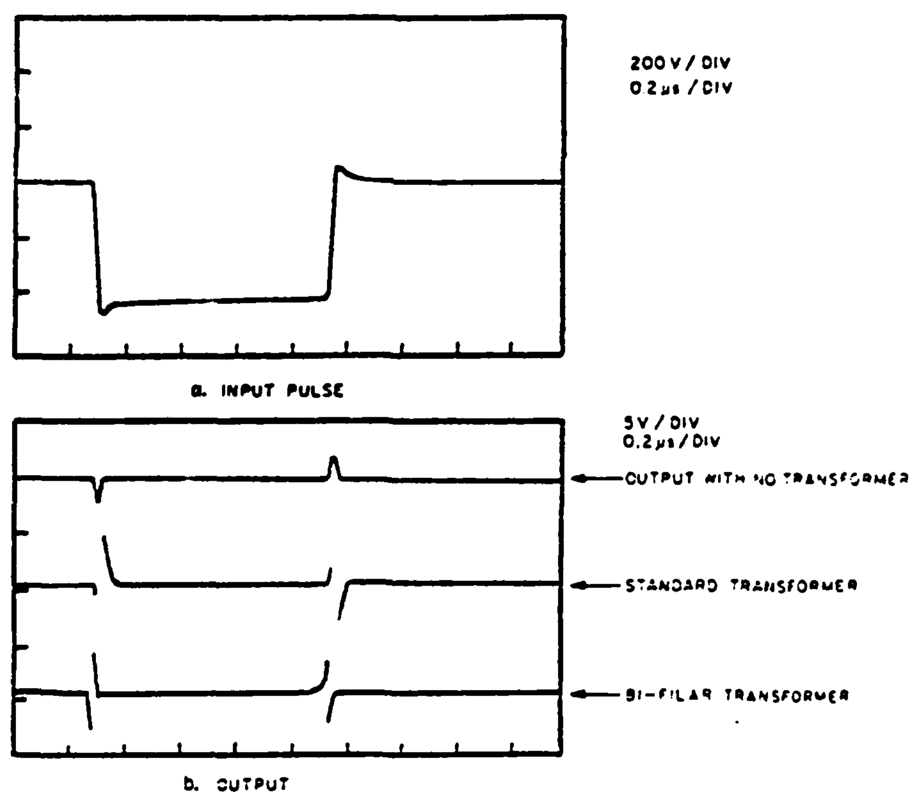


Figure 8.26 Pulse Injection Test Waveforms [8.26]

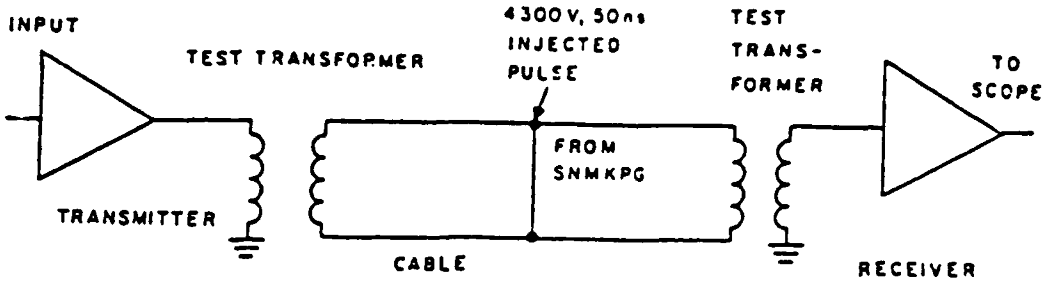


Figure 8.27 High Voltage Pulse Injection Test Set-Up [3.26]

8.5.5 Cable Driver Tests

The cable driver was used for these tests. The purpose of the test was to determine the improvement in rejection to induced voltage (caused by high current pulses in the cable shield) in the cable conductors provided by pulse transformers. The test set-up is shown in Figure 8.28.

A current pulse of 56 A peak amplitude was injected on the outer tube; its return path was through the cable shield. A waveform of the input current pulse is shown in Figure 8.29. Frequency spectra were made at points C and B, respectively, on the cable conductor's output (Figure 8.28). The measurements were taken with and without a pulse transformer in the circuit.

By taking measurements with and without a pulse transformer, it was determined that the transformer increased the rejection of the current pulse on the shield, at point C (Figure 8.28), over that at point B. The increased rejection was 35 dB at 3 MHz and 10 dB at 90 MHz for the bi-filar transformer, and 20 dB at 90 MHz for the standard transformer.

The complete test results are shown in Figure 8.30. Curve A is the shield signal normalized at 0 dB over all frequencies. Curve B is the shielding effectiveness of the shield with respect to the inner conductors, normalized to the 0-dB input signal via the following relation:

SH(f) actual shield current as a function of frequency

IC(f) actual inner conductor current

NIC(f) normalized inner conductor current as a function of frequency

$$NIC(f) = IC(f)/SH(f)$$

Curves C and D represent the shielding effectiveness of the shield and the transformer.

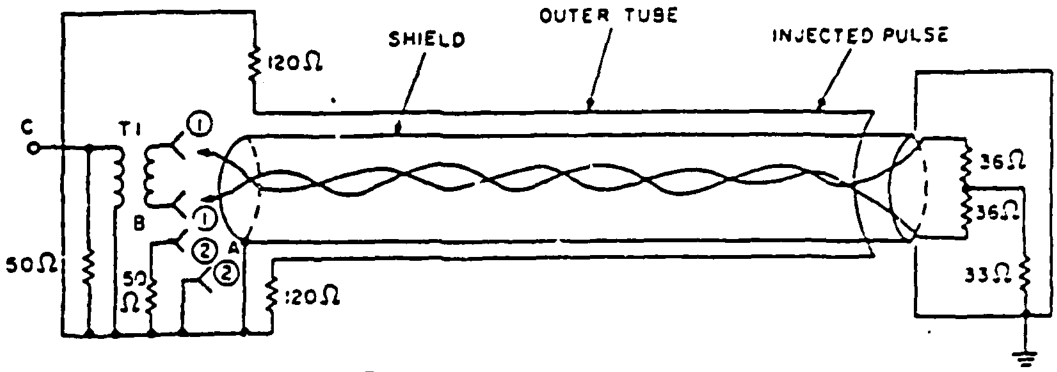
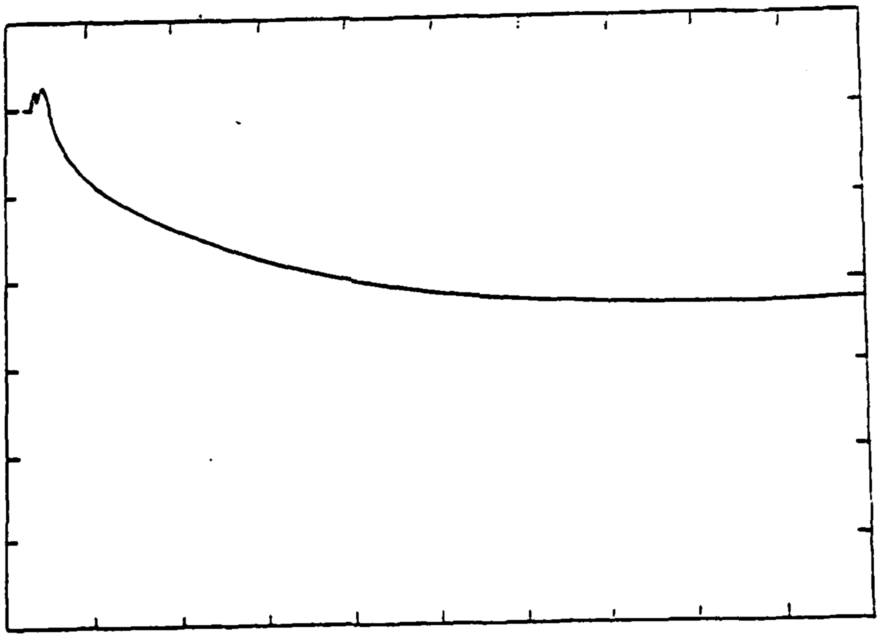


Figure 8.28 Cable Driver Test Setup [8.26]



VERT. 28a/DIV
HORIZ. 100 ns/DIV

Figure 8.29 Cable Driver Pulse [8.26]

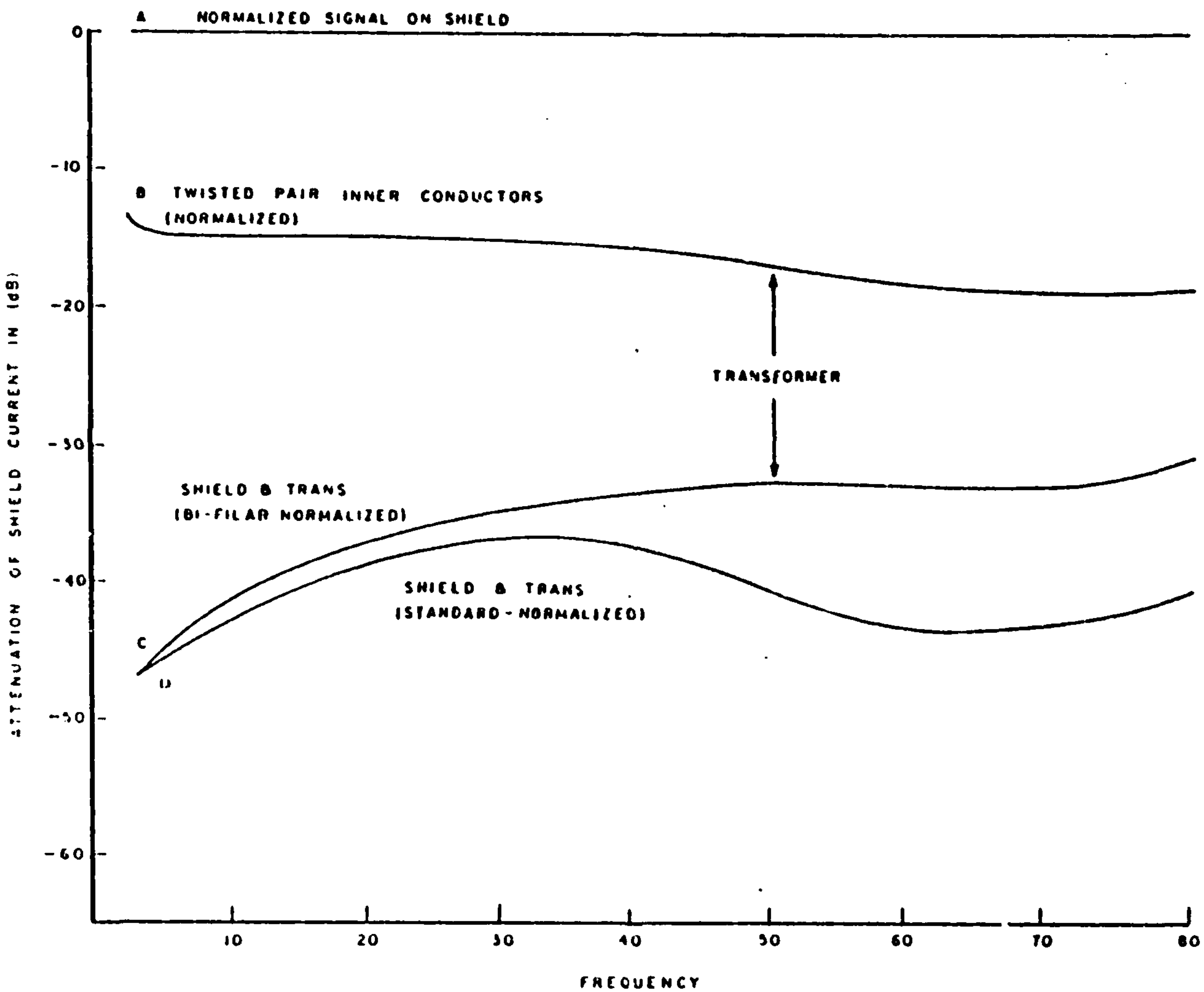


Figure 8.30 Cable Drive Test Curves [8.26]

The difference between curve B and curves C and D represents the increase in rejection of the shield current pulse at the output (point C of Figure 8.28) obtained by using a transformer.

8.5.6 Parallel Plate Simulator Tests

The parallel plate simulator was used to test the effects of a pulse field on the overall transmission link. The transmitting circuit, including an oscillator and cable driver, was battery powered and placed on the top plate of the simulator. The battery powered receiver circuit and an oscilloscope were together in a shielded container. A vertical 8 foot length of cable separated the transmitting and receiving circuits and this length was exposed to the vertically polarized E field pulse generated by the simulator. The test set-up is shown in Figure 8.31. The output of the receiver was monitored during and immediately after the EMP to determine transient behavior of the transmission link as well as ultimate failure level as the EMP magnitude was increased.

Figure 8.32 shows typical responses of the receiver during and immediately after a simulator pulse. Figures 8.32a and 8.32b are for the shunt transformer circuit at two different field amplitudes. The higher exposure response (Figure 8.32b) is actually "cleaner", because (for this test), the cable was isolated. Figure 8.32c shows a typical response with the series transformer circuit. This circuit was successfully tested to a field strength of 22 kv/m. In both cases the pulse rate range for each circuit tested as shown in Paragraph 8.5.2.3. Fields of Figure 8.32 were those indicated by the driving voltage of the power supply.

8.5.7 *Discussion*

Several test methods were used to aid in evaluating and predicting performance of the pulse transformer circuits in a given EMP environment. Some of these tests measured the common mode rejection of the transformers in the frequency domain and others in the time domain. The frequency domain tests were performed with an rf generator, and the time domain (or pulse injection) test method used as Velonex pulse generator and a cable driver. The latter instrument actually represented a hybrid approach because it had a spectrum analyzer attachment for converting a pulse response to its frequency domain equivalent.

Two test methods were used to determine circuit functionality; i.e. how the transformer and its associated electronic circuitry responded to a simulated EMP disturbance. Again, a pulse injection technique was used (but this time on the SNMKPG) as well as a parallel plate simulator. These tests showed that the transmission link would function after the particular given exposures (see paragraphs 7.5.4 and 7.5.5 for a description of the test configurations).

The results of functional tests depend to a large extent on the precise wiring and packaging configurations of the circuits. The settling time due to a disturbance and the ringing are critical functions of the circuit grounding, cabling and positioning with respect to the test equipment. Hence, although the tests on the SNMKPG and parallel plate simulator can indicate whether or not failure levels were exceeded, their effects on the circuit response must be related to specific configuration examples.

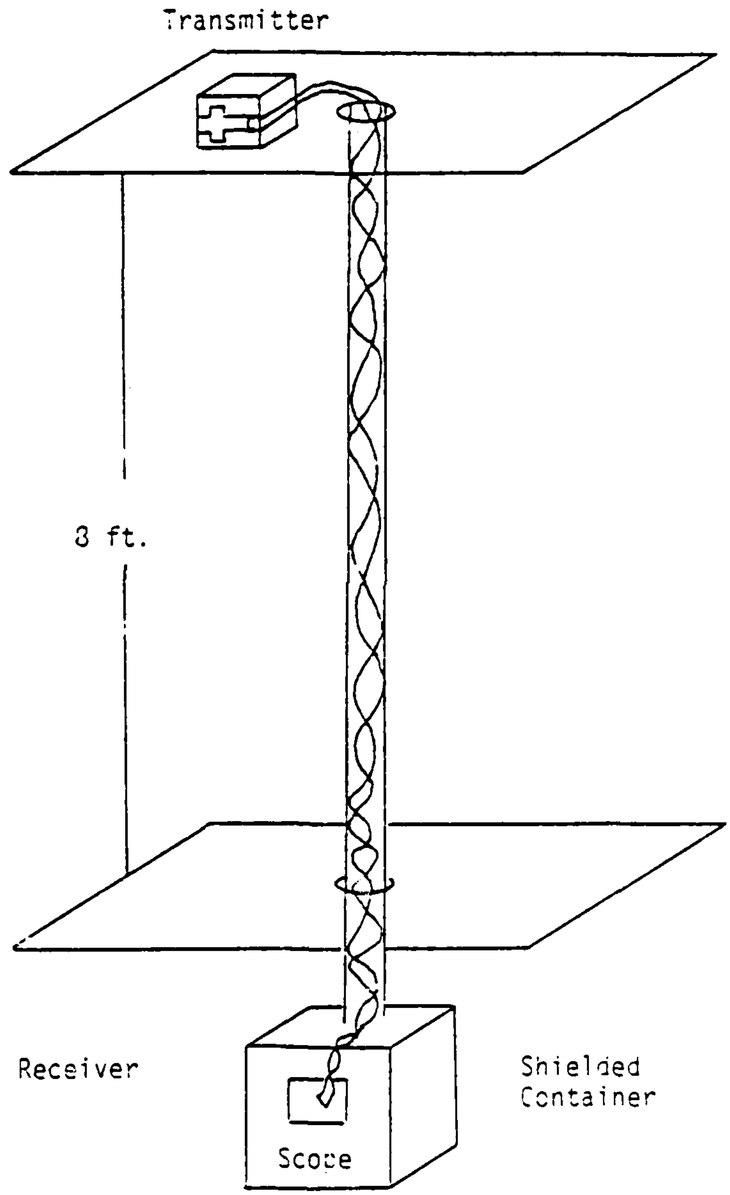
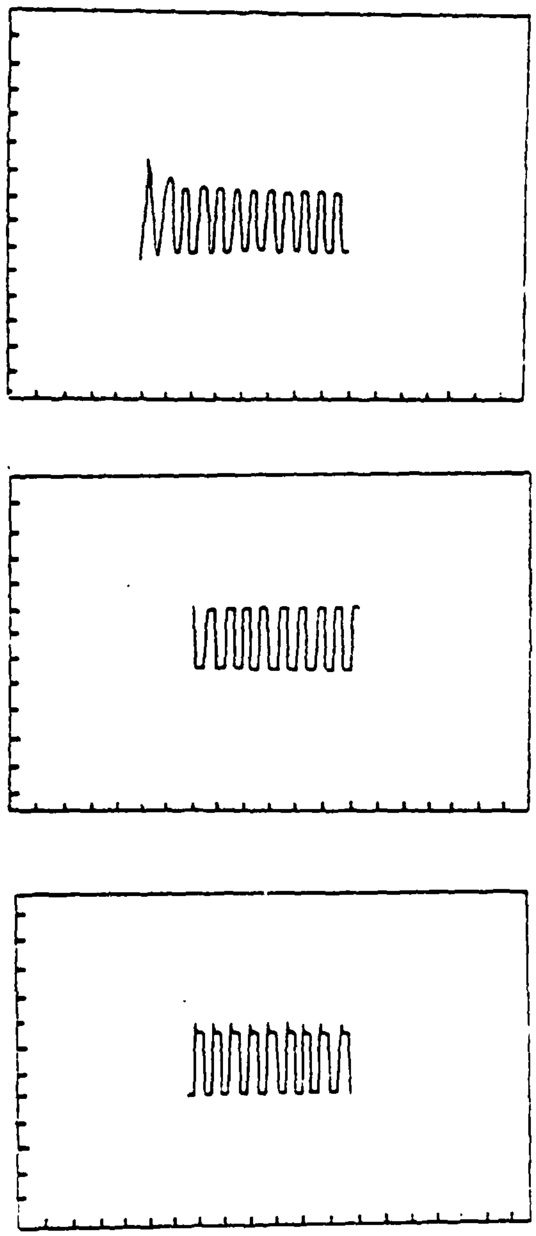


Figure 8.31 Parallel Plate Simulator Test Setup [8.26]



a. SHUNT TRANSFORMER

E=16kV/m

1μs/DIV

2V/DIV

b. SHUNT TRANSFORMER

E=24kV/m

1μs/DIV

2V/DIV

c. SERIES TRANSFORMER

E=8.0kV/m

1μs/DIV

2V/DIV

Figure 8.32 Transmission Link Responses [8.36]

Table 8.4 summarizes the test data from each experiment. As can be seen, not every transformer was tested by each method (indicated by "_____"). The results of the common mode rejection (rf generator), pulse injection and cable driver tests are in general agreement as to the performance of the laboratory unit transformers.

By characterizing the transformer common mode test data to both frequency and pulse techniques, and by relating those results, the data can be useful for various types of EMP specifications. The following discussions analyze and relate the test results.

8.5.7.1 Differential Transmission Tests

The bandwidth of a transformer is limited by parasitic effects, such as interwinding capacitance and leakage inductance. Tests were made on standard and bi-filar wound transformers to determine which transformer had the flattest high frequency response. The results of these tests, (shown in Figure 8.23) indicated that the standard transformer is flat to 10 MHz. After 20 MHz, its response falls off at 20 dB per decade. This roll-off suggests that the standard transformer can be modeled as shown in Figure 8.33.

There is no simple mathematical model to describe the behavior of a bi-filar transformer, such as depicted in the response of Figure 8.23. However, the curve does suggest that a resonance is beginning at 20 MHz. The bi-filar transformer has a flatter frequency response than the standard transformer and is preferred in wide bandwidth applications.

8.5.7.2 Common Mode Rejection Tests

The results of the common mode rejection test (shown in Figure 8.21) reveal that the common mode rejection (CMR) of all the shunt transformers falls off at 40 dB per decade. From this information, a mathematical model can be derived which will predict, within about .15%, the time domain common mode rejection response to the transformer when subjected to various risetime input pulses.

The simplest mathematical model which can be used to predict the CMR of the shunt transformers over the frequency range shown in Figure 8.21 is given:

$$\frac{V_{out}}{V_{in}} = \left[\frac{sRC}{1+sRC}\right]^2 \qquad (8.4)$$

where s = Laplace operator

For the bi-filar shunt transformer, Equation 7-3 becomes:

$$\frac{V_{out}}{V_{in}} \approx \left[\frac{s\,(12.5\times10^{-10})}{s\,(12.5\times10^{-10})+1}\right]^2 \approx \frac{s^2}{(s+8\times10^{8})^2} \qquad (8.5)$$

TEST TYPE	Transformer Connection			
	SHUNT			SERIES
I. Pulse Transformer Performance	Commercial Unit	Standard Lab. Unit	Bi-filar Lab. Unit	Bi-Filar Lab. Unit
Common Mode Rejection 1 MHz	>70 dB	>70 dB	>70 dB	55 dB
10 MHz	37 dB	42 dB	45 dB	55 dB
50 MHz	8 dB	0 dB	16 dB	19 dB
Pulse Injection 400-volt,	—	5-volt peak	4-volt peak	—
15 ns risetime	—	—	—	—
Cable Driver 1 MHz	—	50 dB	50 dB	
(56 A peak) 10 MHz	—	40 dB	33 dB	
II. Fun[illegible]onal Performance (with receiver)				
Pulse Injection 4300-volt, 1 ns risetime, 50 ns pulse width	—	—	Passed Test	—
Parallel Plate Simulation 16 kV/m	—	—	Passed Test	—
22 kV/m	—	—	Passed Test	Passed Test

Table 8.4 Summary of Test Data [8.26]

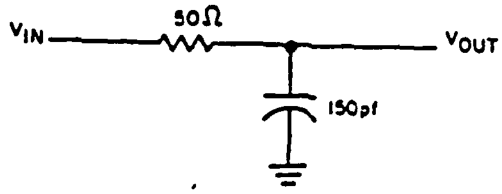


Figure 8.33 Simplified Equivalent Circuit of a Transformer [8.26]

If a common mode input signal of a form shown in Figure 8.34 were applied to the bi-filar shunt transformer, the response of the transformer could be calculated by (8.5).

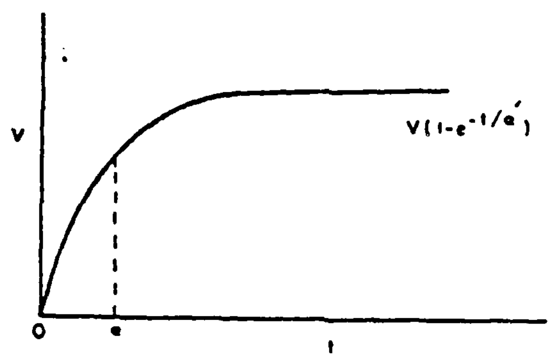


Figure 8.34 Common Mode Input Signal [8.26]

As an example, consider the case where the input to the transformer is given by:

$$V_{in} = V\,(1-e^{-t/\alpha})$$

$$\alpha = 20 \text{ ns}$$

$$V = 500 \text{ volts}$$

The response of the transformer is then given by: (8.6)

$$V_{out}(t) = 500 \left[(4.45 \times 10^{-3})e^{-(3 \times 10^{8})t} - (4.45 \times 10^{-3})e^{-(5 \times 10^{7})t} + t(5.34 \times 10^{7})e^{-(8 \times 10^{3})t} \right]$$

Equation (8.6) is shown graphically in Figure 8.35. Hence, with a knowledge of the transformer frequency domain characteristics, this type of analysis could be carried out for any arbitrary input and the results could be used to predict whether a given input would cause component failure or logic upset.

8.5.8 Test Summary

Pulse transformers have proved to be a versatile and effective component for protecting circuits from EMP transients. Their practical use in protecting internal computer circuits and wideband data transmission link applications was shown. Although the transmission link designs covered data rates from 1 kbps to 10 mbps, it has been shown that frequencies down to 0 Hz can be passed by using series-connected transformers. At the other extremes, bit rates higher than 10 mbps can be accomodated with a reduced overall bandwidth. It is estimated that, with the techniques discussed in this report, bit rates ranging from 1 mbps to 100 mbps can be passed by a single transformer - while still providing EMP protection.

The bi-filar wound units are generally better than the standard, isolated windings. The shunt-connected transformer is more flexible than the series-connected transformer in its application, but the series-connected transformers are preferable for very low frequency work and have added advantage of interface circuit simplicity if grounding configurations permit their use.

Testing proved that injection pulses of 4300 volt peak, 50 ns width and 400 volt peak, dc did not damage the pulse transformer isolated circuitry. Free fields of 22 kv/m were also withstood by the shielded twisted pair. However, in each of these cases, coupled energy could have upset associated logic circuitry. Finally, a useful analysis tool was demonstrated for predicting the output from a given transformer (due to an injected pulse input) when its common mode rejection properties are known in the frequency domain.

The experiments, data and analysis of this report can serve for similar applications within vulnerable systems. Also, the results are seen to provide a

framework for extending these techniques to not only preventing circuit damage due to EMP coupling, but also to preventing logic circuit upset.

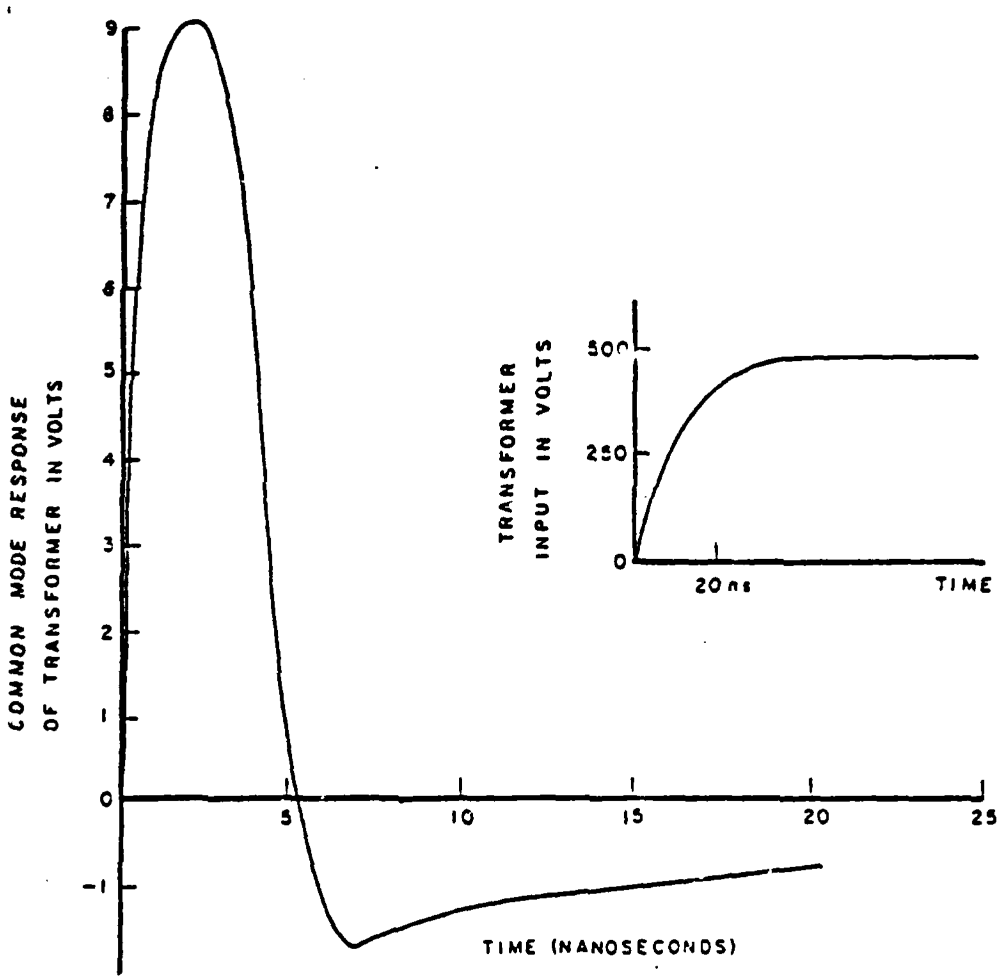


Figure 8.35 Computed Common Mode Response (Bi-Filar Transformer to 500 Volt, 20 ns Risetime Input) [8.26]

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CHAPTER 9

GROUNDING AND BONDING

9.0 Executive Summary

EMP can couple large transients onto the ground system. Thus the methods used for grounding and bonding are important features for hardening shipboard systems. Even grounding measures at the component level are important in the overall reduction of coupled EMP energy. Thus Chapter 9 serves as a design reminder that grounding and bonding practices are an integral part in EMP hardening of equipment.

9.1 Background

In this handbook, a distinction between grounding and bonding is made: grounding guidelines state where to make the connection, and bonding guidelines state how to make the connection.

Ground conductors should be viewed as potential EMP problems rather than cures. Grounding serves no useful interference or signal transmission purpose; it is a safety measure.

For shipboard equipment, there are two separate ground systems, the signal ground system and the structural ground system. The structural ground system consists essentially of the hull and structures attached to it (for metallic hull structures) or cable ground system (for nonmetallic hulls). The structural ground system provides for personnel safety. The signal ground system, as illustrated in this handbook, serves as an electrical reference. The relationship of the two ground systems is shown in Figure 9.1, which shows two equipment racks A^1 and B^1 connected together, and the racks have electronic boxes A and B which "talk" to each other. MIL-STD-1310D [9.1] states that the racks need to be locally connected to the structural ground systems as shown. Signal grounding practices are concerned with how the returns for signal and power are made for systems as well as within equipment racks and the electronic boxes themselves.

Grounding and bonding practices for the structural ground system are discussed in MIL-STD-1310D [9.1]. There it is stated that for metallic hull ships, all equipment shall be connected to the foundation (which is at hull potential) in a manner shown in Figure 9.2. The ground system for nonmetallic hulls is shown in Figure 9.3. In this case, the equipments are locally connected to the ground cable as shown.

In this handbook, the primary concern about equipment is the signal ground system. General grounding principals will first be given, and then specific problems will be discussed. General bonding guidelines will then be presented.

9.2 Grounding

There are two basic grounding principles that should be followed to reduce the transmission and coupling of EMP energy into electronics. They are:

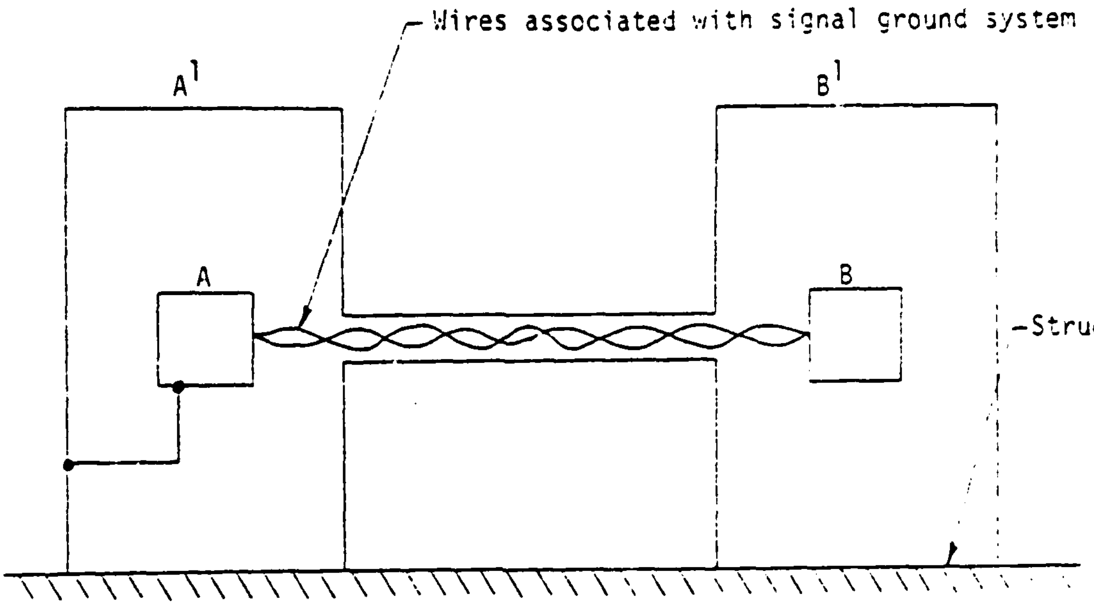


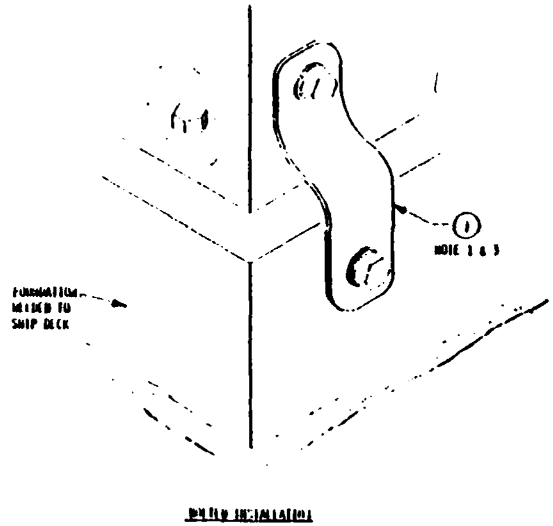
Figure 9.1 Illustration of Signal and Structure Ground Systems

1) Grounding conductors (such as cable shields, ground straps, etc.) should not penetrate the surfaces of shielded volumes, and
2) Ground loops should be minimized.

9.2.1 Examples of General Grounding Principles

In this section, grounding principles which apply to more complex systems will be demonstrated by simple examples.

Consider the ground configuration of Figure 9.1 which shows two circuits, X and Y, located remotely from each other. Wire CD is the "high side" of a signal path, and the "low side" consists of wire EF and AB and of the path in the imperfect ground plane, FA. The imperfect ground plane could represent either the hull or even a "Faraday cage" shield within a hull. This configuration presents two problems. First, the ground potential V_g caused by current flowing in the finite resistance ground plane is applied directly across the circuits X and Y; this voltage could appear as a spurious input signal. Secondly, if the configuration is illuminated by a uniform B-field perpendicular to the plane of loop ABC-DEFA, this B-field induces a voltage in the loop of the form V_{oc} = (loop area) $\times \frac{\partial B}{\partial t}$. This voltage also appears across the electronics in the form of a spurious input. For these reasons, the configuration of Figure 9.1 is not recommended.



ITEM NO	LIST OF MATERIAL PART	SPECIFICATION	NOTE
1	BOND STRAP, TYPE III		1,3
2	BOND STRAP, TYPE IV		2,3,4

NOTES:

1. TYPE III BOND STRAP SHALL BE INSTALLED ONLY IF EMI TESTS INDICATE THE NEED.
2. BOND STRAPS FURNISHED WITH ELECTRONIC EQUIPMENT BY MANUFACTURERS MAY BE USED FOR BONDING RESILIENT MOUNTED EQUIPMENTS IF EQUAL TO, OR SIMILAR TO, THE TYPE III OR IV BOND STRAP AS SPECIFIED HEREIN. WHEN A BOND STRAP IS NOT FURNISHED WITH AN EQUIPMENT, A TYPE IV BOND STRAP SHALL BE INSTALLED. BOND STRAP INSTALLATION SHALL NOT DEFEAT PURPOSE OF RESILIENT MOUNT.
3. WHERE POSSIBLE, USE EXISTING BOLTS, STUDS OR HOLES FOR ATTACHING BOND STRAP.
4. AS AN ALTERNATIVE, A TYPE III BOND STRAP MAY BE INSTALLED ON SHOCK MOUNTED EQUIPMENT.

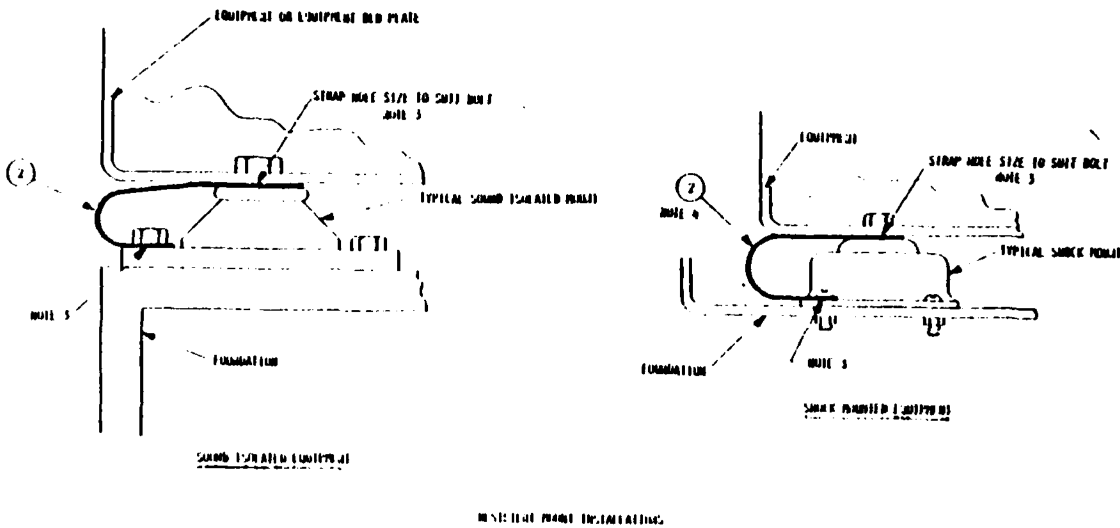


Figure 9.2 Grounding of Equipments and Enclosures [9.1]

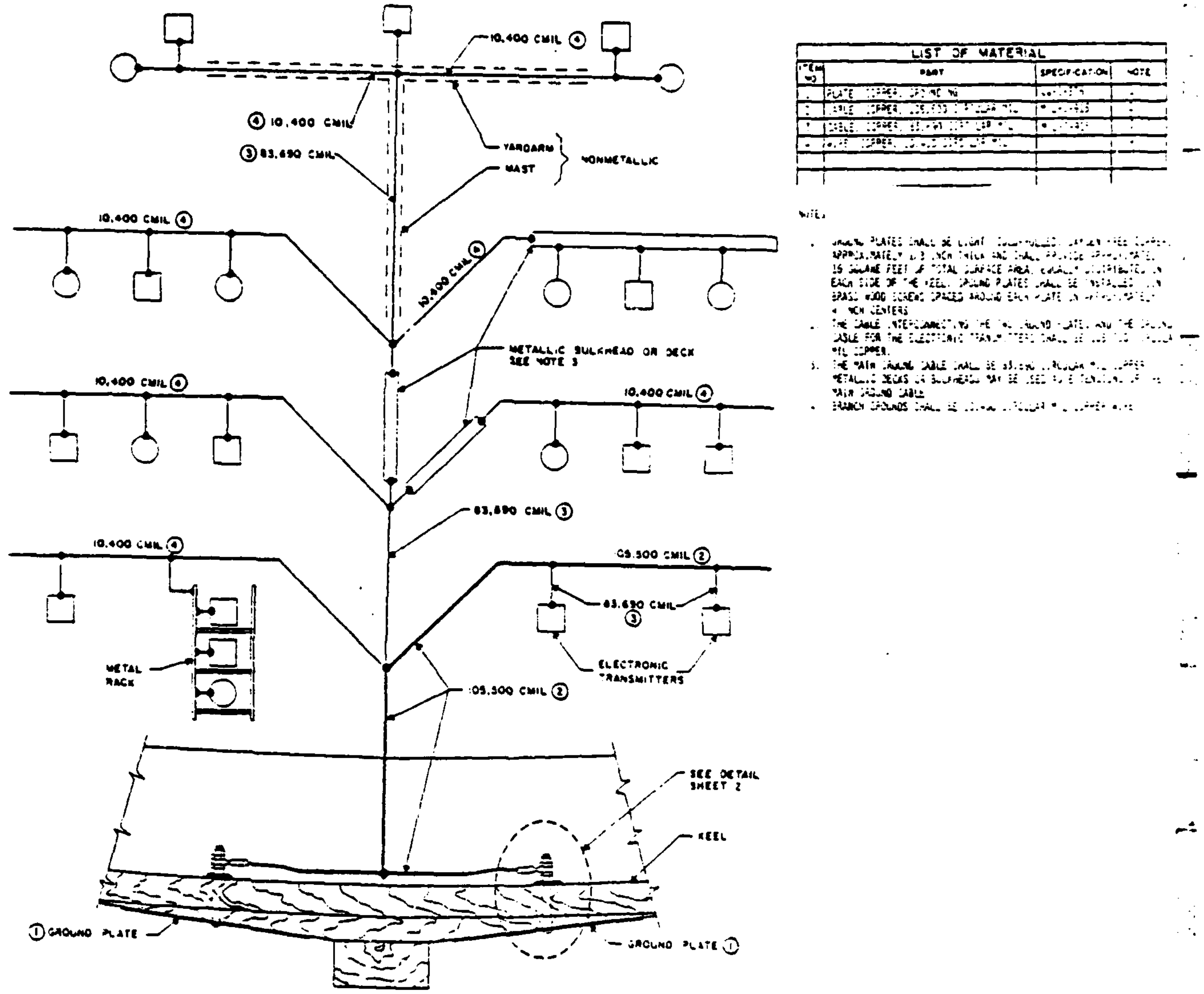


Figure 9.3 Ground System, Nonmetallic Hull Ships [9.1]

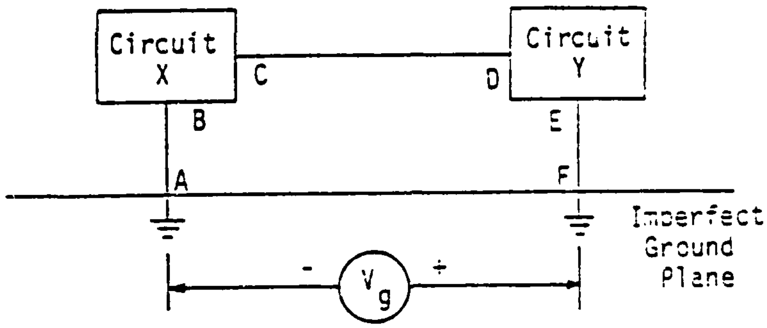


Figure 9.4. Double Point Ground

The ground potential V_g can be eliminated by using the singlepoint ground configuration of Figure 9.5. Here, the currents flowing in the ground plane causing V_g do not couple to the electronics. In this configuration, loop ABCDA is still susceptible to magnetic loop coupling.

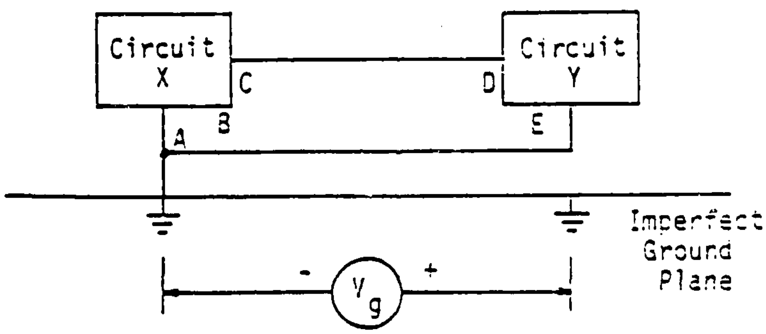


Figure 9.5 Single Point Ground

The loop coupling problem can be minimized by using twisted pair cables for the signal and its return (Figure 9.6). The loop area is considerably reduced by the twisted pair cables, and alternate loop voltages approximately cancel each other. Note that in Figure 9.6 the ground in circuit X is made inside the shielded volume and resumes on the exterior of the shield surface.

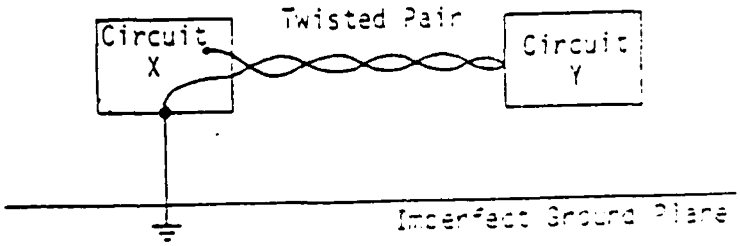


Figure 9.6 Reduction of Magnetic Loop Pickup

In Figure 9.7, a further refinement of Figure 9.6 is provided by shielding all electronics and cabling. Circuit X, circuit Y, and the twisted pair are now enclosed in a total shield consisting of conducting boxes and the cable shield. Note that the low side of circuit X is connected to its shield, but that circuit Y is not. From an EMP point of view, it is usually preferred not to connect points C and D together. However, from a practical standpoint, C and D are connected per MIL-STD-1310D for safety and other reasons.

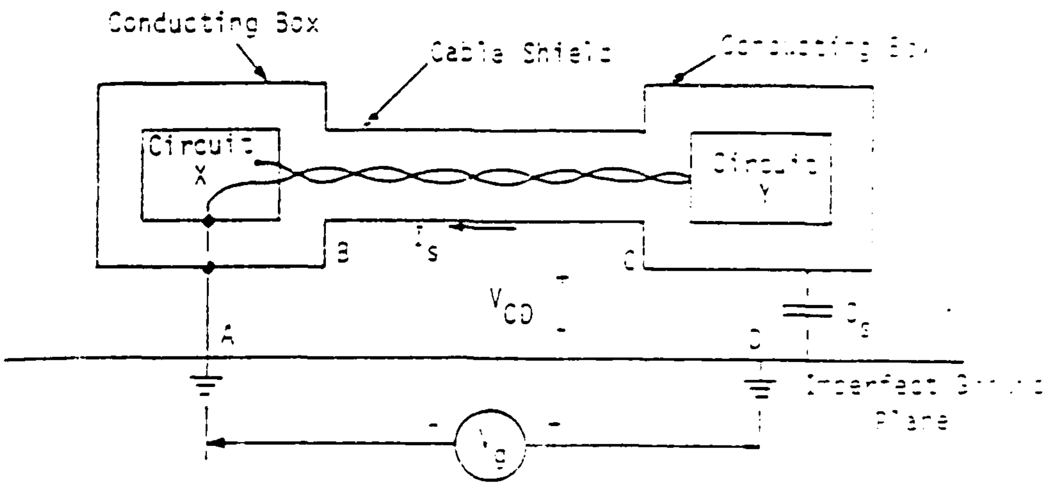


Figure 9.7. Singly Shielded Example

Figure 9.8 shows a double-shielded configuration in which circuits X and Y and the twisted pair are now within a double shield. Note that circuit Y and the inner shield are not connected to each other or to the outer shield. Again, from an EMP point of view, it is desirable to not connect C and D together, but practical considerations will force C and D to be connected. Points E and C are not connected, because this would tend to increase the current flow in the inner shield, and thereby increase the leakage through the shield.

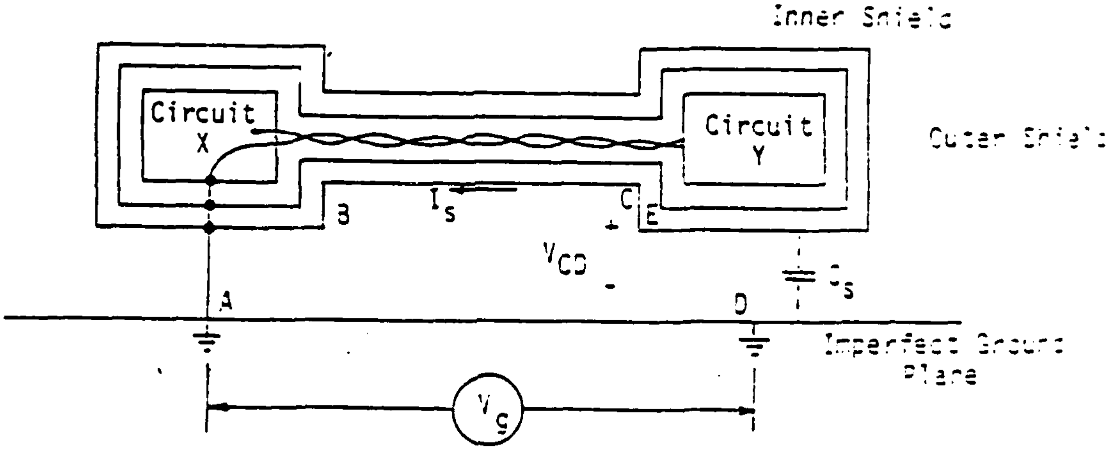


Figure 9.8. Double-Shielded Example

In Figure 9.9, circuits X and Y are grounded to the local hull ground at their respective locations because of other design constraints. The cable shield must be circumferentially bonded at points E and C. If the cable shield is left open as shown, large voltages can be induced on the system. The configuration shown is not recommended.

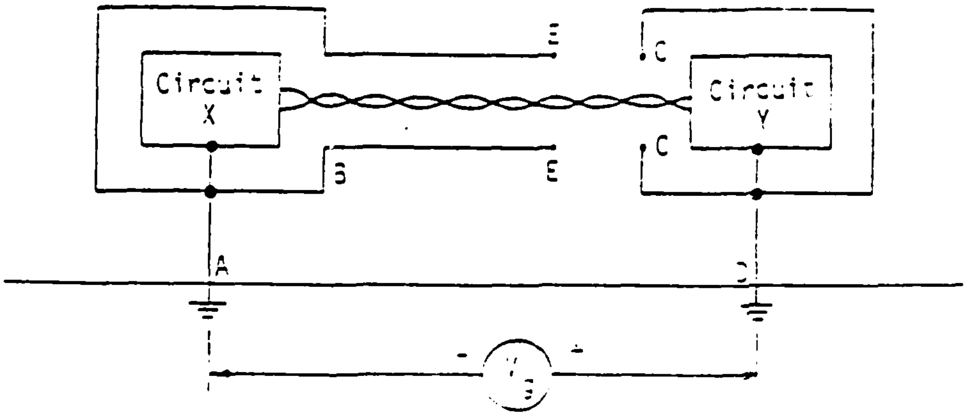


Figure 9.9 Single Shielded, Double Point Ground Example

The voltage induced on the twisted pair is in the common mode and is reduced by the common mode rejection ratio of the electronics in circuit Y if stray capacitance effects at the electronics input do not unbalance the twisted pair.

The application of the unipoint ground system is illustrated on a system-wide basis by means of the radial or "tree" configurations shown in Figure 9.10 [9.2]. In either case, there are no loops susceptible to magnetic field coupling, and currents flowing in the metal ship structure cause no ground differential voltages to exist. Each line in Figure 9.10 represents all electrical wiring, including grounds, shields, signals, and power. Signals and power lines and their returns should be in shielded twisted pairs to reduce magnetic field pickup. If any of the equipment is grounded to the metal ship structure, a loop which will destroy grounding integrity is formed.

The "tree" system has the disadvantage of mutual impedance coupling. For example, the impedance of line DC is an impedance in common with electronics box BB and AA, and currents flowing in line DC change the potential of boxes AA and BB, but not that of CC. Thus some boxes are at different ground potentials. The radial system does not have the mutual impedance coupling problem.

Both configurations of Figure 9.10 experience problems when the cable length becomes longer than 1/8 wavelength of the highest significant EMP frequency. A realistic upper frequency limit is about 100 MHz whose wavelength is 3 meters. One eighth wavelength is then about 37 cm. One solution of this problem is to reduce the high frequency content of the signal by using the double shielding concept illustrated in Figure 9.8. The outer shield is an extended Faraday cage whose transfer impedance decreases with frequency.

9.2.2 Interior Equipment Grounding Practices

For EMP considerations it has been found that the type of grounding practices used within shielded equipment racks and within the individual components which are in the equipment rack is not critical. Either multipoint or single point configurations can be used. If the component cabinets on equipment racks are much larger than standard rack size, or are not shielded, then special precautions based on the previously discussed principles (Section 9.2.1) must be taken.

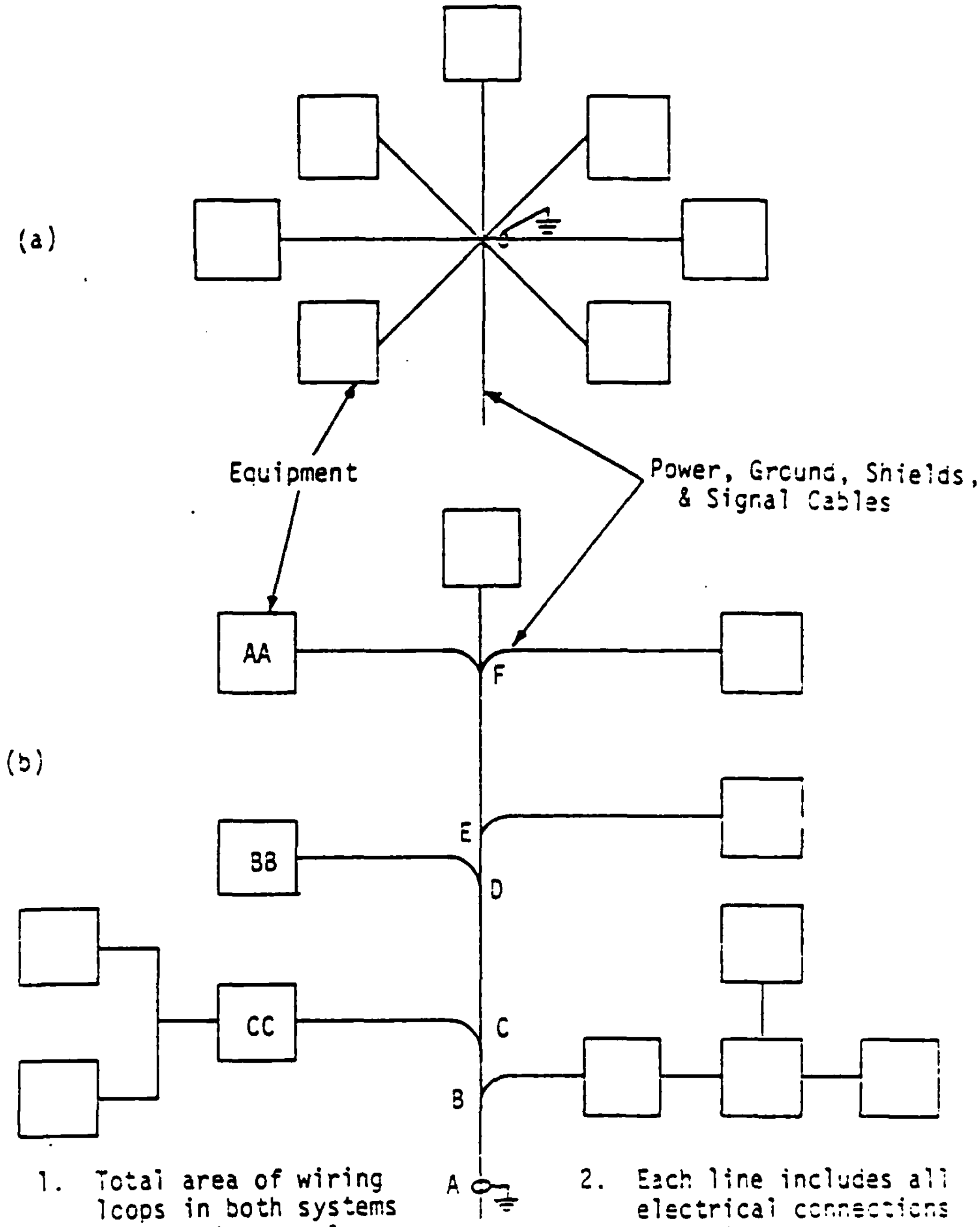
9.2.3 Power Cable Entry

Figure 9.11 illustrates typical power line entry into an equipment rack or cabinet. It is noted that the TPDs are located within a shielded entry compartment. The ground wire (for AC lines) and the return wire (for DC lines) are grounded with this compartment.

9.2.4 Signal Entry

The design practice for signal cable entry is illustrated in Figure 9.12, and is similar in concept to that for power entry. A shielded compartment houses the TPDs. The shielded cable is circumferentially bonded to the RFI connector such that a continuous Faraday cage is maintained.

For signal entry via waveguide, the waveguide must be peripherally bonded to the equipment housing as illustrated in Figure 9.13.



NOTE: 1. Total area of wiring loops in both systems is zero in any plane.

2. Each line includes all electrical connections to equipment.

Figure 9.10 Wiring to Reduce EMP Susceptibility (a) Radial, (b) "TREE" Wiring System [9.2]

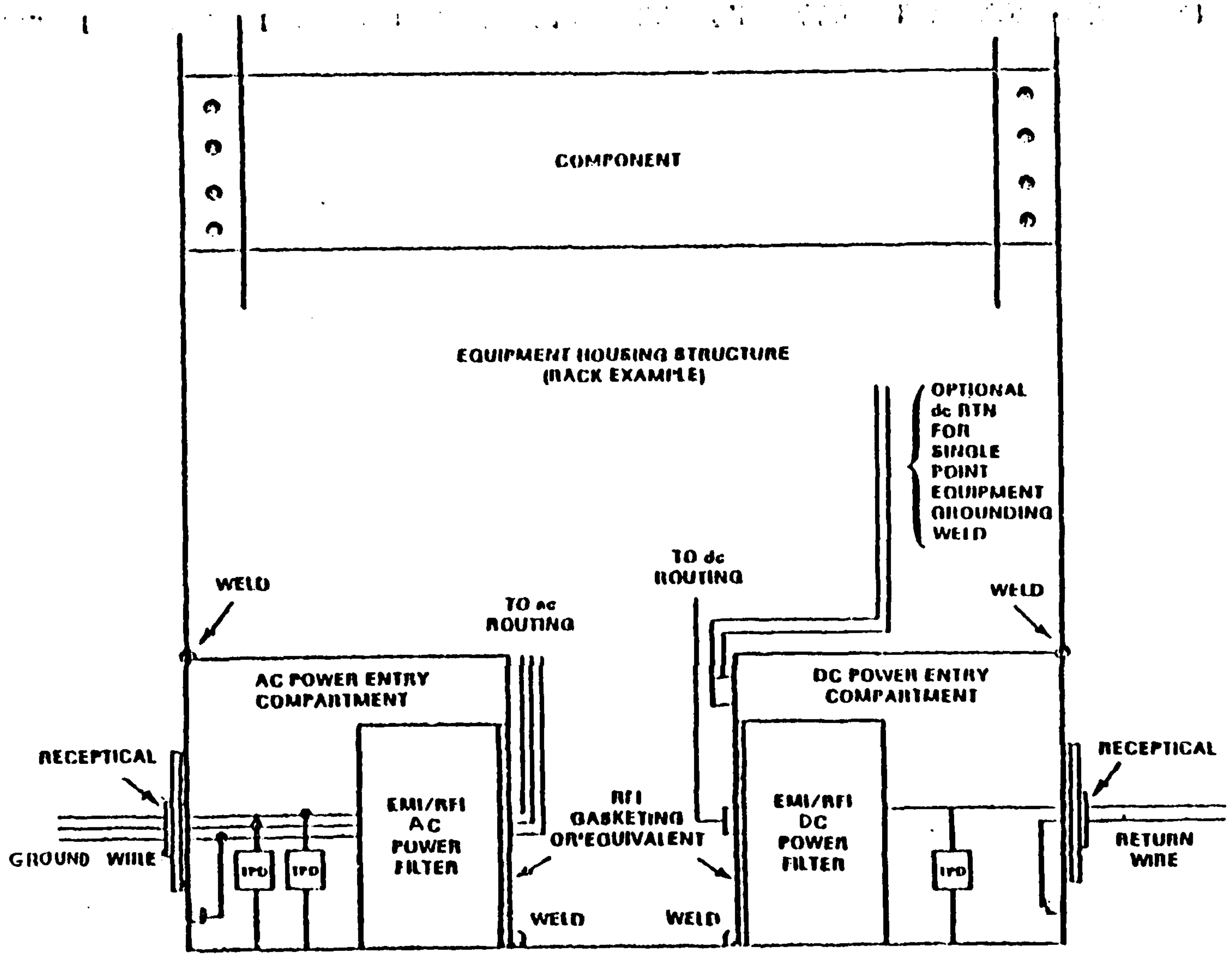


Figure 9.11 Example of typical ac and dc power entry to an equipment housing. Internal routing of cables and positioning of compartments given as an example. The design should employ good isolation and routing techniques to prevent coupling from ac and dc power leads to each other and to other equipment internal cables [9.3]

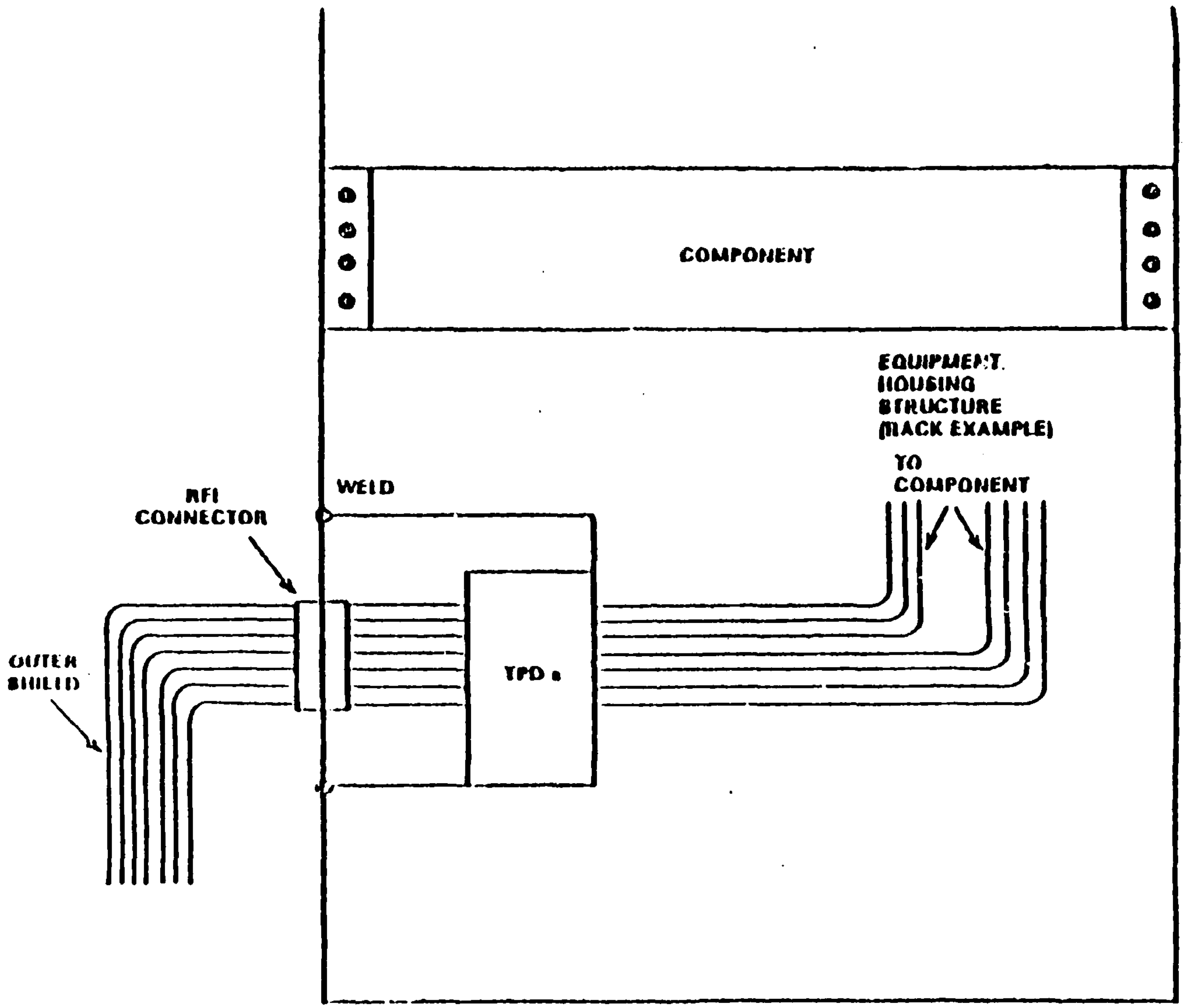


Figure 9.12 Example of signal and control entry to an equipment housing (rack example). Terminal protection treatment of the individual wires and shielded pairs are discussed in Section 6.3.8 [9.3]

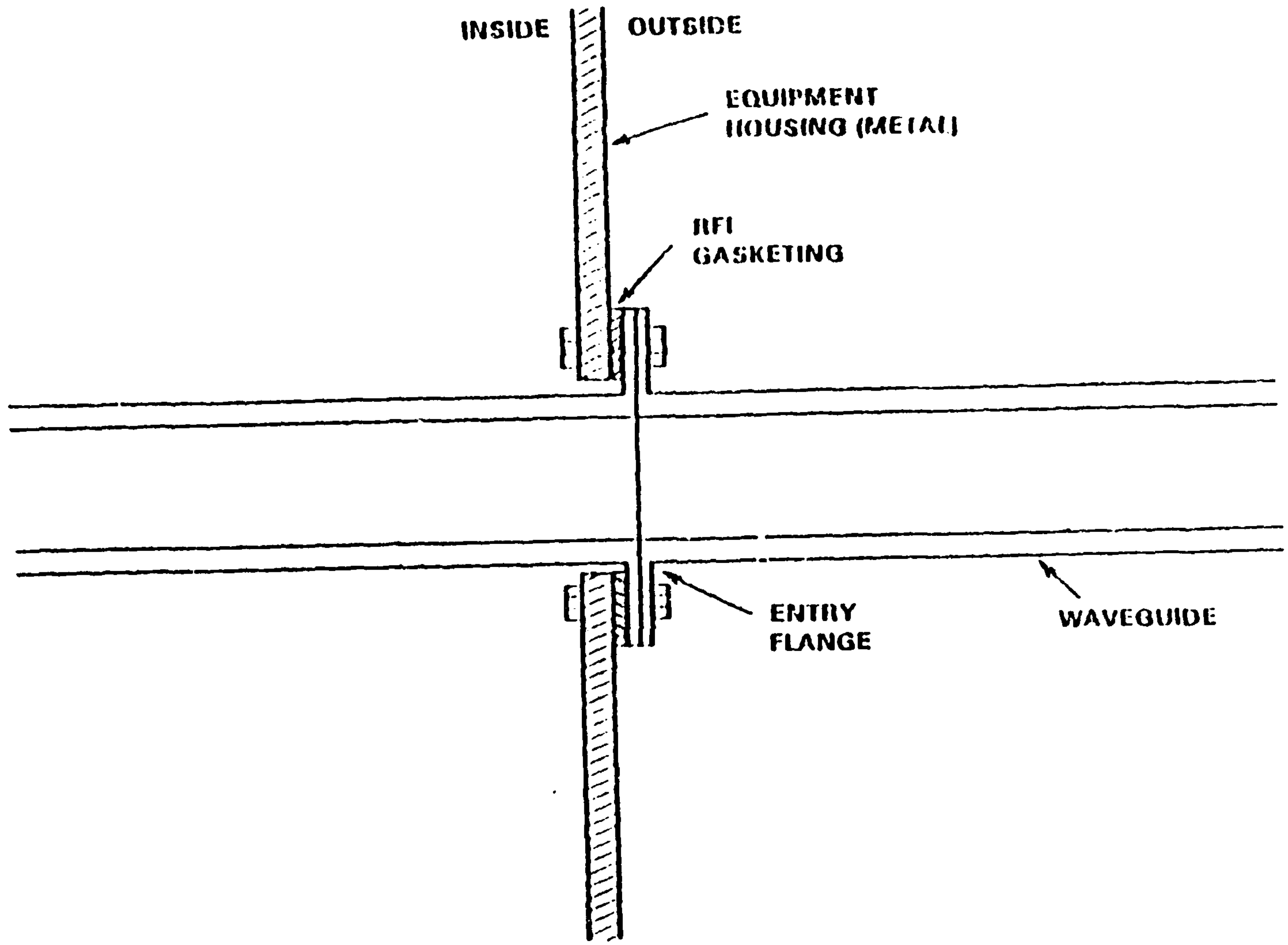


Figure 9.13 Waveguide Entry Flange [9.3]

9.3 Bonding

9.3.1 Background

Bonding is the electrical connection of metal parts. The electrical impedance between the parts must be at a low level to prevent arcing at the bond which could cause large voltage sources on cables (cf. Section 4.1).

Figure 9.14 illustrates the effect of a poor bond upon a filter which is designed to suppress an interfering signal [9.2]. If the contact resistance were zero, interference current would flow to the ground point. But, because the bond has a relatively high impedance, less interfering current is directed from the susceptible equipment.

Bonding can be classified as direct and indirect bonding. Direct bonding is direct contact of the two metal parts to be bonded. Indirect bonding is the connection of two metal parts by means of a third intermediate conductor such as a strap, gasket, or some other conductor. Although direct bonding is preferred, it cannot be done when the two metal parts are located some distance from each other.

Bonding guidelines for installation of equipment on ships are described in MIL-STD-1310D [9.1]. In this handbook, bonding principles which apply to equipment are presented.

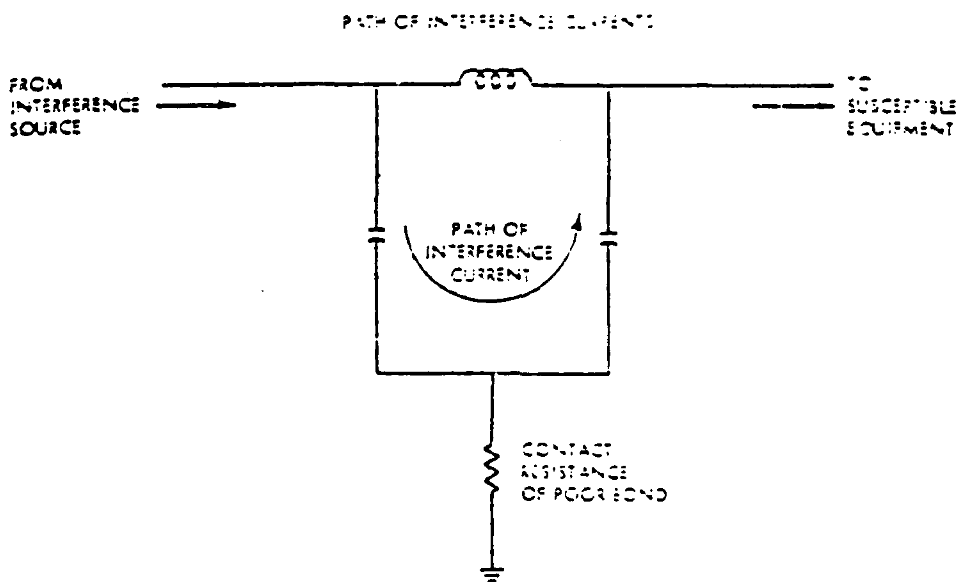


Figure 9.14 Effect of Poor Bonding on Filter Performance [9.2]

9.3.2 Direct Bonding

9.3.2.1 Bond Impedance

The effectiveness of a bond is determined by measuring its impedance. For example, MIL-B-5087B specifies that a bond should exhibit no more than 2.5 mΩ DC impedance between bonded elements. This DC impedance tells very little about the high frequency characteristics of the bond. For example, Reference 9.7 clearly illustrates this point (see Figure 9.15). Even for a laboratory test bond, the dc resistance has little to do with the high frequency impedance.

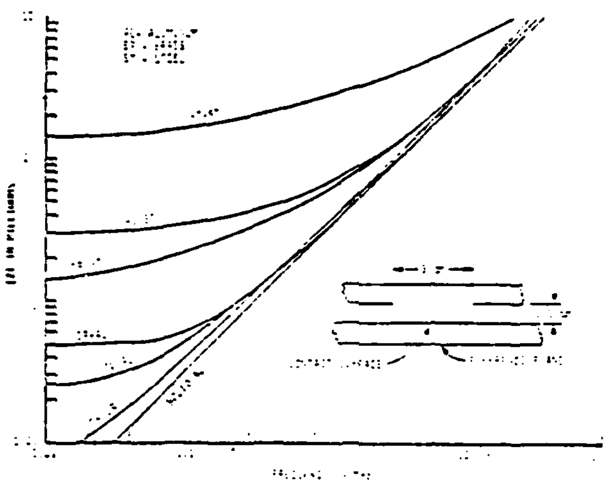


Figure 9.15 Frequency Variation of Bonding Impedance Between Several Materials [9.4]

9.3.2.2 Joining Methods

Direct bonds can be made by welding, riveting, bolting, brazing, or sweating for permanent contact, or by clamps and lock thread devices for surfaces that must be separated periodically.

9.3.2.3 Effects of Corrosion on Bonding

The following discussion is based on Reference 9.5.

The direct contact of two dissimilar metals in the presence of moisture will lead to corrosion at the interface. Either galvanic or anodic corrosion can occur. Galvanic reaction, which is the exchange of ions in a solution, occurs when the two metals have different electromotive potentials. Anodic reaction, also called electroplating, is the result of current flow through the moist contact area. If galvanic corrosion is prevented, anodic corrosion will usually be prevented also.

Table 9.1 lists the electrochemical series for some selected metals; a more complete listing is given in MIL-STD-889. The metal connected to the farther

Table 9.1 Electrochemical Series for Selected Metals [9.3]

1. Magnesium	12. Nickel
2. Magnesium alloys	13. Brass
3. Zinc	14. Copper
4. Aluminum 25	15. Bronze
5. Cadmium	16. Copper-nickel alloys
6. Steel or Iron	17. Monel
7. Cast Iron	18. Silver solder
8. 18-8 Stainless Steel	19. Silver
9. Lead-tin solders	20. Graphite
10. Lead	21. Gold
11. Tin	22. Platinum

down in the listing will corrode in a moist environment, but contact between adjacent metals in the table is considered compatible.

If two metals that are widely separated in the table must be bonded, a third metal, intermediate in the table, must be inserted between, either by plating or by inserting a thin piece of the third metal. Also, if circumstances permit, a replacable washer made from the more positive of the two metals may be inserted.

Table 9.2 gives acceptable bonding methods and material combinations for dissimilar metals that are bonded together [9.2]

If two dissimilar metals are bonded, the one higher up in Table 9.1 will corrode. The anode (the more positive metal) should, therefore, have a greater exposed surface area than the cathode. Figures 9.16 and 9.17 illustrate two means of minimizing corrosion in a bond area. In the first method, the cathode size is minimized and in the second, the exposed area is reduced by applying a protective coating to the cathode surface or to both surfaces.

9.3.2.4 Surface Cleaning

Most metals, if left exposed, form a surface oxide. This must be removed before bonding. Aluminum, magnesium, stainless steels, copper, nickel, silver, and brass are examples. The following procedures will adequately prepare these surfaces for bonding:

Table 9.2 Acceptable Bonding Methods and Material Combinations [9.2]

METALLIC STRUCTURE	ALUMINUM BONDING JUMPER	TINNED COPPER BONDING JUMPER
Magnesium and alloys	Direct or magnesium washers[b]	Aluminum or magnesium washer[a]
Zinc, cadmium, aluminum, and aluminum alloys	Direct[a]	Aluminum washer[a]
Steel (except stainless)	Direct[a]	Direct[a]
Tin, lead, and tin-lead solders	Direct[a]	Direct[b]
Copper and copper base alloys	Tinned or cadmium-plated washers[b]	Direct[b]
Nickel and nickel base alloys	Tinned or cadmium-plated washers[b]	Direct[b]
Stainless steel	Tinned or cadmium-plated washers[b]	Direct[b]
Silver, gold, and precious metals	Tinned or cadmium-plated washers[b]	Direct[b]

[a] Indicates Type I screw which is cadmium, zinc plated, or aluminum.
[b] Indicates Type II screw which is stainless steel or Type I

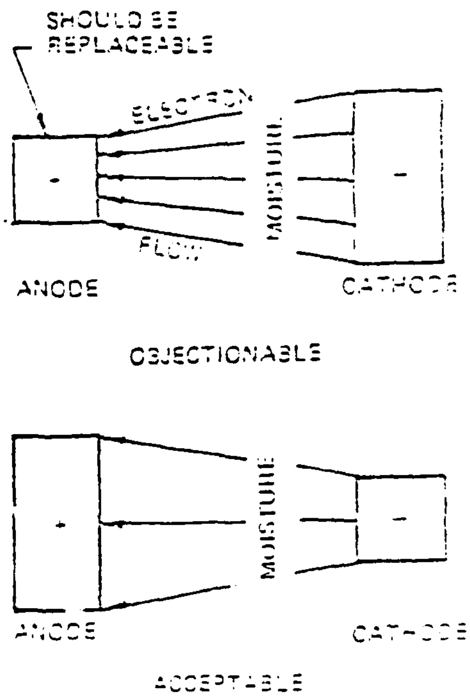


Figure 9.16 Relative Anode Cathode Area [9.6]

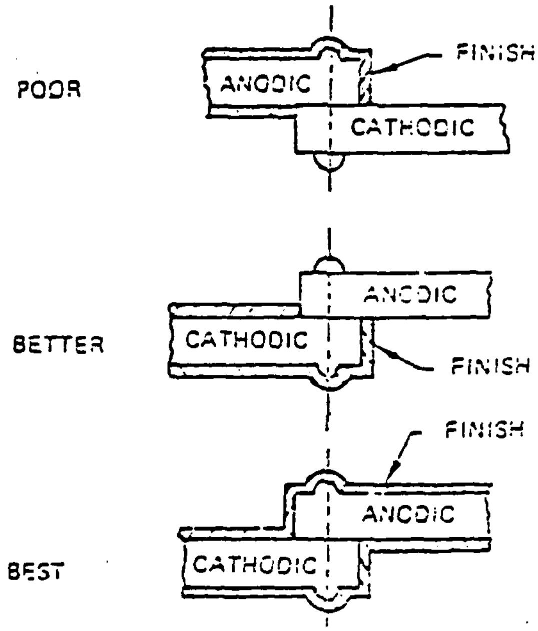


Figure 9.17 Finishing Around Dissimilar Metal Bonding Joints [9.5]

1. *For aluminum and aluminum alloys, MIL-S-5002 and MIL-C-5541*
2. For magnesium, MIL-M-3171
3. For copper, nickel, silver, brass, bronze, clean by degreasing and slightly etching the surface.

Grease or oil can be removed by vapor degreasing, ultrasonic cleaning, organic solvent (such as trichloroethane, triochloroethylene, or perchloroethylene) or emulsion cleaning which employs a mineral oil distillate and an emulsifying agent. The metal surface can be etched in a bath or chromic acid dry (CrO_3), 2 lb/gal, and sulfuric acid, 4 oz/gal. Average dip time is between 2 and 30 sec. Prolonged exposure of parts in this bath may cause excessive etching. The metal surface must be immediately rinsed in cold running water and then in hot water to facilitate drying.

9.3.2.5 Protective Finishes

A protective finish on the bond is necessary to protect it in a salt fog or spray environment. Three basic methods insure protection of the bond:

(a) Plating with gold, silver, nickel, tin or other corrosion-resistant conductors.

(b) Applying chemical films such as alodine, oakite, or iridite.

(c) Coating the entire joint with a protective material.

Table 9.3 gives a comparison of chemical film versus plated nickel on aluminum, and Table 9.4 presents data on chemical films on other metals.

Table 9.3 Chemical Film Versus Plated Metal on Aluminum [9.5]

Property	Chemical Film	Plated Metal (Electroless Ni)
Cost-Relative	5%	100%
Galvanic Compat.	Excellent - causes no corrosion	Corrosion-inducing
Thread Contour	Same As Machined	Same, Until Chipped
Lubricity	Lubricant Needed	Lubricant Needed
Repairability	Swab Wide Areas	No Repair Method
Self-Healing	Scratches Are Self-Healing	Not Self-Healing
Abrasion-Resist.	Flows Under Pressure	Permanent Scars
Scratch-Resist.	Easily Scratched	Scratch Resistant (Not Repairable)
Hardness	Same as Aluminum	Hard, But Cracks Easily
Crack Propagation	No	Yes
Contamination-Producing	None	Metal Particles (Conductive)
Adhesion	Excellent, No Problems	Variable, and Not Easily Tested
Thermal	Unchanged: 72 Hr at 150 F	Untested
Conductivity	Low	High

Table 9.4 Chemical Films on Other Metals - Initial Results [9.5]

Metal	Chemical Film	Init. Elect. Resist. (milli-ohms)	Corrosion Test Results	Final Electrical Resistance (milliohms)
AZ31B Magnesium	Dow No. 19	7.92	Salt spray - failed	High
	Dow No. 7	8.81	Salt spray - failed	High
	Dow No. 7	15.58	10-day humidity - pitted	High
	Dow No. 7 (honed surface)	0.13	10-day humidity - passed	10.80
	Alodine 600	18.60	10-day humidity - sl'y pitted	High
	Alodine 600 (honed surface)	2.55	10-day humidity - passed	2.23
Zinc Plate on AZ31B Magneisum	Kenvert 18	0.05	Salt spray - failed	High
	Kenvert 18	0.01	10-day humidity - passed	0.02
Cadmium Plate on AZ31B Magnesium	Kenvert 18	0.28	Salt spray - failed	High
	Kenvert 18	0.07	10-day humidity - pitted	0.14
Zinc Plate on Mild Steel	Kenvert 18	0.06	168-hour salt spray - passed	0.12
Cadmium Plate on Mild Steel	Kenvert 18	1.17	168-hour salt spray - passed	4.04
Copper	Kenvert 18	1.46	168-hour salt spray - darkened	High

9.3.3 Indirect Bonding

A method of computing the electrical characteristics of bond straps is outlined in Reference 9.6. A typical bondstrap is shown in Figure 9.13. The solid bar has DC resistance which is a function of its physical dimensions and of the resistivity of copper:

$$R_{dc} = \frac{\rho a}{A} \qquad 9.1$$

where

ρ = resistivity of copper (ohm-inch)

a = length of bar (inch)

A = cross-sectional area (inch^2).

The ac resistance of the strap is a function of frequency as well as of physical dimensions [9.7]:

$$R_{ac} = \frac{K\,663a\,\sqrt{f}\;0.10^{-9}}{2(w + t)} \qquad 9.2$$

where f is frequency in Hz and K is a function of the ratio w/t (Figure 9.14).

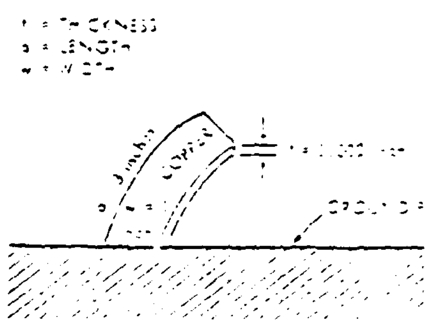


Figure 9.13 Typical Bond Strap [9.6]

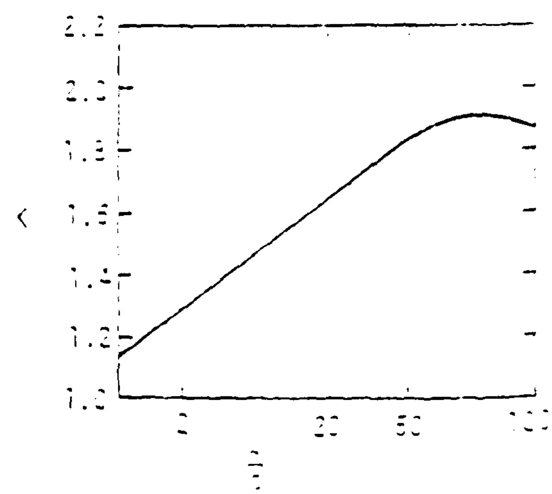


Figure 9.14 K-Factor [9.7]

Because in all cases the ac resistance is appreciably greater than the dc resistance, no meaningful correlation exists between the two. The bond strap equivalent circuit is shown in Figure 9.20.

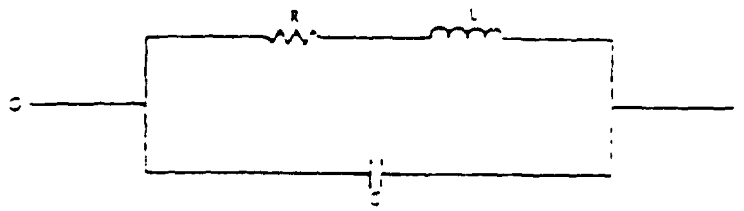


Figure 9.20 Equivalent Circuit of a Bond Strap [9.2]

In Figure 9.20 C is the distributed capacitance from the terminal T and points along the bar to the ground plane G. Therefore, the circuit in Figure 9.20 may be used as the bond-strap equivalent circuit. C may be roughly approximated by assuming that the bond forms a parallel plate capacitor with the ground plane:

$$C = 0.2244K \frac{a}{d} \ \mu\mu f \qquad (9.3)$$

where

A = area of the "plates" (inch^2)

d - spacing of the "plates" (inch).

The inductance of the bond is perhaps the most difficult to determine but is the most important factor over a good portion of the frequency band of interest. For low frequencies [9.7]

$$L = 0.00508\ a[2.303 \log_{10} \frac{2a}{w+t} + 0.5 + 0.2235 \frac{w+t}{a}] \qquad (9.4)$$

where a is in inches and L in in μh. For higher frequencies, L will be somewhat less.

The impedance of the strap may be expressed as

$$Z = \frac{R + j\omega\ [L\ (1 - \omega^2\ LC) - CR^2]}{(1 - \omega^2\ LC)^2 + \omega^2 C^2 R^2} \qquad (9.5)$$

or the magnitude of the impedance as

$$Z = \left[\frac{R^2 + \omega^2 L^2}{(1 - \omega^2 LC)^2 + \omega^2 C^2 R^2} \right] . \qquad (9.6)$$

Figure 9.21 shows the resonance property of the ground strap impedance, and Table 9.5 summarizes the bond strap parameter characteristics. The resonance property has been demonstrated experimentally in Reference 9.4. Figures 9.22 and 9.23 present measurements of the bonding effectiveness of two lengths of bond straps between a cabinet and a ground plane illuminated by rf. The distance between the ground plane and cabinet was varied for the measurements. The bonding effectiveness was obtained by measuring the voltage between the cabinet and the ground plane, with and without the bond strap. Positive values of bonding effectiveness indicate that the voltage was reduced when the strap was connected, and negative values indicate that the voltage actually increased with the bond strap connected. Bond straps can be detrimental to EMP hardening if the resonance is within a significant region of the power density spectrum of the EMP threat.

Experiments show that bond strap effectiveness decreases rapidly when the inductance increases beyond about .025 μh. Adding bond straps does not increase effectiveness. If a single bond is used, its location is important, for example, on receivers having unshielded antennas, the best location is at the corner nearest the antenna lead.

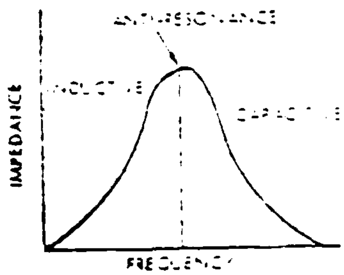


Figure 9.21 Impedance Plot of Bond Strap [9.2

Table 9.5 Bond Strap Parameter Summary Chart [9.6]

FOR AN INCREASE IN	dc RESISTANCE (R_{dc})	ac RESISTANCE (R_{ac})	INDUCTANCE (L)	CAPACITANCE (C)
LENGTH (a)	increases	increases	increases	—
WIDTH (w)	—	decreases as sum	decreases as sum[a]	—
THICKNESS (t)	—	decreases as sum	decreases as sum[a]	
AREA (A) = ($w \times t$)	decreases	—	—	increases
$\sqrt{\text{FREQUENCY}}$ ($\sqrt{f}$)	—	increases	—	—
BOND SPACING (d)[b]	—	—	—	decreases

NOTES:

[a] For small dimensions

[b] From ground

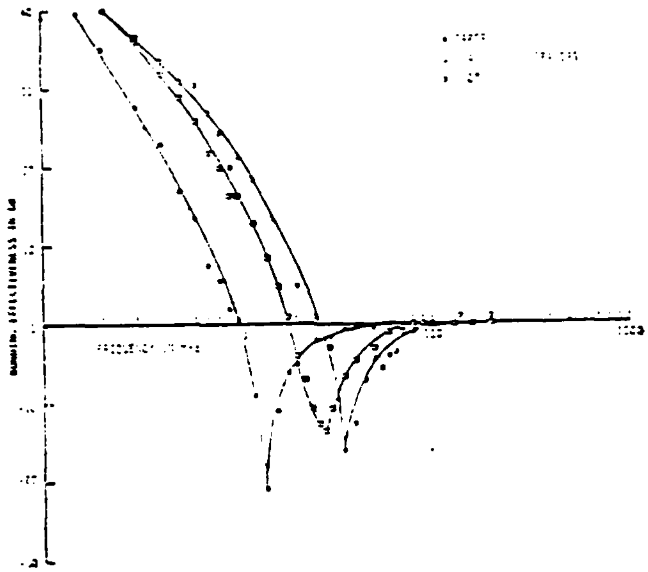


Figure 9.22 Bonding Effectiveness for a 9-1/2 inch Strap [9.4]

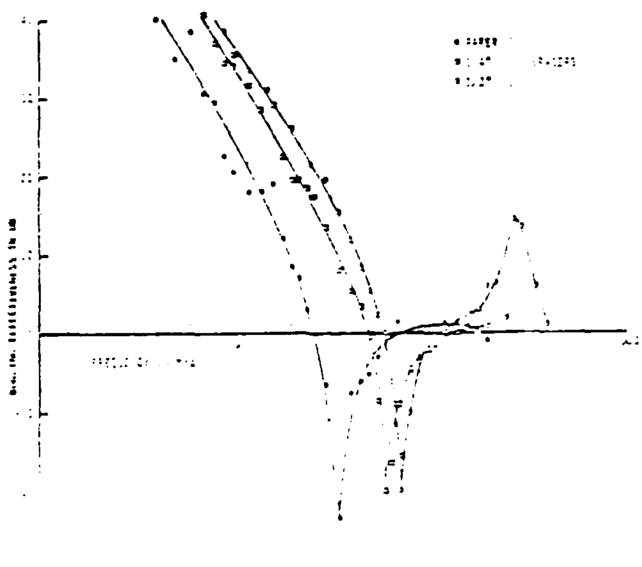


Figure 9.23 Bonding Effectiveness for a 2-3/8 inch Strap [9.4]

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9.3 Harry Diamond Laboratories, "DSN Design Practices for High Altitude Electromagnetic Pulse (HEMP) Protection", Draft A, 20 May 1980.

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CHAPTER 10

HARDNESS VALIDATION PROCEDURES

10.0 Executive Summary

There are basically two types of EMA tests which can be applied to equipment. The first type of test is a development test. One or more of these types of tests can be done during the design and development of the equipment to check certain parts of the equipment design. Certification tests are done on the complete equipment to verify hardness. In this chapter, both types of tests are discussed.

10.1 Background

One of the big problems associated with developing hardened systems is to determine if the system is hard. This process of determining system hardness is defined as hardness validation. In this handbook, hardness validation is divided into two distinct parts. The first part concerns developmental tests accomplished during system development which a manufacturer can do to ensure that his equipment will be hard when it is completely assembled. The second part concerns specific certification tests which will be imposed on the equipment after it is assembled.

The purpose of Section 10.2, "Development Tests", is to provide general guidance in the design of these tests. These tests are equipment dependant and the development of these tests is the responsibility of the manufacturer. The test procedures written for the development tests include cable shield integrity, shielding of seams and apertures, and interface testing. All development test plans shall be submitted to the Naval Contracting Officer for approval prior to the use of such tests for contract deliverable data.

Section 10.3, "Certification Tests", provides the criteria for the certification testing of electronic, electrical and electro mechanical equipment, and unless otherwise directed applies to all hardened and unhardened ship CLASSES. It is assumed that these tests will be accomplished at Naval facilities.

10.2 Development Tests

10.2.1 Current Injection On Cable Shields

The object of driving cable shields can be to produce a transient current in the shield and observe the response of the system, or else to measure the shield transfer impedance. The requirements placed on the current waveform often include specific wave shapes, rise times, and uniformity along the length of the shield. To control these properties of the shield current, it may be necessary to design wave shaping circuits and current return paths as well as an energy storage unit. The current return path is an important element of the coupling structure because it sets the size and uniformity of the impedance that must be driven by the energy source. Several coupling structures that may be used to obtain a known, uniform characteristic impedance between the cable shield and its current return are described below. Some of these schemes take advantage of the system or cable construction to minimize

the amount of additional hardware that must be installed, and some permit the pulse to be shaped by the natural impedances of the system structure. It should also be pointed out that while this section is concerned with shielded cables, the techniques discussed apply equally well to similar structures by any other name (e.g., armor, conduit, and pipeline).

10.2.1.1 Coaxial Transmission Line Configurations for Driving Cable Shields [10.1]

One of the simplest concepts for obtaining a uniform current density and characteristic impedance in a cable shield is to make the cable shield the center conductor of a coaxial transmission line as illustrated in Figure 10.1. With this configuration, the characteristic impedance of the transmission line formed by the cable shield, and its concentric current return path is:

$$Z_o = \frac{60}{(\epsilon_r)^{1/2}} \log \frac{r_o}{r_s} \qquad (10.1)$$

where r_o is the inside radius of the return path, r_s is the outside radius of the shield, and ϵ_r is the dielectric constant of the insulation between the shield and the return path. When the current rise time caused by the energy source inductance is neglected the current in the shield for a step-function voltage will be:

$$I(t) = \frac{V}{Z_o} e^{-t/CZ_o} \qquad (10.2)$$

where V is the initial voltage of the capacitor bank and C is its capacitance. The peak voltage between the shield and the cylindrical return path is the initial voltage of the capacitor bank. The spectrum of the current pulse is:

$$I(\omega) = \frac{CV}{1 + j\omega CZ_o} . \qquad (10.3)$$

The magnitude of the spectrum is CV, and the spectrum is flat with 3 dB from DC to $f = 1/2\pi CZ_o$. The bandwidth, spectral magnitude, and peak value of the driving current are related to the capacitance, characteristic impedance, and operating voltage as follows:

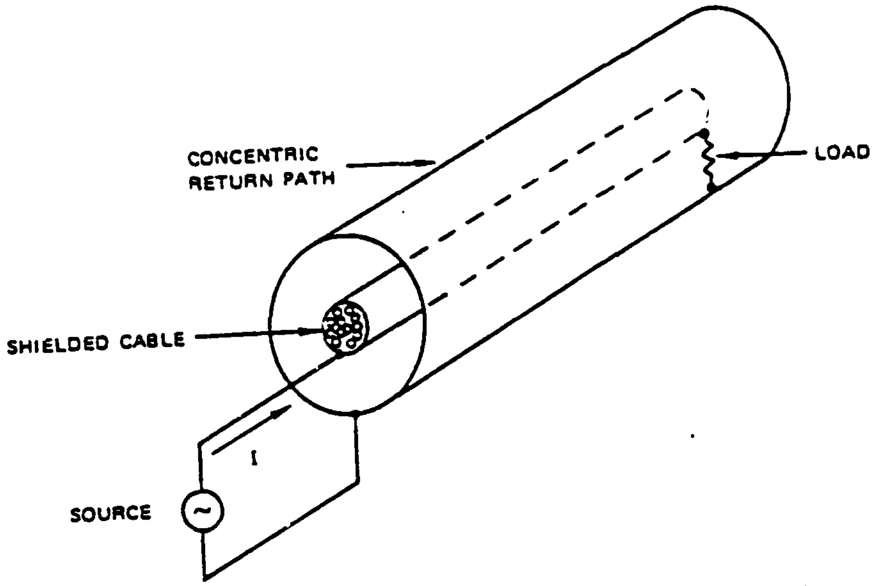


Figure 10.1 Concentric Cylinder Current Injection Coupling Structure in a Coaxial Transmission Line

$$\text{Bandwidth} = 1/2\pi CZ_o, \text{ in Hz}$$

$$\text{Spectral magnitude} = CV, \text{ in ampere-seconds} \qquad (10.4)$$

$$\text{Peak current} = V/Z_o, \text{ in amperes.}$$

The exponential current pulse obtained from the capacitor discharges into a terminated transmission line has the desirable characteristic that its spectrum is continuous - that is, it contains no dominant zeros or poles where the current spectrum is very small or very large. Although the flat bandwidth of the exponential pulse is $1/2\pi CZ_o$, its usable bandwidth is much greater because the spectrum is well behaved even when its magnitude is decreasing as $1/f$. The usable spectrum is determined by the rise time of the pulse which was assumed to be zero (10.2).

The capacitance, voltage, and characteristic impedance can be manipulated to obtain the desired spectral magnitude, peak current, or bandwidth as shown in (10.4) within the ranges permitted by available capacitors and voltage breakdown limits of the coaxial configuration. To maximize the peak current, for example, Z_o must be made small, which implies making r_o/r_s in (10.1) approach unity. This approach requires that the gap between the inner and outer conductors become small, however, and encroaches on the ability of the gap

to hold off the peak voltage V. The peak field strength E_s at the surface of the shield is:

$$E_s = \frac{V}{r_s \log \frac{r_o}{r_s}} \tag{10.5}$$

This field strength, which is critical to breakdown considerations, is the minimum for a given applied voltage V and outer conductor radius r_o when $r_o/r_s = e = 2.72$. In our case, however, we are more likely to have a fixed shield radius r_s, with freedom to choose the diameter of the return current path. With these conditions, the maximum peak current can be expressed as:

$$I_{max} = \frac{V}{Z_o} = \frac{r_s \log\left(\frac{r_o}{r_s}\right) E_{breakdown}}{\frac{60}{(\epsilon_r)^{1/2}} \log\left(\frac{r_o}{r_s}\right)} = \frac{(\epsilon_r)^{1/2} r_s \; E_{breakdown}}{60} \tag{10.6}$$

For air at atmospheric pressure $E_{breakdown} = 3 \times 10^6$ V/m and $\epsilon_r = 1$, I_{max} is:

$$I_{max} = 5 \times 10^4 \; r_s \tag{10.7}$$

Thus, the maximum current that can be developed is a terminated coaxial structure having a 2 inch diameter cable with atmospheric air dielectric is about 1 kA. By using oil dielectric, for which $\epsilon_r = 2.4$ and $E_{breakdown} = 1.5 \times 10^7$ V/m, the maximum current can be increased to about 8 kA. For polyethylene ($\epsilon_r = 2.4$, $E_{breakdown} = 4 \times 10^7$ V/m). the maximum current is about 20 kA. It should be noted that these are fundamental limits on the currents that can be injected on semi-infinite cables or cables terminated in their characteristic impedance. These currents can be achieved only when the driving terminals and termination structure are carefully designed to avoid concentrations of electric field that might reduce the breakdown voltage. It should also be point out that the transmission line geometry of concentric circular cylinders produces an electric field strength around the cable shield that is uniform in the azimuthal direction.

Any other configuration, such as parallel cylinders, produces a nonuniform, azimuthal distribution of field strength so that a transmission line of a given characteristic impedance formed with any other geometry will break down at a lower voltage than a line of that impedance formed by concentric circular cylinders. To achieve currents larger than those given above, therefore, the terminating impedance must be made smaller than the characteristic impedance. Reducing the terminating impedance produces a mismatch in the transmission line that results in a damped oscillatory current in the shield, however.

Coaxial cylinders can be formed from the two outer shields of a doubly-shielded cable to drive a current in the inner shield. This scheme, as illustrated in Figure 10.2 is efficient in terms of the pulse driver requirements because only the current in the inner shield must be simulated and this current is often much smaller than the total cable current induced by an incident EM wave. Whether or not this driving technique can be used depends on the characteristics of the shield system and the inner shield current waveform.

10.2.1.2 Parallel Wire Configurations for Driving Cable Shields [10.1]

In practice, the required bandwidth of the current pulse spectrum and the voltage limitations of the terminating resistor and capacitor bank require that the characteristic impedance be made as small as possible. The lowest characteristic impedances are available in coaxial transmission lines; however, it is difficult to construct such a line (except in those cases discussed above where the natural geometry of the system can be used), if the test cable is more than about a hundred feet long, particularly, if the outer shield of the test cable is not insulated for high voltages. In spite of its desirable electrical features (i.e., low characteristic impedance and uniform current distribution), this method of forming the transmission line has limited application because of the mechanical problems of drawing long cables through pipes and providing high-voltage insulation between the cable and the pipe.

An alternative to the coaxial line is the parallel-wire transmission line. The characteristic impedance of a parallel-wire line with unequal diameters as illustrated in Figure 10.3 is:

$$Z_o = \frac{120}{\left(\epsilon_r\right)^{1/2}} \cosh^{-1}\left(\frac{4D^2 - d_1^2 - d_2^2}{2\, d_1 d_2}\right) \qquad (10.8)$$

where D is the wire spacing, d_1 and d_2 are the wire diameters, and ϵ_r is the dielectric constant of the insulating medium. When allowance is made for high-voltage insulation, it is difficult with a single driving conductor to obtain characteristic impedances of less than 100 ohms. It is possible to reduce this impedance by nearly 50 percent, however, by using two conductors in parallel (as illustrated by the second conductor indicated by the dashed lines in Figure 10.3) to drive the test cable. This arrangement also produces a more uniform distribution of the current in the outer shield of the test cable and reduces magnetic coupling to the core of the cable.

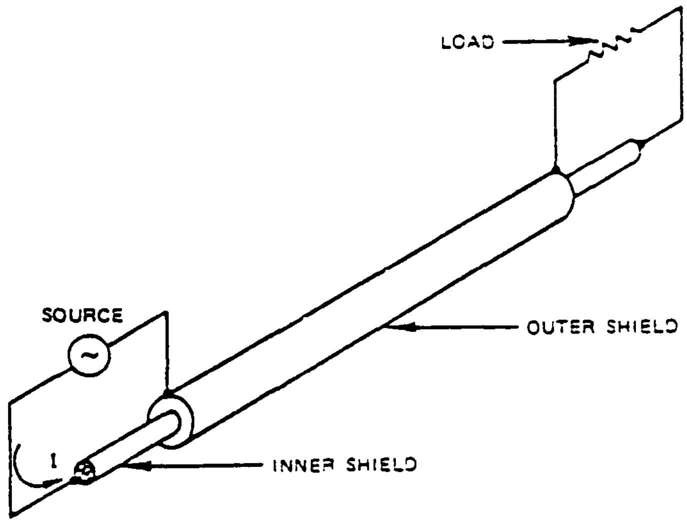


Figure 10.2 Shield as a Coupling Structure for Current Injection

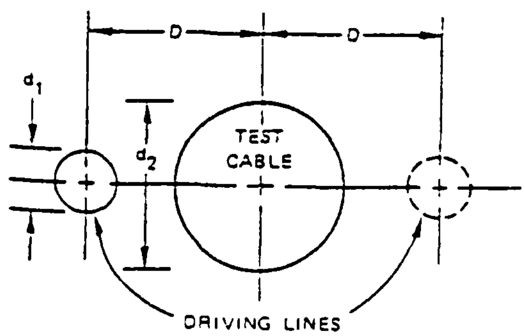


Figure 10.3 Parallel-Wire Transmission Line With Unequal Wire Diameters

it is fairly easy to construct a long, low-impedance uniform test line using the parallel-wire configuration as illustrated in Figure 10.4. High-voltage lines are used to drive the test cable, and the test cable is used as the low-voltage return for the parallel-wire line. If necessary, the cables can be insulated with wood or similar low-cost, low-voltage insulation to prevent arcing. Because the high voltage is confined to the well-insulated driving lines, this approach also has advantages in terms of the safety of the operating personnel.

The maximum current that can be produced in a semi-infinite parallel wire transmission line is even more severely limited than the current for a coaxial configuration because the electric field is concentrated between the driving lines and the cable shield. Both the characteristic impedance and the azimuthal uniformity of the field can be improved, however, by increasing the number of driving lines.

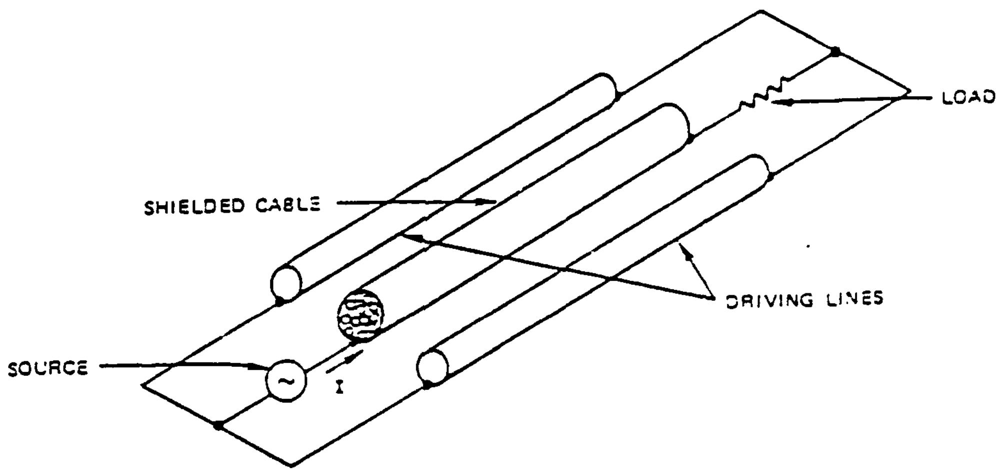


Figure 10.4 Parallel Driving Lines as a Coupling Structure for Current Injection

A variation of the parallel-wire driving structure is useful for driving shielded cables with insulating jackets that are routed along metal structure or laid in metal cable trays as illustrated in Figure 10.5. This configuration has the characteristics of a symmetrical two-wire transmission line, because the ground plane can be replaced by an image conductor to form a two-conductor line having twice the characteristic impedance of the conductor and ground plane. For the conductor of a diameter d, whose center is a height h above the ground plane, the characteristic impedance is:

$$Z_o = \frac{60}{\left(\epsilon_r\right)^{1/2}} \cosh^{-1}\left(\frac{2h}{d}\right). \qquad (10.9)$$

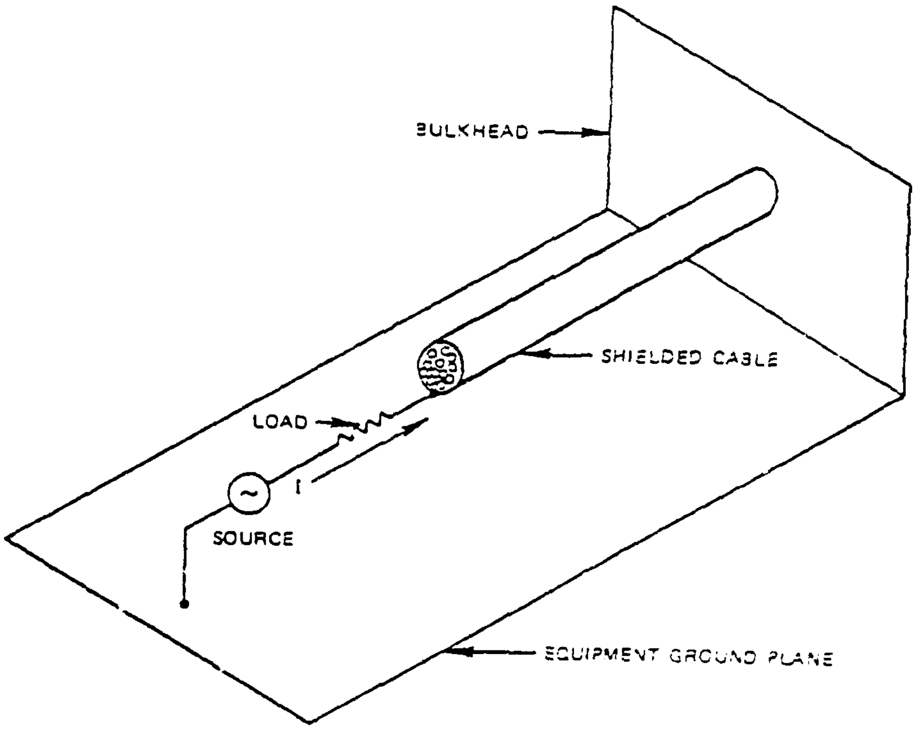


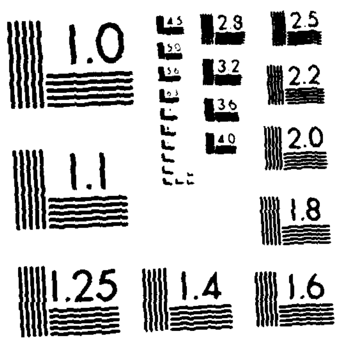
Figure 10.5 Equipment Ground as a Coupling Structure for Current Injection

This method of driving the shield is limited to applications where one end of the shield can be removed from the ground and connected to the energy source. In cases where simulation is required, it has the advantage that much of the pulse shaping is accomplished by the system structure, if the cable length and terminations are preserved.

If both ends of the cable are grounded to the structure in the system and it is desired to preserve this transmission line configuration so that the geometry of the system will shape the current waveform, then the current may be injected by means of a current transformer constructed as illustrated in Figure 10.6. The toroidal core can be split and clamped around the cable without disturbing the cable system. The equivalent circuit of an N turn primary and single-turn secondary current transformer referenced to the primary is illustrated in Figure 10.7, where L_1 and C_1 are the primary inductance and stray capacitance. R_c is the core loss resistance, L_c is the core leakage inductance, and L_2 and C_2 are the secondary inductance and stray capacitance, respectively. The core loss resistance is:

$$R_c = \frac{0.4\pi N^2 A}{\ell \times 10^8}\ \Omega$$


NC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

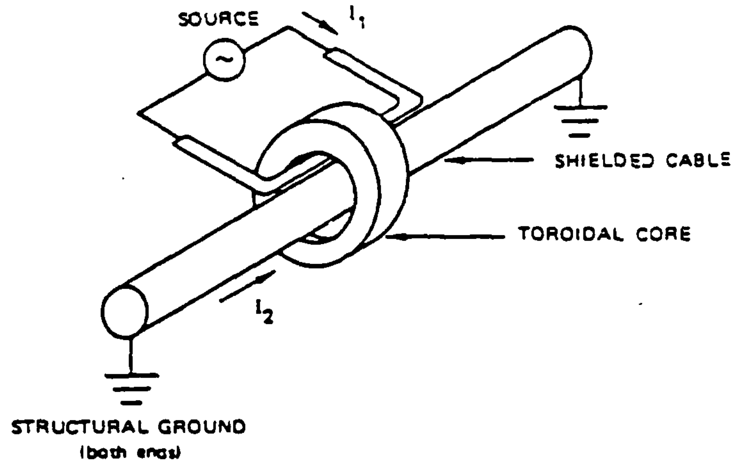


Figure 10.6 Current Transformer to Inject Current on a Grounded Cable Shield

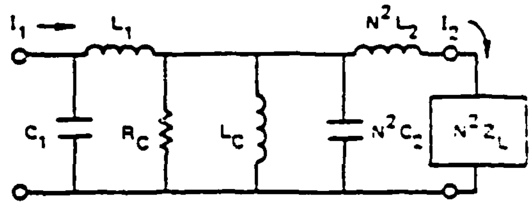


Figure 10.7 Equivalent Circuit of a Toroidal Core Current Transformer

where A is the cross section area in cm^2 of the toroidal core material, ℓ in cm is the mean magnetic path length in the toroidal core, and is the core material loss resistance factor. The core loss resistance factor is a function of frequency, core saturation induction, and heat dissipation in the core. The core leakage inductance is:

$$L_c = \frac{0.4\pi N^2 A}{\ell \times 10^8} \mu_c \qquad (10.11)$$

where μ_c is the pulse permeability of the toroidal material.

In a typical core current-injection application, the primary and secondary windings consist of one turn each so that L_1, L_2, and C_2 are all small compared to R_c and L_c which are characteristic of the toroidal core material. The Z_L

must be determined from the cable geometry and terminations. Frequently, the cable may be presented as a uniform transmission line (with a characteristic impedance Z_o) for at least a few ns. If the current transformer is installed in the middle of a cable 10 feet long, therefore, the initial load impedance will approximately be $2\ Z_o$ for about 10 ns, as is shown in the early time equivalent circuit in Figure 10.8. This equivalant circuit neglects the primary and secondary inductances and is valid for pulse rise times greater than a few nanoseconds. In practice, the loss resistance R_c is frequently smaller than the load impedance, and thus the current transfer efficiency is low (5 to 50% is typical). Loss resistance can be increased by using higher μ core material; but this approach suffers from the typically inverse relationship between μ and frequency and may adversely affect the rise time characteristics. Loss resistance can also be increased by increasing the cross-sectional area A while maintaining path length ℓ. This is readily accomplished by using multiple (or smaller) cores, and has only a second-order effect on the rise time due to the increase in L_1.

For late times, the load impedance will consist of lumped inductance, capacitance, and resistance parameters as is shown in the late time equivalent circuit in Figure 10.8. The late time current in the cable will have a response that is predominantly determined by the load characteristics. The core loss, R_c and L_c, determine the current efficiency as in the early time equivalent circuit and the loss inductance will slightly modify the cable response.

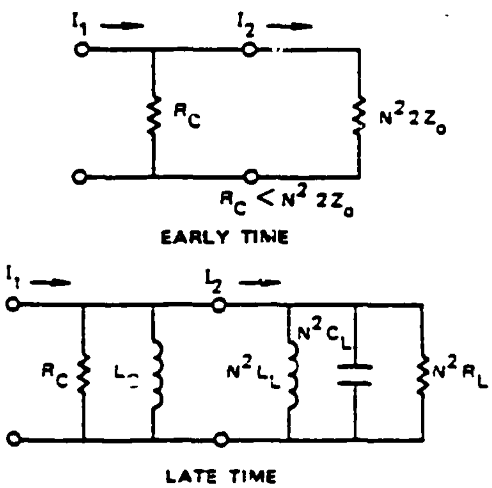


Figure 10.8 Early and Late Time-Equivalent Circuits

10.2.1.3 Natural and Unmatched Cable Terminations [10.1]

In most of the cases described above, it is implied that the transmission line used for injecting current into the cable shield should be terminated in its characteristics impedance to prevent the current from reflecting at the end of the driven structure. In the discussion of the technique illustrated in Figure 10.6, however, it was pointed out that the designer could take advantage of the natural structure to shape the injected pulse since this approach would greatly simplify the design of the driving pulse source required to simulate a free-field-induced current in the cable shield.

The use of unmatched terminations for the driving structure, particularly short-circuits, has other advantages that may contribute to the simplicity and economy of the direct-injection test. As was pointed out in (10.6), the maximum current that can be injected on a transmission line of a given size that is determined in a matched load is limited to a fairly moderate level by the dielectric strength of the insulation. However, if the transmission line is terminated in a short circuit and if the current rise time is considerably longer than the round-trip transit time between the driving source and the short-circuit, much larger currents can be produced without approaching dielectric breakdown voltages. Morover, high-current, short-circuit terminations are easy to produce and are inexpensive; high-current resistive loads are often expensive and usually must be designed with considerable skill to avoid high-voltage flashover problems without compromising high-frequency impedance characteristics.

Because of these advantages, short-circuit terminations are well suited to applications where large currents must be produced but where precise control of the current pulse shape is not critical - for example, for the injection of current on a long cable that has a solid tubular shield. Because the cable is long, the current that must be simulated may be large, but, because, it has a solid shield, only the low frequencies penetrate the shield so that only the low-frequency spectrum of the current pulse is of interest.

As an example of how to utilize the natural characteristics of the cable, consider a case such as that illustrated in Figure 10.2 in which the current is injected into the inner shield of a long, doubly-shielded cable and the outer shield is used as the current return path. The load between the shields at the end opposite the driving source is a short circuit. For this example, the energy source is a charged capacitor that is connected between the shields and discharged into the shield-to-shield transmission line. No deliberate shaping of the leading edge of the current pulse is used. The spectrum of the current pulse is:

$$I(\omega) = \frac{CV}{1 + j\omega CZ} \tag{10.12}$$

where Z is the input impedance of the shorted cable. For the shorted transmission line, the input impedance is:

$$Z = Z_o \tanh \gamma \ell \tag{10.13}$$

where Z_o is the characteristic impedance of the coaxial shield-to-shield line, γ is the propagation factor for the line, and ℓ is the line length between the input terminals and the short circuit.

10.2.1.4 Measuring Transfer Impedance and Transfer Admittance of Cables and Connectors

The triaxial tester is a common method of measuring the transfer characteristics of shielded cables or cable connectors. Figure 10.9 shows a typical test fixture. The test fixture should be much shorter in length than the wavelength

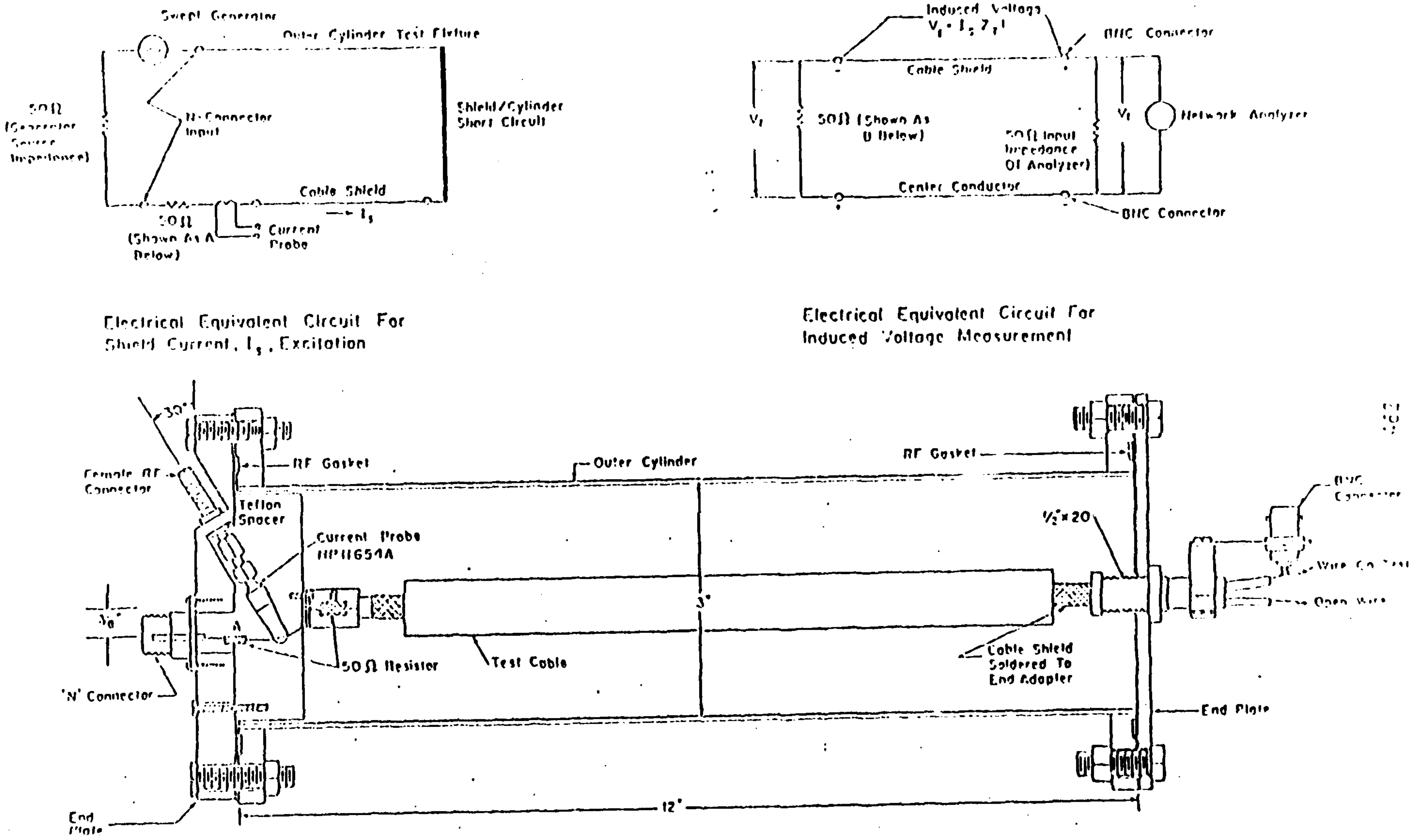


Figure 10.9 Test Fixture and Circuit Equivalents for Surface Transfer Impedance Measurements [10.4]

of interest to avoid standing wave generation. By attaching a text fixture to a swept CW generator, the transfer impedance or transfer admittance of the shielded cable or cable connector can be measured at each frequency.

The transfer impedance for shielded cables is

$$Z_T = V_I/(2I_s \ell) \tag{10.14}$$

where V_I is the induced voltage drop across one of two matched loads connecting the inner cable conductor(s) to the cable shield, I_s is the shield current, and ℓ is the length of the cable sample. The factor of two in (10.14) is due to the termination of the cable at both ends with a matched load. Figure 10.9 shows the equivalent circuits for the source excitation of the cable shield and induced excitation of the inner conductor(s). Note that in this particular figure a 50 Ω cable is tested, To determine the transfer impedance for connectors simply replace the cable sample with a connector. The cable used to measure the connector transfer impedance should be one with a total cable transfer impedance which is much lower than the measured transfer impedance of the connector with cable. The transfer impedance for the cable plus connector is

$$Z_T = V_I/(2I_s) \tag{10 15}$$

where V_I and I_s are defined in (10.14).

The transfer admittance can be obtained using the same test fixture as shown in Figure 10.9 where the conducting end plate is removed and the loads and sources are modified. Figure 10.10 shows a typical test fixture used for measuring the transfer admittance of cables or connectors. By driving the test fixture with a voltage source V_s and by measuring the current I_s on the inner conductor(s), the transfer admittance of the shielded cable is

$$Y_T = I_I/(V_s \ell) \tag{10.16}$$

where ℓ is the length of the cable sample. The transfer admittance of the cable connector is

$$Y_T = I_I/V_s \tag{10.17}$$

where I_I and V_s are defined in (10.16). Typically, the coupling through transfer admittance can be neglected.

10.2.2 Direct Injection on a Signal-Carrying Conductor [10.13]

The injection of the test signal into signal-carrying conductors, such as the core conductors of a shielded cable or the conductors of an unshielded cable, usually requires a more carefully designed experiment than the injection of test signals into cable shields. Most tests in which the cable shield is driven utilize loose coupling between the driving source and the signal-carrying conductors because the shield usually provides more than 20 dB of isolation. Because of this loose coupling, the system impedances that affect the responses of the signal-carrying conductors are not significantly affected by the driving system and the responses essentially occur from natural excitation of the cable shield. When the test is injected directly into the signal-carrying

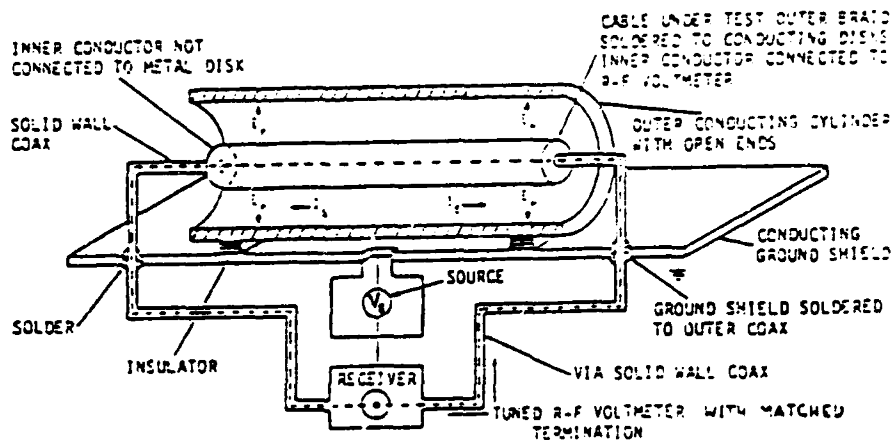


Figure 10.10 Surface Transfer Admittance Test Setup [10.5]

conductors, however, the driving source and coupling-system impedance may alter the system response. Thus, additional effort may be required to evaluate the effect of these differences - that is, to determine the system response had the effects of the injection system not been present or to place bounds on the possible effects of the injection system.

10.2.2.1 Injection of Common-Mode Voltages [10.1]

For the case where one end of a cable is accessible for injection of test signals, a common-mode test voltage can be directly injected at the end through an impedance matrix as illustrated in Figure 10.11. The impedance matrix may simulate the impedance usually connected between the conductors and between the conductors and the cable shield or system ground. In the case of a long cable, the voltage delivered to the conductors is:

$$V_{in} = \frac{Z_{in}}{Z + Z_{in}} V \qquad (10.18)$$

where V is the source voltage, Z_{in} is the input impedance of the cable with its normal load on the right-hand side (see Figure 10.11), and Z is the common mode characteristic impedance of the terminating resistors between the source and the cable. It should be noted that, if the right-hand end of the cable is also terminated in its characteristic impedance, only half of the source voltage is applied to the cable.

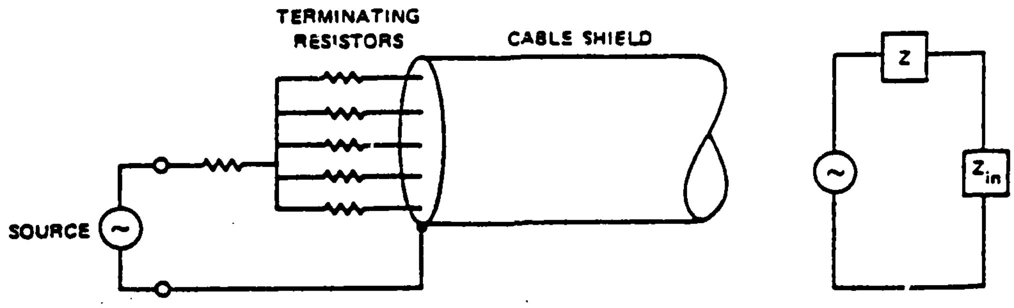


Figure 10.11 Impedance Matrix Used to Inject Common-Mode Voltages

This method of driving cable conductors is perhaps the most straightforward and commonly used of all the direct injection methods. It can also be used with unshielded cables that are routed along a metal structure or are placed in metal cable trays. With unshielded cables of this type, the current is driven against the metal structure or trays rather than against the shield. One disadvantage of this method is that the cable being driven must be disconnected at one end; hence, the system may not be operating in its normal state during the test.

When one end of the cable is not accessible, another injection method must be used. Such cases arise where disconnecting the cable precludes operating the system in its normal mode - for example, disconnecting the main power leads to inject a signal on these leads precludes operating the system from power supplied through the leads. In these cases, it may be necessary to accept some compromise in the quality of the simulation to perform tests economically. One approach that can be used under certain conditions is illustrated in Figure 10.12. At some suitable junction in the cable system, the energy source is capacitively coupled to the conductors and permitted to drive them with respect to the local ground or chassis. As illustrated in the figure, however, the current injected at this point is divided into two parts, one flowing in each direction from the injection point. Because this method of distributing the current differs radically from the current distribution that results from EMP excitation of the system, some care is required in designing a valid test using this approach.

The validity of a test using the injection method shown in Figure 10.12 depends on not significantly affecting system response by the attachment of the energy source or by injection of unwanted currents. To clarify the latter point, assume that the portion of the system to the right of the injection point in the figure is of primary interest in the test. Thus, for the test to be valid, the portion of the current that flows to the left from the injection point must not be reflected back into the right-hand circuitry during the period when the system is being observed to determine its response to the EMP. This condition implies that no significant reflections should return from the left end of the circuit, which in turn implies that this circuit be a very long (round-trip transit time that is longer than viewing time) or very short (round-trip transit time is shorter than any response of interest) or that it be terminated in a matched load (no reflections).

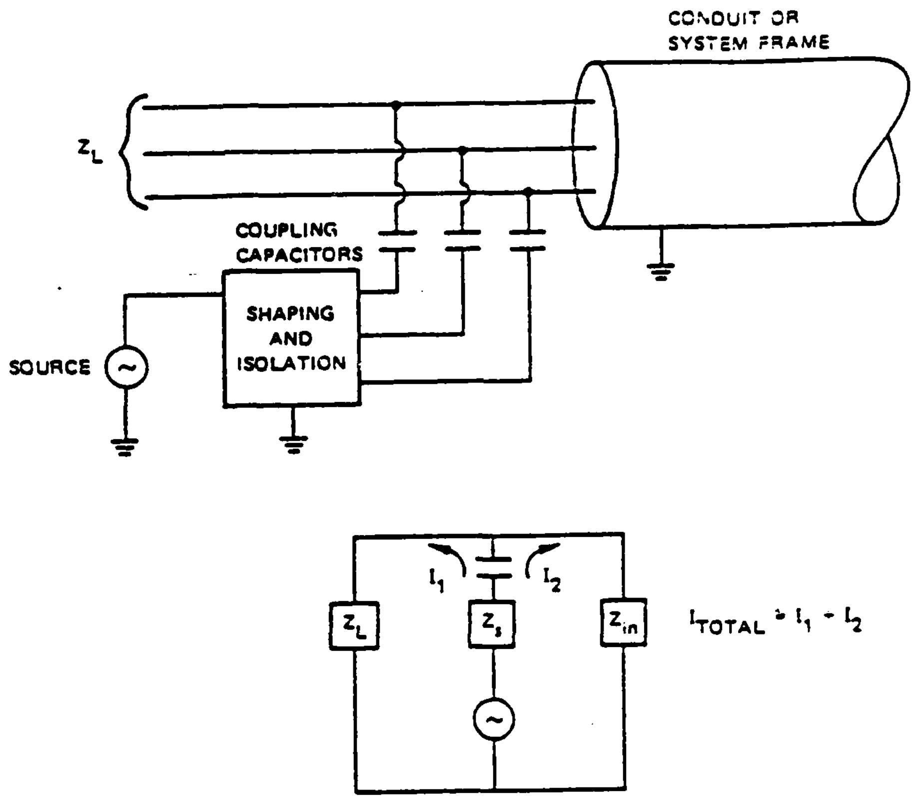


Figure 10.12 Capacitors Used to Inject Common-Mode Voltages

The stipulation that attachment of the energy source should not significantly affect the system response usually implies that the coupling between the direct injection source and the system conductors be loose so that the system impedances are not perturbed. It is important to observe that the loose coupling requirement applies to the differential-mode impedances as well as to the common-mode, or line-to-ground, impedances - that is, the attachment of the energy source should, in general, disturb neither the line-to-ground impedances nor the line-to-line impedances of the cable at the injection point. The loose-coupling requirement usually requires that the source voltage be much larger than the voltage that is to be injected, because most of the source voltage must be dissipated in the coupling network if loose coupling is to be achieved.

10.2.2.2 Common-Mode Voltage Driver

An example of a direct injection system is one in which a common-mode voltage is injected onto the conductors of an unshielded cable that connects an operating console with remote equipment cabinets. To drive the conductors in such a manner that the system response to the conductor-coupled signals is simulated, it is necessary to produce bulk currents similar to those induced by the EMP field, whether the cable is shielded or not. When the cable is not shielded, however, the problem of coupling a driving source to the cable is more difficult, because tight coupling to the cable may alter the cable response and invalidate the test. Conversely, loose coupling may not produce a large enough

cable excitation to be useful. The approach used here is to capacitively couple the signal to the unshielded cable by passing the cable conductors through a large conductive pipe that is excited by a capacitor discharge. This arrangement is illustrated in Figure 10.13.

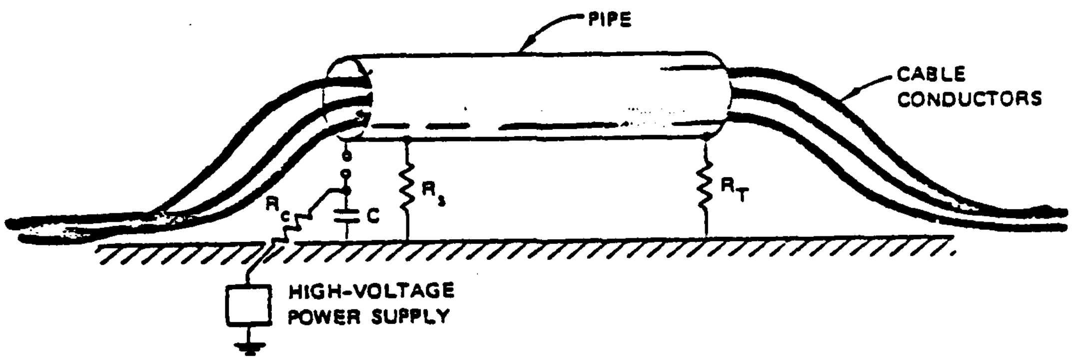


Figure 10.13 Cable Driver for Unshielded Cables

The conductor coupling capacitance is a polyvinyl chloride (PVC) pipe 10 feet long and 8-1/2 inches in diameter with a 3/8-inch wall thickness. A copper covering 8 ft long over the outside of the pipe forms one capacitor electrode, and the cable covering is terminated in corona rings, and the PVC pipe extends beyond the copper at each end to prevent arcing directly to the cables. The capacitor C is charged through a charging resistor R_C from a high-voltage dc power supply until the spark gap fires, connecting the storage capacitor C to the pipe and permitting it to discharge through the pulse-shaping resistor R_S. Because the 8 foot pipe over the ground plane behaves as a section of transmission line that will oscillate unless properly terminated, the resistor R_T at the end of the pipe opposite the driving capacitor is used to terminate the pipe. Also, if one wants to inject other waveforms, the driving source shown could be replaced with one that provides the desired waveshape.

10.2.3 Enclosure Shielding Effectiveness Tests

An enclosure may be formed from several different shielding materials of differing shielding characteristics. In addition, the overall SE for an enclosure will be compromised, to some extent, by the necessity for having certain points of entry (POE) into the enclosure as well as undesired leakage points at joints, apertures, access panels, etc. Verification tests are intended primarily to assess the SE obtained for an overall enclosure such as a shielded drawer, rack, bay, or system enclosure rather than to assess the intrinsic shielding of a particular material. Therefore, emphasis will be placed on tests of POE in an enclosure.

A set of measurement procedures to determine the shielding effectiveness of the enclosure EMP shielding elements will be presented here. The portion of shielding effectiveness which can be allocated to the continuous metal surfaces

of an enclosure will be termed the intrinsic SE. Although values for intrinsic SE may range to over 100 dB, the total SE of an enclosure is governed by the compromising discontinuities which can lower the SE to 20 dB or less.

It will be assumed that the intrinsic shielding effectiveness associated with any enclosure material can be adequately characterized through well known analytic formulation. The SE so determined represents the upper bound on the SE for a given shielding material.

A good way to measure the SE of enclosures is called the parallel plate method. This technique yields fairly uniform fields of low impedance, high impedance, or plane waves according to the termination of the parallel plate. Termination in a short circuit yields low impedance; termination in an open circuit gives high impedance; and termination in the characteristic impedance gives plane waves. This method has its greatest utility in testing relatively small enclosures.

The parallel plate test method provides a measure of enclosure shielding effectiveness from 3 kHz to 20 GHz [10.2].

Figure 10.14 illustrates a typical test setup for the parallel plate method. The detector is a small loop antenna with attenuator and receiver inside the enclosure [10.2].

The measurements shall be taken with the enclosure oriented in the following directions:

(a) Longitudinal axis parallel to axis of parallel plate.

(b) Longitudinal axis perpendicular to axis of parallel plate.

(c) Lateral axis of enclosure perpendicular to axis of parallel plate.

The shielding effectiveness for this method is defined as:

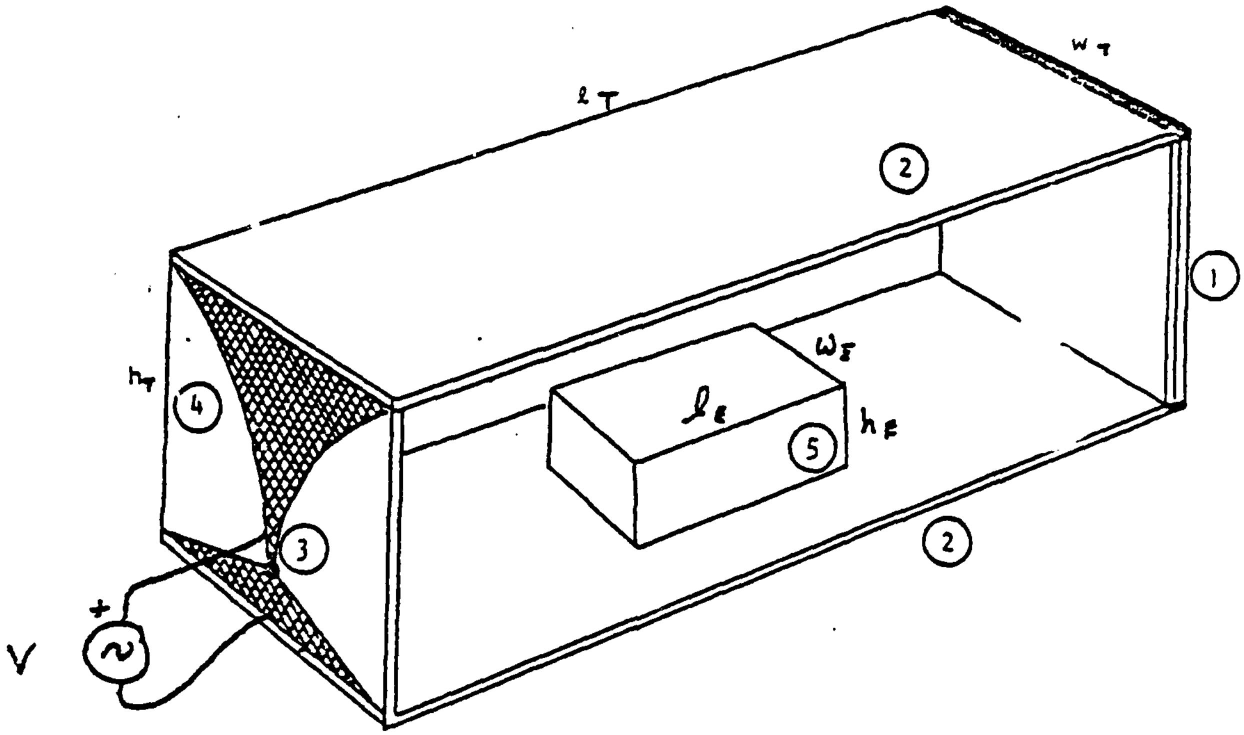
$$SE = 20 \log_{10} \left| \frac{E_1}{E_2} \right| \text{dB} \qquad (10.19)$$

where

E_1 = the field with no enclosure present.

E_2 = the field measured within the enclosure.

Care must be exercises that the relative dimensions of the enclosure under test and the parallel plate line conform to the restriction shown in Figure 10.14. There are many advantages of this technique. The field generated is relatively uniform within the bounds of the parallel plate region. Also, for large enclosure measurements, a practical parallel strip line may be constructed of a few (four or five) parallel wires placed along either side of the enclosure. In addition, the uniformity of the field over a wide frequency range is improved in comparison with other methods because of the smaller inherent capacitance associated with this setup. Finally, the parallel plate method is easily



1. TERMINATION - SEPARATED LAYERS OF 377 Ω/□ CONDUCTIVE PLASTIC FILM, JOINED AT ENDS AND CONNECTED TO CONDUCTIVE PLANES
2. CONDUCTIVE PLANES, ALUMINUM SLOTTED LONGITUDINALLY 1/2" OC
3. INPUT CONNECTOR, BNC OR N TYPE
4. WAVE LAUNCHER, 1/16" COPPER ON 1/2" PLEXIGLASS (~ LOG CURVE)
5. TEST ENCLOSURE

$$V = \frac{E(t)}{h}$$

Figure 10.14 Parallel Plate Line

adaptable for predominantly magnetic or electric fields, or for fields of free space impedance by short circuiting, open circuiting, or by termination in the characteristic impedance, respectively.

Disadvantages of this method are related primarily to the cumbersome size of the test setup for large enclosures. Another disadvantages of this method is that the setup yields high VSWRs at high frequency indicating a large departure from ideal E-field and H-field distributions [10.2].

Other pertinent considerations include limitations on the size of the enclosure tested relative to the dimensions of the parallel plate region. For example, the ratio of the height of the test sample to plate separation must be kept below certain limits in order to avoid large perturbations of the test fields. Also, the width of the test enclosure must be smaller than the parallel plate width in order that the field uniformity be maintained over the entire enclosure. Nominal values of test fixture dimensions as a function of the size of the enclosure being tested are as follows:

$$\begin{aligned} h_T &= 2\ h_E \\ l_T &= 4\ l_E \\ W_T &= 3\ W_T \end{aligned} \tag{10.20}$$

10.3 Certification Testing

10.3.1 Background

In Section 10.2, developmental tests which a manufacturer may wish to use are described. In Section 10.3, tests which certify EMP hardness are described. The EMP criterial environment which the equipment must survive were described in Section 2.4. The objective of certification testing is to ensure that the criteria is met. The certification testing program shall demonstrate the EMP survivability of the critical equipment being procured. The EMP test procedure is to inject a series of damped sinusoid pulses on the system's interconnecting cables. The magnitude of the test pulses shall be increased from a low level until either the specified current or voltage level is obtained. The tests shall be performed at least 10%, 50%, and 100% of the specified maximum amplitudes. As a minimum, EMP certification tests shall be performed at frequencies of 0.5, 1, 2, 5, 10, 20, and 50 MHz. Additional test frequencies determined in the functional analysis shall be included. The required number of test pulses depends on the number of independent test conditions and the specified survivability probability and associated confidence factor (Section 10.3.5).

10.3.2 Non-Antenna Interface Pin and Cable Transient Test [10.3]

10.3.2.1 Pretest Functional Analysis [10.3]

A functional analysis shall be performed before the certification testing to determine the following items:

(a) The interface cables and pins to be tested.

(b) The system functions which must be monitored to determine system failure or transient upset.

(c) The additional test frequencies (i.e. interface cable resonant frequency, clock frequencies, data rates, etc.).

10.3.2.2 Critical Equipment Configuration [10.3]

Non-antenna interface circuits shall be tested with the EMP transients presented in Section 2.4.3.2. The equipment shall be tested with the power on and with power off and in all applicable modes of operation with the test cables or specified interconnected cables terminated in actual or simulated loads. If the equipment being tested is designed to interface with GFE, then those interface cables shall be terminated in a suitable termination box which provides the necessary signal and data exchange. The EMP tests shall be performed with the equipment configured to represent a typical shipboard installation. The pretest functional analysis will have identified which function or functions to monitor for system failure. Failure is defined as the loss, degradation, or malfunction of any essential function of the equipment that would affect overall system performance and mission success or safety.

10.3.2.3 Test Procedure [10.3]

The EMP test transients shall be coupled onto the critical equipments interface cable (or wire for an interface pin test) by non-conductive coupling. The coupling method is shown in Figure 10.15 where an insulated cable from the injection source is colocated with the critical equipment interface cable to induce the specified EMP transients. The injection source used shall be capable of producing a damped sine wave transient at the specified test frequency with the specified damping ratio. In addition, the amplitude of the damped sine wave transient must be variable so the injected transient can be increased from a small value up to the maximum specified level.

The EMP test transient injected on the system's cable/wire shall be monitored to ensure that the specified test frequency and damping rate are obtained from the injection source and coupling cable. The amplitude and waveshape of the injected transient shall be monitored with a current sensor and voltage probe. The transient shall be recorded with a suitable oscilloscope for documentation of the EMP test.

10.3.3 Antenna Interface Pin Tests [10.3]

Critical equipment which contains antenna interface circuits shall be tested with the EMP transients presented in Section 2.4.3. Equipment that will be installed on both hardened and unhardened ships shall be tested with the unhardened equipment test criteria. The critical equipment shall be configured to represent an actual shipboard installation The equipment shall be operational and power applied. Radio receivers shall be operated and tested in all operational modes. Transmitter equipment shall be energized and operated with the rf power in a standby mode for the EMP test. A suitable pulse generator shall be used to develop the required voltage and current pulses for the EMP test. The pulse generator shall be capable of producing the selected test frequency with the specified damping factor of $Q = 16 \pm 4$ and have an internal

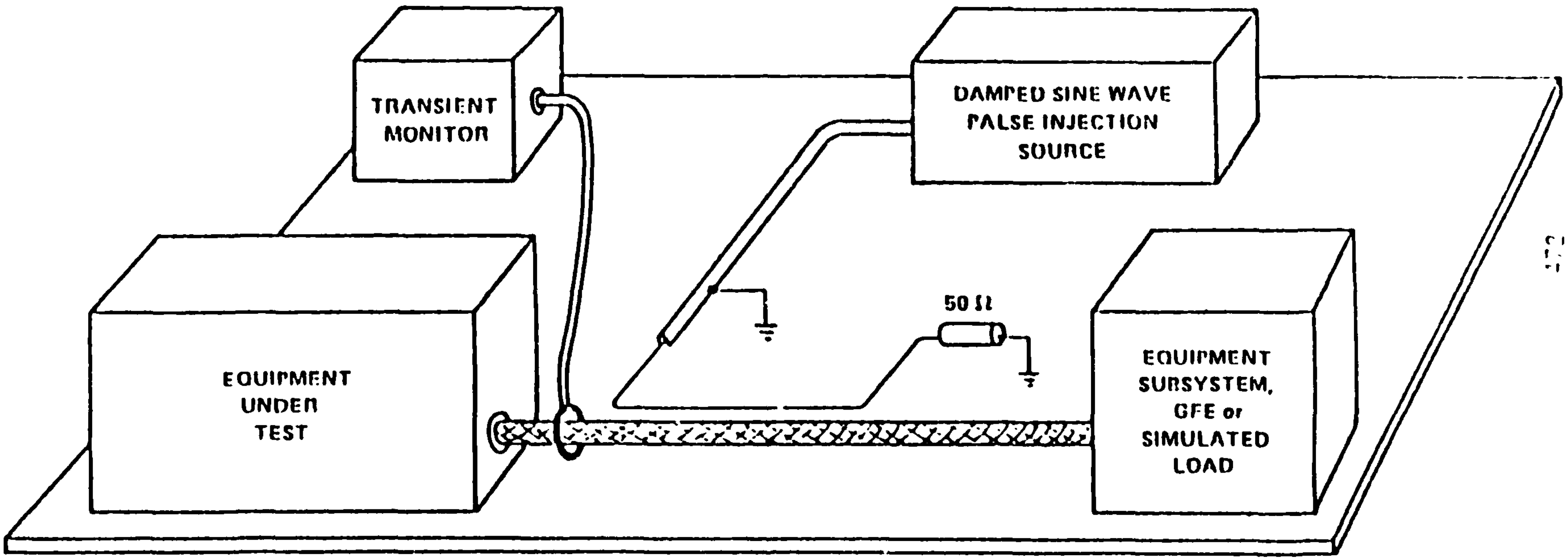


Figure 10.15 Interface Cable Injection Test Method

source impedance of 50 Ω. The EMP test frequencies shall include as a minimum 100 KHz, 700 KHz, 1 MHz, 2 MHz, 5 MHz, 10 MHz and 20 MHz. The HF tests shall be performed for each of the test frequencies plus the additional test shall be performed at the above frequencies plus the additional test frequencies of 50 MHz, 100 MHz, 225 MHz and 400 MHz. Additional test frequencies that are within the test spectrum presented in Figure 2.6 may be selected and included in the minimum set of frequencies. A minimum of 10 pulses shall be injected for each test configuration and frequency.

10.3.3.1 Unhardened Antenna Interface Pin Tests [10.3]

Critical equipment that contains unhardened antenna interface circuits shall be tested to the maximum transient levels specified in Section 2.4.3.3. The maximum test voltage for various test frequencies is presented in Figure 2.6 for HF and UHF/VHF equipment. The damped sinusoid pulse generator and the critical equipment shall be configured for the test as shown in Figure 10.16. The EMP test transient shall be monitored at the output of the pulse generator. For each test frequency, two cases of equipment configuration shall be tested. For the first case, the coax cable that connects from the output of the injection source to input of the critical equipment shall have a length that corresponds to the half wave resonance of the test frequency. For the second case, the coax cable shall have a length that corresponds to the quarter wave resonance of the test frequency.

10.3.3.2 Hardened Antenna Interface Pin Tests [10.3]

Critical HF radio equipment that is planned to interface with hardened HF antennas shall be tested with a damped sinusoid pulse generator that is modified as follows. The output of the pulse generator shall be connected to the actual antenna protection device that is planned for the antenna hardening. The cable length between the output terminals of the pulse generator and the antenna protection device shall be less than 0.1 meters. A diagram of the test equipment configuration is shown in Figure 10.16. The coax cable that is connected between the antenna protection device and the critical equipment under test shall have the following lengths. For Case 1 of the test, the coax cable shall have an electrical length that corresponds to the half wave resonance of the injected test frequency. For Case 2, the length of the coax cable shall correspond to the quarter wave resonance of the test frequency.

10.3.3.3. Hardened UHF/VHF Antenna Interface Pin Tests [10.3]

(To be determined).

10.3.4 Electromagnetic Field Transient Tests [10.3]

10.3.4.1 Critical Equipment Configuration

The critical equipment shall be configured to represent a typical shipboard installation. Equipment that will be located in the exterior or in the interior spaces of a ship shall be configured in an actual shipboard installation, installed in a suitable EMC test chamber or configured as shown in Figure 10.17.

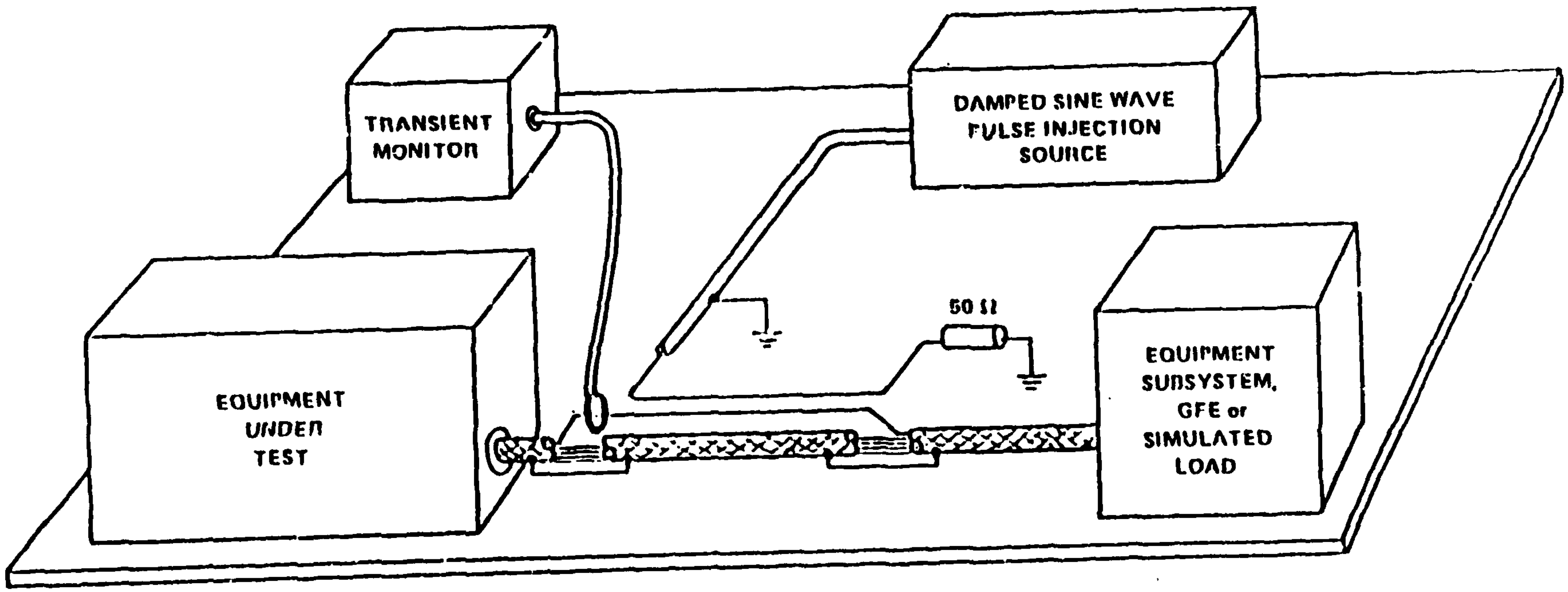


Figure 10.16 Interface Pin Injection Test Method

10.3.4.2 Electromagnetic Field Test Environment

Critical equipment that is planned to be installed in the interior spaces of a ship shall be tested with the local electromagnetic field transients. An injection source which is capable of producing a damped sinusoid wave form shall be used to drive the insulated center conductor of a coax cable that is located 1 meter away from the critical equipment. The maximum level of the current pulse that produces the electromagnetic field is given in Table 2.1 for various equipment locations. The planned shipboard location for the critical equipment shall be used to obtain the value of the maximum value of pulse current used to develop the electromagnetic field environment. (See Figure 10.17)

10.3.4.3 Test Procedures

The local electromagnetic fields used to test the critical equipment shall be generated by a suitable damped sinusoid pulse generator. The generator shall be capable of producing the maximum value of current required for the test frequencies. The pulse generator shall drive the insulated center conductor of a coax cable that is terminated in a 50 Ω resistor. A current probe shall be used to monitor the output of the pulse generator and ensure that the maximum value of current is obtained for each test frequency. The test frequencies determined in the system functional analysis shall be used to verify the critical equipment hardness to EMP.

10.3.5 Equipment Certification

The specifications in Section 2.4.2 require that the system (or equipment) must have greater than a 90% probability of survival with a confidence factor of at least 50% in order to be certified. Figures 10.18 and 10.19 show the number of successful tests required as a function of survival probability and confidence level. From Figure 10.18 or 10.19, it is seen that at least seven successful tests must be performed at threat level in order to be certified. For example, seven systems chosen randomly must pass 90% of each of the required certification tests.

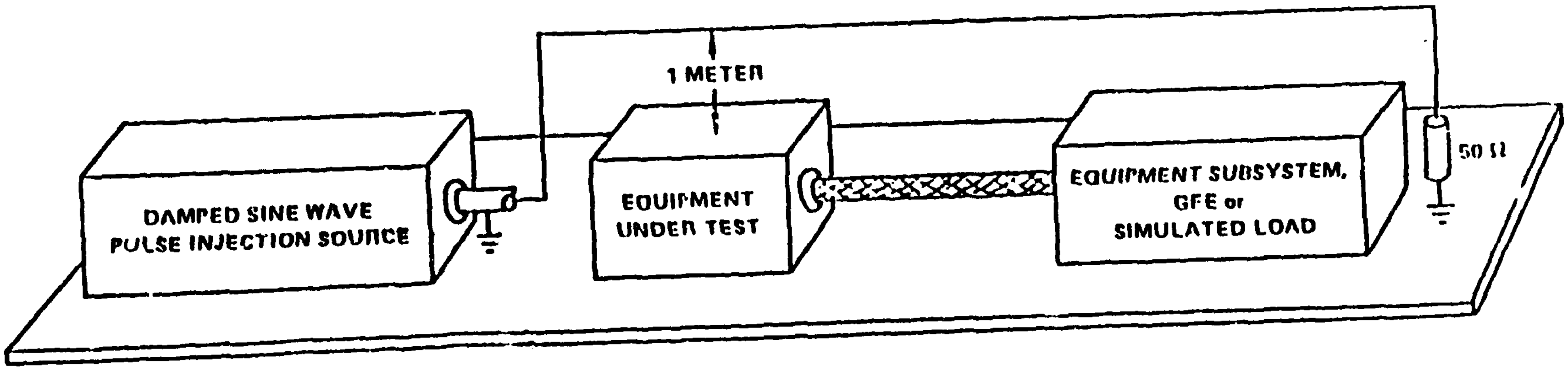


Figure 10.17 Electromagnetic Field Test Method

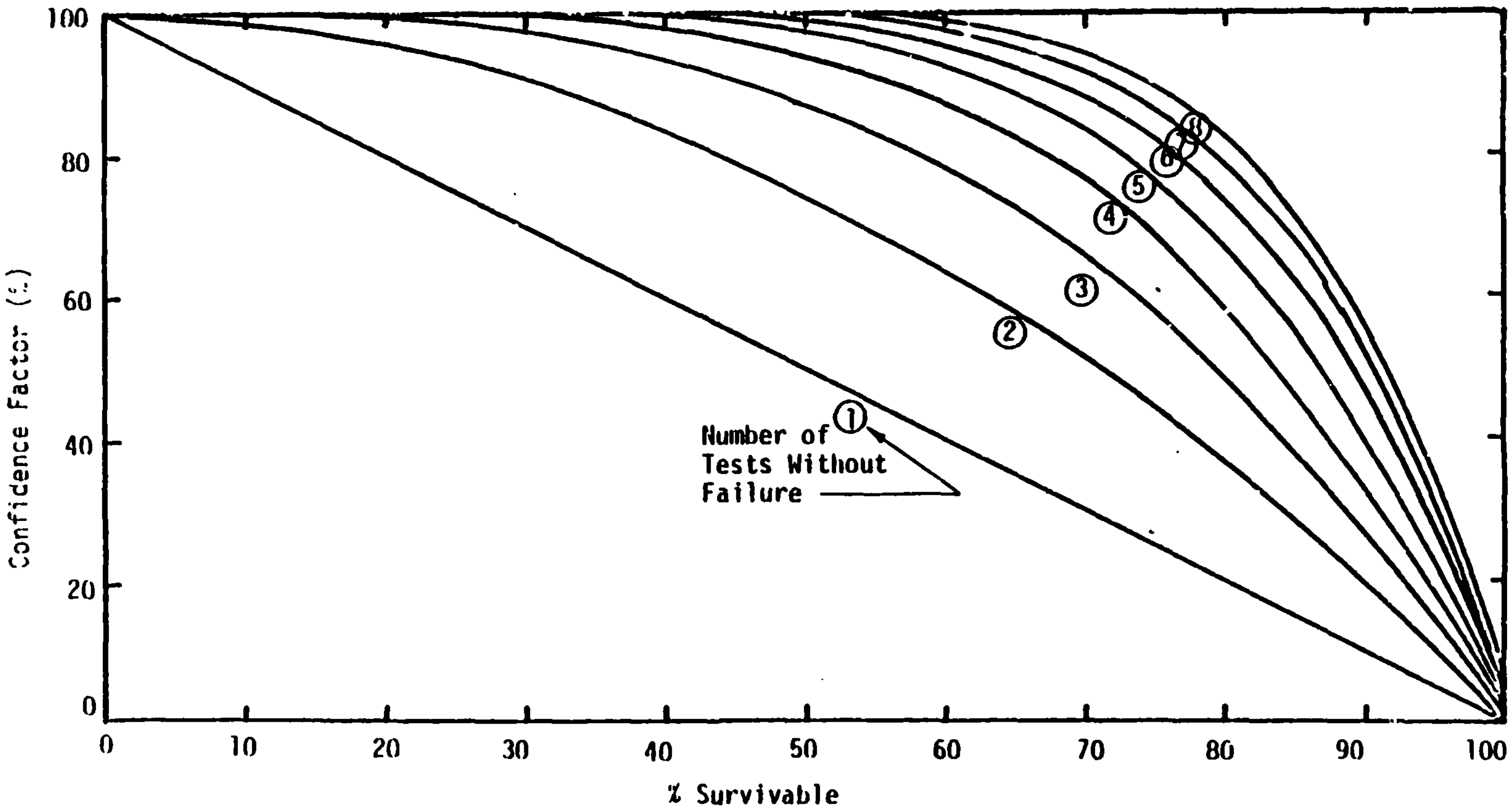


Figure 10.18 Confidence Factor Versus Survivability

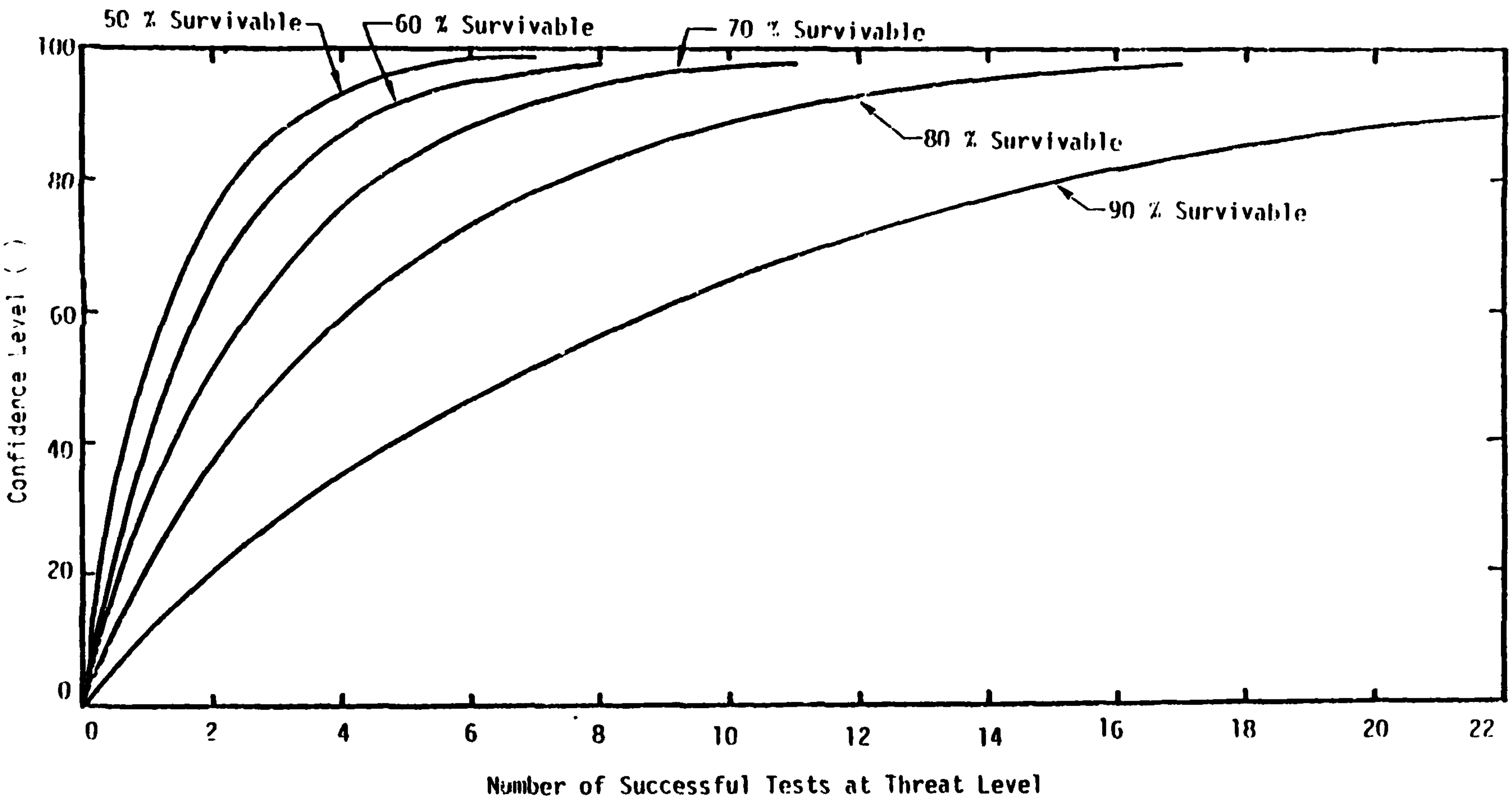


Figure 10.19 Confidence Level Versus Number of Successful Tests at Threat Level

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10.1 "Engineering Techniques for Electromagnetic Pulse Hardness Testing," DNA 3332F, no date.

10.2 "Electromagnetic Pulse (EMP) Specification Applications Handbook," WL-TR-79-162, no date.

10.3 "Equipment EMP Survivability Criteria," NSWC-SOW-C8013, no date.

10.4 "Surface Transfer Impedance Measurements of Navy Shielded Cables," Chapter 9, NSWC, Contract # N60921-74-C-0176.

10.5 Rickets, L.W., et.al., "EMP Radiation and Protective Techniques," Wiley-Interscience, 1976.

CHAPTER 11

HARDNESS ASSURANCE, MAINTENANCE, AND SURVEILLANCE

11.0 Executive Summary

Once equipment has been developed and determined to be hard, there is a question on whether production models are hard and that they will remain hard during their life cycle. For example, during the manufacturing process, a hardness check on production units should be conducted (hardness assurance). In addition, during the operational life of the equipment, usage and the environment may degrade system hardness. It is therefore also necessary to determine if hardness of installed equipment has degraded (surveillance) and to perform the necessary maintenance procedures to keep it hard. In order to accomplish hardness assurance, surveillance, and maintenance, it is necessary for the equipment manufacturer to develop a hardness program plan. The features of this plan are discussed in this chapter.

11.1 Background [11.1]

The purpose of this section is to set forth the responsibilities of the contractor in the preparation of a "Hardness Assessment, Surveillance, and Maintenance Plan" for EMP critical equipments to be produced and delivered to the Navy for shipboard use.

Each such plan is device specific and must be developed by the contractor at the time of device certification so that the Navy logistics agencies may incorporate the plan into the overall shipboard equipment maintenance program.

Hardness surveillance and maintenance for EMP is a discipline which is still in its infancy. The basic objective of this discipline is to counter the deleterious aging and operational environment influences on subsystem EMP hardness. Conclusive evidence of aging impacts on semiconductor hardness which is the majority of the critical device hardening problem is non-existent. Data on normal conductor skin aging does not reveal any aging impact. The current assumption is that aging does not significantly degrade piece part hardness so no surveillance or maintenance requirements are levied to counter any such possible effects.

The only requirement currently levied by specification are for configuration control, piece part control of replacement hardness components, and surveillance frequency. The contractor shall minimally address these issues in his plan and should add additional requirements as dictated by specific design considerations.

Hardness reliability is the probability that the EMP protective system will continue to meet operational requirements over a specified time interval, given that it was working at the beginning of the interal.

To achieve high hardness reliability requires a Hardware Assurance Program conducted by the Navy and the hardness critical equipment manufacturer during production. It requires that all personnel whose activity in any way involves the hardness critical systems be trained regarding the purpose of such hardness and the realities of maintaining this hardness on ship. A hardness surveillance program must be incorporated which is directed at the specific

peculiarities of the hardness critical equipment. Then if surveillance reveals any failures a Hardness Maintenance Program is put into effect to return the equipment to its initial level of hardness.

These Hardness Reliability Program elements are discussed in the following sections.

11.2 Hardness Degradation

The primary sources of hardness degradation result from structural degradation, mechanical damage, improper handling or use, improper hardness configuration control, poor hardness control for replacement parts, and the general lack of knowledge, training, and sensitivity to, and regarding, hardness criteria and technology.

The contractor shall address those areas of the hardness critical system in his plan and shall suggest the appropriate training. surveillance and maintenance procedures necessary to minimize the degradation of system hardness.

11.3 Hardness Assurance

Hardness Assurance is the process of assessing sufficient production models of a system, subsystem or hardness critical item (HCI) to ensure that the specification is being met by production units.

Hardness Assurance is concerned with maintaining system hardness during the production which follows successful system or HCI certification testing and before the system is operationally deployed. The task is necessitated by vagueries in the production process and statistical uncertainties in the unique characteristics of the components comprising the system, subsystem and HCIs.

Component sample failure tests are viewed as a necessity for an effective hardness assurance program and are to be included as a requirement in the production specifications.

A decision must be made based upon cost effectiveness versus hardness uncertainty relative to the desirability of performing line replacable unit (LRU) tests to increase confidence in EMP hardening. Two types of tests are possible, test to failure and test to specification.

Test to specification level has a cost advantage if the tested units can be utilized following the test. If the reliability impact of overstress testing is not known and the tested units cannot enter the operational inventory, then the cost advantage is lost and test to failure should be pursued.

Tests to failure provide more specific information about failure thresholds and on a sampling basis are considered desirable for high confidence hardness assurance.

Cost trade off analysis shall be prepared by the contractor and submitted along with his recommendations and program plan to the Navy for approval at the time of certification testing.

The manufacturer shall develop an EMP Hardness Assurance Program which shall ensure that design changes do not occur during the production phase that can dramatically affect system hardness by changing circuit configurations. This EMP Hardness Assurance Plan will document the procedures which the production contractor will employ to effect EMP configuration control and piece part hardness control. The configuration control plan and piece part hardness control procedure shall be submitted immediately following device certifications. The production contractor is further required to provide details relative to this proposed LRU Hardness Assurance Test Plan.

Once developed and approved by the Navy these procedures must be enforced by the contractor to make certain that changes in circuit configuration do not occur without their impact on damage and upset hardness being analyzed and the system recertified.

11.4 Hardness Training

An essential ingredient to Hardness Reliability is the training of all persons who directly or marginally are associated with EMP hardened systems.

The production contractor shall provide as part of his production contract EMP hardness training material for use in hardness awareness briefings for all technical and managerial levels associated directly or peripherally with the hardened system. He shall additionally provide material for use in hardness proficiency training for hardware engineers and technicians explaining how to use the available hardness information and data to accomplish the redesign, reprovisioning and repair of hardened systems without inadvertently degrading hardness information and data to accomplish the redesign, reprovisioning and repair of hardness systems without inadvertently degrading hardness. Engineering instructions for design hardening techniques which can be implemented in hardened systems and HCIs for each applicable nuclear environment shall be provided.

All of the training material shall be specific in regard to its applicability to the devices addressed by the production contract.

In the development of a hardness training program specific attention must be directed toward those organizations whose activities are considered potential sources of inadvertent hardness degradation. They must be made aware of the potential problem and thoroughly briefed regarding the scope of hardness maintenance and the mechanics by which the HM Program will be implemented.

11.5 Hardness Critical Items (HCI)

An essential element in the implementation of a hardness maintenance program is the identification of the hardness critical items (HCI) associated with each hardened system.

The contractor will list the part numbers of all HCIs and submit these as an appendix to his Hardness Assurance Surveillance and Maintenance Plan. The hardness requirements of each HCI shall be indicated and the specific hardness design features of the equipment, which enable it to survive all applicable hardness requirements, shall be identified and described.

11.6 Hardness Surveillance

An EMP protection system behaves in an off-line standby mode. Therefore, the system must be checked periodically to insure that the system continues to meet performance requirements. The surveillance effort is therefore less important if the EMP system is highly reliable. For this reason the cost of the system reliability may be traded off against the cost of system surveillance.

Hardness surveillance techniques can significantly degrade system hardness reliability through the use of high-stress environments during surveillance. It has been observed that the reliability of an EMP protected system may be inversely related to the surveillance frequency.

The Hardness Surveillance Program shall start with an evaluation of the potential for degradation due to age and operational factors associated with each HCI. It is necessary to identify the design features and degradation mechanisms of each HCI, which could lead to a serious degradation of system level hardness. Additionally, the production contractor shall identify the appropriate tests and inspection techniques requisite to the early detection of hardness degradation in each listed HCI.

The contractor is responsible for providing an information management system capability sufficient for the collection of statistical data relative to the degradation of performance of HCIs for the purpose of anticipating incipient failure modes in the fleet equipment inventory.

The contractor shall develop a Hardness Surveillance Program which will periodically inspect or evaluate each hardness critical operational system or subsystem to assure that no hardness degradation has occurred.

11.7 Hardness Maintenance [11.1]

Hardness Maintenance is the repair of all operational systems or subsystems as a result of a deficient finding during hardness surveillance.

The responsibility for the development of the hardness maintenance program is vested with the Navy logistics personnel and their associate contractors. They have the specific responsibility of defining the hardness maintenance program during the procurement and production phase of the device life cycle as it is an integral part of the equipment acquisition process specifically associated with the integrated logistics support plan.

For each hardness critical system a decision must be made relative to the most cost effective method to effect the hardness maintenance program. The choices available will assign the program responsibility to local authority (shipboard depot), or government/contractor test facility.

If the local authority is selected as the responsible maintenance organization then the program must provide a comprehensive hardness training program for the responsible organizations. This program will be tailored to the specific needs of the responsible authority.

The hardness maintenance program must provide the resources to (1) redesign hardened equipment, (2) reprovision hardened parts, (3) repair hardened

equipment, and (4) survey hardened equipment. These resources will include all the hardness information/data required to develop and implement the capability to redesign, reprovision, and repair hardened systems without inadvertently degrading hardness. The hardness information/data requirements need to include identification to the lowest level at which hardness requirements are defined and identification of all deployed equipment configurations. If system hardness is the result of numerous hardness modifications, adequate data must be available to provide configuration tracability to each modification.

The contractors plan shall be developed under the guidance of the Navy logistics authority and shall be submitted for review and approval at the time of certification test.

11.8 Summary of Contractor Responsibilities

11.8.1 Prepare a Hardness Assurance Surveillance and Maintenance Plan (HA/S/M) and submit to Navy 30 days prior to certification testing.

11.8.1.1 The HA/S/M Plan shall include details of configuration control, hardened price part control, and surveillance frequency along with any other device specific requirements.

11.8.1.2 Prepare recommendations on the testing of Line Replacable Units (LRUs). Discuss the consequences of testing to specification limits and contrast with the benefits of testing to failure. Present cost trade off analysis for the two techniques.

11.8.1.3 Submit a LRU Hardness Assurance test plan to Navy at the time of certification testing.

11.8.1.4 Enforce configuration control and hardened piece part control throughout the production cycle of the hardened device.

11.8.2 Develop specific training material directed to the user organization relative to the care and handling of the EMP hardened system.

11.8.2.1 The material shall include a briefing presentation for all managers, engineers and technicians, involved directly or indirectly in the care and use of EMP hardened systems.

11.8.2.2 The training program will include hardness proficiency training material for engineers and technicians.

11.3.2.3 The training program will include engineering instruction on the design hardening techniques incorporated in the hardened device.

11.8.3 The contractor will provide a list of all hardness critical items (HCIs) at the time of certification testing.

11.8.3.1 The HCI list will specify the hardness requirements imposed on each HCI.

11.3.3.2 The HCI list will indicate the design features used to satisfy the EMP hardness requirement on each HCI.

11.8.3.3 The HCI list will indicate the anticipated degradation mechanisms associated with the EMP hardened devices. Specifically address the issues of aging operations, and misuse degradation and indicate the surveillance and protection techniques associated with each degradation mechanism.

11.8.4 The contractor shall present surveillance test and inspection techniques for each HCI.

11.8.4.1 The contractor shall prepare a management information system to accumulate and statistically analyze the results of the surveillance program so that incipient failures in the deployed inventory may be averted.

11.8.5 The contractor shall develop a hardness surveillance plan to be implemented by the Navy on shipboard. This program will be submitted to the Navy at the time of certification testing for inclusion in logistics operating procedures.

11.8.5.1 The hardness surveillance plan will identify specific maintenance actions to be taken when failure of an HCI is detected.